512Kx8 MONOLITHIC SRAM *PRELIMINARY**

FEATURES

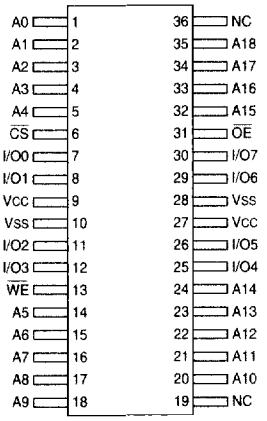
- Access Times 15, 17, 20, 25ns
- Low Power BiCMOS
- Revolutionary, Center Power/Ground Pinout JEDEC Approved
  - 36 lead Ceramic SOJ (Package 100)
  - 36 lead Ceramic Flat Pack (Package 200)
- Evolutionary, Corner Power/Ground Pinout JEDEC Approved
  - 32 pin Ceramic DIP (Package 300)
  - 32 lead Ceramic SOJ (Package 101)
  - 32 lead Ceramic Flat Pack (Package 206)
- BiCMOS:
  - Radiation Tolerant with Epitaxial Layer Die
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

REVOLUTIONARY PINOUT

36 FLAT PACK
36 CSOJ

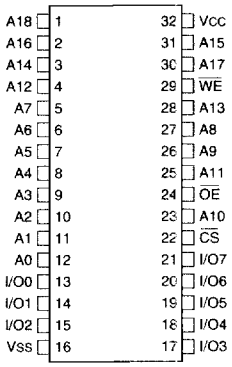
TOP VIEW



EVOLUTIONARY PINOUT

32 DIP
32 CSOJ (DE)
32 FLAT PACK (FE)

TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		140	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		ns
Address Access Time	t_{AA}		15		17		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25	ns
Output Enable to Output Valid	t_{OE}		7		9		10		12	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		9		10		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		9		10		12	ns

1. This parameter is guaranteed by design but not tested.

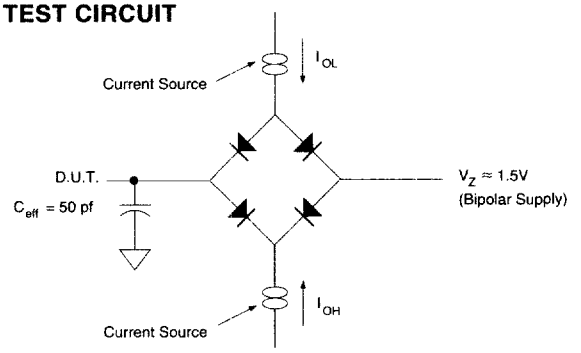
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-15		-17		-20		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		ns
Chip Select to End of Write	t_{CW}	12		14		15		17		ns
Address Valid to End of Write	t_{AW}	12		14		15		17		ns
Data Valid to End of Write	t_{DW}	7		9		10		12		ns
Write Pulse Width	t_{WP}	12		14		15		17		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		7		9		9		10	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

ORDERING INFORMATION

W M S 512K 8 B - XXX X X E X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

E = Epitaxial Layer

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

PACKAGE:
C = 32 Pin Ceramic .600" DIP (Package 300)
DE = 32 Lead Ceramic SOJ (Package 101) Evolutionary
DJ = 36 Lead Ceramic SOJ (Package 100)
F = 36 Lead Ceramic Flat Pack (Package 200)
FE = 32 Lead Ceramic Flat Pack (Package 206)

ACCESS TIME (ns)

BiCMOS

ORGANIZATION, 512K x 8

SRAM

MONOLITHIC

WHITE MICROELECTRONICS