To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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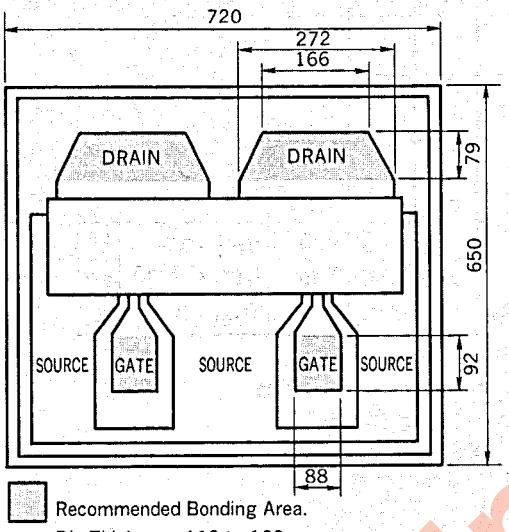
RENESAS

GaAs MES FET
NE8002

C-BAND MEDIUM POWER GsAs FET
N-CHANNEL GaAs MES FET

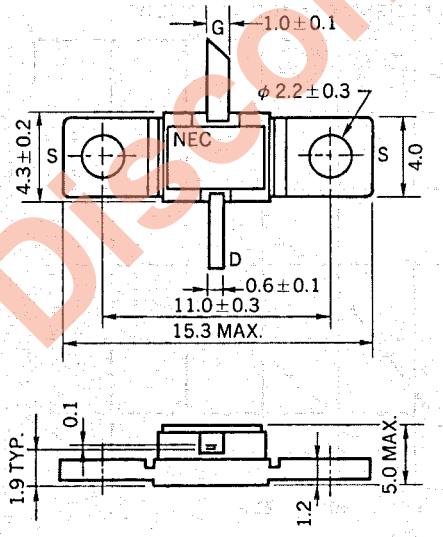
Discontinued Product

PACKAGE DIMENSIONS
NE800200 (CHIP)
(Units in mm)



Recommended Bonding Area.
Die Thickness: 110 to 160 μm

PACKAGE CODE-96/99
(Units in mm)



DESCRIPTION

The NE8002 is a GaAs power FET offering a recessed gate structure which provides high break-down and operating voltages. The device operates with a drain voltage (V_{DS}) of 9 V for CW circuits and up to 13 V for pulsed circuits.

FEATURES

- $P_{O(1\ dB)}$ = 29.0 dBm, G_L = 9.0 dB @ V_{DS} = 9 V, f = 7.2 GHz (NE800296), 8.4 GHz (NE800299)
- Hermetically sealed package assures high reliability.

ORDERING INFORMATION

PART NUMBER	PACKAGE CODE
NE800200	00(CHIP)
NE800296	96
NE800299	99

ABSOLUTE MAXIMUM RATING (T_a = 25 °C)

Drain to Source Voltage	V_{DS}	20	V
Gate to Source Voltage	V_{GS}	−14	V
Drain Current	I_D	1.0	A
Gate Current	I_G	3.0	mA
Total Power Dissipation	P_T	5.0*1	W

*1 T_C = 25 °C

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ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Saturated Drain Current	I_{DSS}	450	600	800	mA	V_{DS} = 2.5 V, V_{GS} = 0
Pinch-off Voltage	V_P	−2.5	−3.5	−5	V	V_{DS} = 2.5 V, I_D = 4 mA
Transconductsnce	g_m		120		mS	V_{DS} = 3 V, I_D = 250 mA
Thermal Resistance	R_{th}		30	32	°C/W	channel to case

PERFORMANCE SPECIFICATIONS (T_a = 25 °C)

PART NUMBER		NE800200			NE800296			NE800299			UNIT	TEST CONDITIONS	
PACKAGE CODE		CHIP			96			99					
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
Output Power*2	P_{out}	28	29		28	29					dBm	V_{DS} = 9 V, $I_D \leqq$ 300 mA	P_{in} = 21.0 dBm, f = 7.2 GHz
								28	29		dBm		P_{in} = 21.5 dBm, f = 8.4 GHz
Output Power at 1 dB Gain Compression Point	$P_{O(1\ dB)}$		29			29					dBm	V_{DS} = 9 V, $I_D \leqq$ 275 mA	f = 7.2 GHz
									29		dBm		f = 8.4 GHz
Linear Gain	G_L		9.0			9.0					dB	V_{DS} = 9 V, $I_D \leqq$ 275 mA	f = 7.2 GHz
									9.0		dB		f = 8.4 GHz
Power Added Efficiency*3	η_{add}		38			38			38		%	$P_{out} = P_{O(1\ dB)}$	

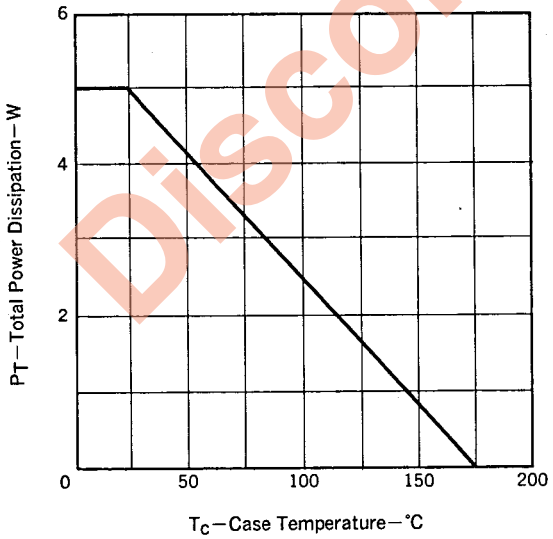
*2 Devices are measured in a tuned amplifier circuit.
The drain current, I_D, is 200 to 300 mA and the gate current is limited below the absolute maximum rating.

*3 $$\eta_{add} = \frac{P_{O(1\ dB)} - P_{in}}{V_{DS} \times I_D} \times 100\ (\%)$$

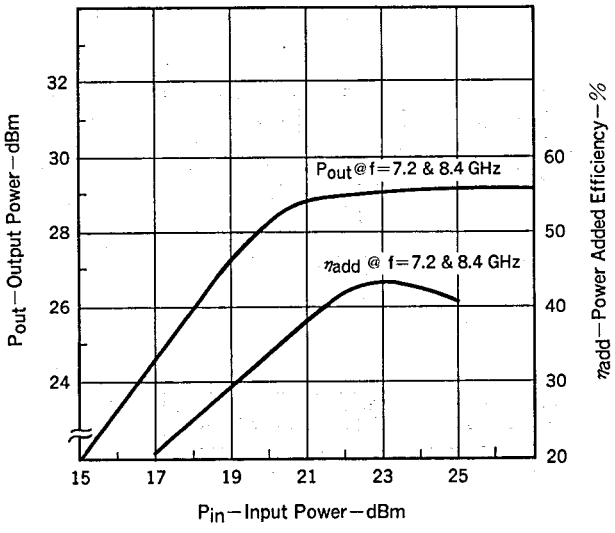
Discontinued Product

TYPICAL CHARACTERISTICS

POWER DERATING CURVE



NE800296, NE800299
OUTPUT POWER AND POWER ADDED EFFICIENCY vs. INPUT POWER



S-PARAMETER

NE800200 (V_{DS} = 9 V, I_D = 300 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.882	−109.4	5.171	113.9	0.051	34.4	0.225	−75.3
2000	0.858	−144.3	2.940	87.6	0.057	20.0	0.237	−106.8
3000	0.852	−159.3	2.007	73.2	0.057	17.3	0.267	−109.8
4000	0.848	−167.5	1.504	60.1	0.054	17.7	0.337	−118.1
5000	0.848	−172.6	1.194	49.5	0.053	23.3	0.400	−122.6
6000	0.846	−177.3	0.979	39.5	0.051	27.8	0.457	−128.4
7000	0.840	179.1	0.818	31.7	0.051	46.5	0.500	−131.5
8000	0.835	175.5	0.723	23.9	0.091	32.7	0.526	−137.6
9000	0.856	173.3	0.626	15.5	0.064	37.8	0.590	−140.0
10000	0.861	171.1	0.553	8.6	0.071	42.2	0.631	−145.6
11000	0.854	168.5	0.495	2.1	0.081	44.2	0.663	−148.5
12000	0.840	164.8	0.436	−4.7	0.089	44.0	0.690	−153.4
13000	0.835	161.2	0.389	−10.1	0.099	41.8	0.711	−157.8
14000	0.838	158.8	0.345	−14.6	0.105	39.9	0.726	−162.7
15000	0.841	158.0	0.309	−18.1	0.111	39.7	0.742	−165.1
16000	0.830	156.5	0.280	−22.5	0.119	37.9	0.748	−167.2
17000	0.797	153.7	0.250	−24.6	0.131	36.7	0.744	−170.0
18000	0.772	150.1	0.233	−27.5	0.141	31.0	0.747	−174.6

NE800296 (V_{DS} = 9 V, I_D = 300 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.871	−136.8	4.691	91.3	0.046	23.4	0.183	−114.5
2000	0.845	−171.1	2.630	57.0	0.049	13.9	0.234	−145.9
3000	0.831	170.8	1.946	30.4	0.053	9.0	0.309	−162.7
4000	0.796	156.9	1.729	6.1	0.060	10.8	0.380	−174.4
5000	0.708	138.4	1.833	−22.6	0.079	0.3	0.471	175.6
6000	0.372	97.4	2.276	−67.0	0.098	−30.8	0.633	161.9
7000	0.501	−119.2	1.938	−140.7	0.051	−103.8	0.774	128.3
8000	0.842	−165.6	0.962	163.3	0.034	81.4	0.689	99.6
9000	0.869	171.5	0.518	119.1	0.092	35.5	0.630	76.9
10000	0.752	156.3	0.301	60.0	0.164	−6.9	0.565	50.9

NE800299 (V_{DS} = 9 V, I_D = 300 mA)

frequency (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
1000	0.845	−132.4	5.340	93.6	0.048	27.0	0.201	−118.6
2000	0.809	−171.8	2.926	58.0	0.051	17.8	0.251	−153.8
3000	0.810	167.7	2.039	31.4	0.055	13.8	0.328	−171.5
4000	0.812	152.3	1.626	7.7	0.062	14.9	0.406	173.8
5000	0.800	137.0	1.415	−14.8	0.077	12.6	0.472	161.3
6000	0.773	118.5	1.340	−38.4	0.095	1.7	0.534	147.3
7000	0.716	92.0	1.338	−65.9	0.113	−14.0	0.592	132.9
8000	0.636	52.1	1.351	−99.4	0.125	−39.2	0.665	115.0
9000	0.601	−6.7	1.282	−141.0	0.107	−75.7	0.734	93.0
10000	0.613	−68.1	1.071	174.6	0.056	−128.2	0.752	68.9

Discontinued Product

CHIP HANDLING

DIE ATTACHMENT

Die attach can be accomplished with a Au-Sn (300 ± 10 °C) preforms in a forming gas environment. Epoxy die attach is not recommended.

BONDING

Gate and drain bonding wires should be minimum length, semi-hard gold wire (3-8 % elongation) 30 microns or less in diameter. Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Die attach and bonding time should be kept to a minimum. As a general rule, the bonding operation should be kept within a 280 °C — 5 minute curve. If longer periods are required, the temperature should be lowered.

PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

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[MEMO]

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