150-mA Ultra Low-Noise LDO Regulator With Discharge Option

FEATURES

- Ultra Low Dropout—130 mV at 150-mA Load
- Ultra Low Noise—30 μ$V_{(rms)}$ (10-Hz to 100-kHz Bandwidth)
- Shutdown Control
- 110-μA Ground Current at 150-mA Load
- 1.5% Guaranteed Output Voltage Accuracy
- 300-mA Peak Output Current Capability
- Uses Low ESR Ceramic Capacitors
- Fast Start-Up (50 μs)
- Fast Line and Load Transient Response (≤ 30 μs)
- 1-μA Maximum Shutdown Current
- Output Current Limit
- Reverse Battery Protection
- Built-in Short Circuit and Thermal Protection

Pb-free Available

- Output, Auto-Discharge In Shutdown Mode
- Fixed 1.8, 2.5, 2.6, 2.8, 2.85, 2.9, 3.0, 3.3, 5.0-V Output Voltage Options
- Thin SOT23-5 Package

APPLICATIONS

- Cellular Phones, Wireless Handsets
- Noise-Sensitive Electronic Systems, Laptop and Palmtop Computers
- PDAs
- Pagers
- Digital Cameras
- MP3 Player
- Wireless Modem

DESCRIPTION

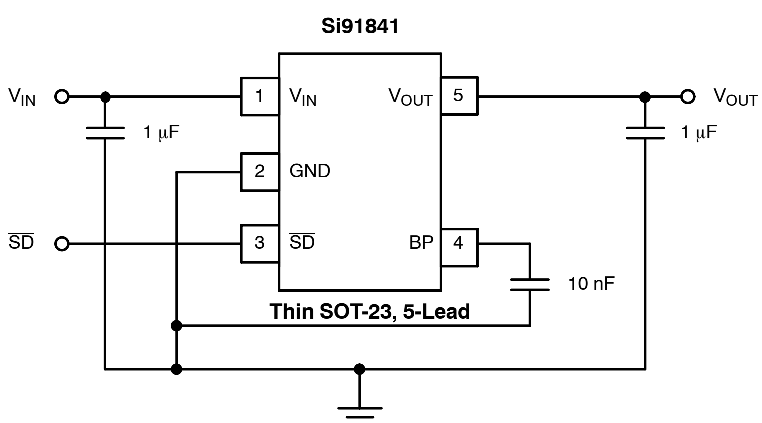
The Si91841 is a 150-mA CMOS LDO (low dropout) voltage regulator. It is the perfect choice for low voltage, low power applications. An ultra low ground current makes this part attractive for battery operated power systems. The Si91841 also offers ultra low dropout voltage to prolong battery life in portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the Si91841's ultra low output noise. An external noise bypass capacitor connected to the device's BP pin can further reduce the noise level. The Si91841 is designed to maintain regulation while delivering 300-mA peak current, making it ideal for systems that have a high surge current upon turn-on.

For better transient response and regulation, an active pull-down circuit is built into the Si91841 to clamp the output voltage when it rises beyond normal regulation. The Si91841 automatically discharges the output voltage by connecting the output to ground through a 100-Ω n-channel MOSFET when the device is put in shutdown mode.

The Si91841 features reverse battery protection to limit reverse current flow to approximately 1-μA in the event reversed battery is applied at the input, thus preventing damage to the IC.

The Si91841 is available in both standard and lead (Pb)-free packages.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings
Input Voltage, V_{IN} to GND . . . . –6.0 to 6.5 V
$V_{\overline{SD}}$ (See Detailed Description) . . . . –0.3 V to V_{IN}
Output Current, I_{OUT} . . . . Short Circuit Protected
Output Voltage, V_{OUT} . . . . –0.3 V to V_{IN} + 0.3 V
Package Power Dissipation, (P_d)[b] . . . . 440 mW

Package Thermal Resistance, (θ_{JA})[a] . . . . 180°C/W
Maximum Junction Temperature, $T_{J(max)}$ . . . . 150°C
Storage Temperature, T_{STG} . . . . –65°C to 150°C

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 5.5 mW/°C above T_A = 70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN} . . . . 2 V to 6 V
Input Voltage, $V_{\overline{SD}}$ . . . . 0 V to V_{IN}

Operating Ambient Temperature, T_A . . . . –40°C to 85°C

C_{IN} = C_{OUT} = 1 µF (ceramic), C_{BP} = 0.01 µF (ceramic)
Maximum ESR of C_{OUT}: 0.4 Ω

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified T_A = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1 V I_{OUT} = 1 mA, C_{IN} = 1 µF, C_{OUT} = 1.0 µF $V_{\overline{SD}}$ = 1.5 V	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Start-Up BP Current	I_{OUT}	ON/$\overline{OFF}$ = High	Room		1		mA
Input Voltage Range	V_{IN}		Full	2		6	V
Output Voltage Accuracy	V_{OUT}	1 mA ≤ I_{OUT} ≤ 150 mA	Room	–1.5	1	1.5	%
			Full	–2.5	1	2.5	
Line Regulation (V_{OUT} ≤ 3 V)	$\frac{\Delta V_{OUT} \times 100}{\Delta V_{IN} \times V_{OUT(nom)}}$	From V_{IN} = $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V	Full	–0.06		0.18	%/V
Line Regulation (3.0 V < V_{OUT} ≤ 3.6 V)			Full	0		0.3	
Line Regulation (5-V Version)		From V_{IN} = 5.5 V to 6 V	Full	0		0.4	
Dropout Voltage[d, g] ($V_{OUT(nom)}$ ≥ 2.6 V)	$V_{IN} - V_{OUT}$	I_{OUT} = 1 mA	Room		1		mV
		I_{OUT} = 50 mA	Room		45	80	
			Full		50	90	
		I_{OUT} = 150 mA	Room		130	180	
			Full			220	
Dropout Voltage[d, g] ($V_{OUT(nom)}$ < 2.6 V, V_{IN} ≥ 2 V)		I_{OUT} = 50 mA	Room		65	100	
			Full			120	
		I_{OUT} = 150 mA	Room		190	250	
			Full			300	
Ground Pin Current[e, g] ($V_{OUT(nom)}$ ≤ 3 V)	I_{GND}	I_{OUT} = 0 mA	Room		100	150	µA
			Full			180	
		I_{OUT} = 150 mA	Room		110	200	
			Full			230	
Ground Pin Current[e] ($V_{OUT(nom)}$ > 3 V)		I_{OUT} = 0 mA	Room		110	170	
			Full			200	
		I_{OUT} = 150 mA	Room		120	200	
			Full			230	
Peak Output current	$I_{O(peak)}$	V_{OUT} ≥ 0.95 x $V_{OUT(nom)}$, t_{PW} = 2 ms	Full	300			mA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified $T_A = 25°C$, $V_{IN} = V_{OUT(nom)} + 1$ V, $I_{OUT} = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 1.0$ µF, $V_{\overline{SD}} = 1.5$ V		Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Output Noise Voltage	e_N	$V_{NOM} = 2.6$ V, BW = 10 Hz to 100 kHz, 0 mA < I_{OUT} < 150 mA, $C_{NOISE} = 0.01$ µF		Room		30		µV(rms)
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	$I_{OUT} =$ 150 mA	f = 1 kHz	Room		60		dB
			f = 10 kHz	Room		40		
			f = 100 kHz	Room		30		
Dynamic Line Regulation	$\Delta V_{O(line)}$	V_{IN} : $V_{OUT(nom)} + 1$ V to $V_{OUT(nom)} + 2$ V, $t_r/t_f = 2$ µs, $I_{OUT} = 150$ mA		Room		20		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	I_{OUT} : 1 mA to 150 mA, $t_r/t_f = 2$ µs		Room		20		
Thermal Shutdown Junction Temperature	$T_{J(S/D)}$			Room		150		°C
Thermal Hysteresis	T_{HYST}			Room		20		
Reverse current	I_R	$V_{IN} = -6.0$ V		Room		1		µA
Short Circuit Current	I_{SC}	$V_{OUT} = 0$ V		Room		700		mA
Shutdown								
Shutdown Supply Current	$I_{CC(off)}$	$V_{\overline{SD}} = 0$ V		Room		0.1	1	µA
$\overline{SD}$ Pin Input Voltage	$V_{\overline{SD}}$	High = Regulator ON (Rising)		Full	1.5		V_{IN}	V
		Low = Regulator OFF (Falling)		Full			0.4	
Auto Discharge Resistance	R_DIS	Si91841 Only		Room		100		Ω
$\overline{SD}$ Pin Input Current[f]	$I_{IN(\overline{SD})}$	$V_{\overline{SD}} = 1.5$ V, $V_{IN} = 6$ V		Room		0.7		µA
$\overline{SD}$ Hysteresis	$V_{HYST(\overline{SD})}$			Full		150		mV
V_{OUT} Turn-On Time	t_{ON}	$V_{\overline{SD}}$ (See Figure 1), $I_{LOAD} = 100$ nA				50		µS

Notes
a. Room = 25°C, Full = −40 to 85°C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT} \geq 2$ V are measured at $V_{OUT} = 3.3$ V, while typical values for dropout voltage at $V_{OUT} < 2$ V are measured at $V_{OUT} = 1.8$ V.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that V_{IN} does not not drop below 2.0 V.
e. Ground current is specified for normal operation as well as "drop-out" operation.
f. The device's shutdown pin includes a typical 2-MΩ internal pull-down resistor connected to ground.
g. $V_{OUT(nom)}$ is V_{OUT} when measured with a 1-V differential to V_{IN}.

TIMING WAVEFORMS

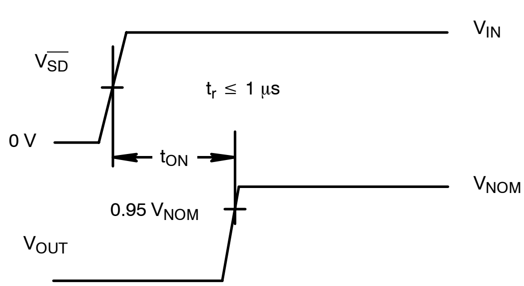
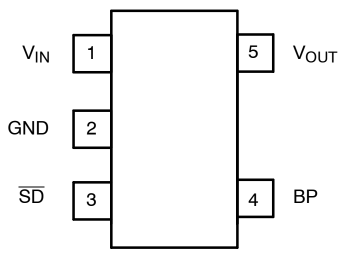


FIGURE 1. Timing Diagram for Power-Up

PIN CONFIGURATION

Thin SOT-23, 5-Lead



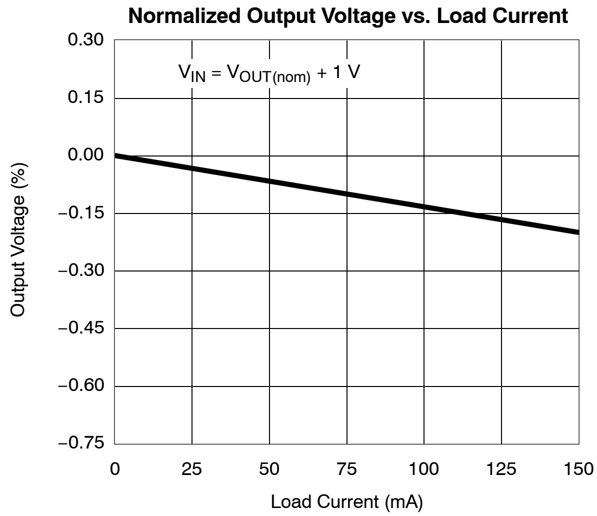
PIN DESCRIPTION		
Pin No.	**Name**	**Function**
1	V_{IN}	Input supply pin. Bypass this pin with a 1-μF ceramic or tantalum capacitor to ground
2	GND	Ground pin. For better thermal capability, directly connected to large ground plane
3	$\overline{SD}$	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused
4	BP	Noise bypass pin. For low noise applications, a 0.01 μF ceramic capacitor should be connected from this pin to ground.
5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.

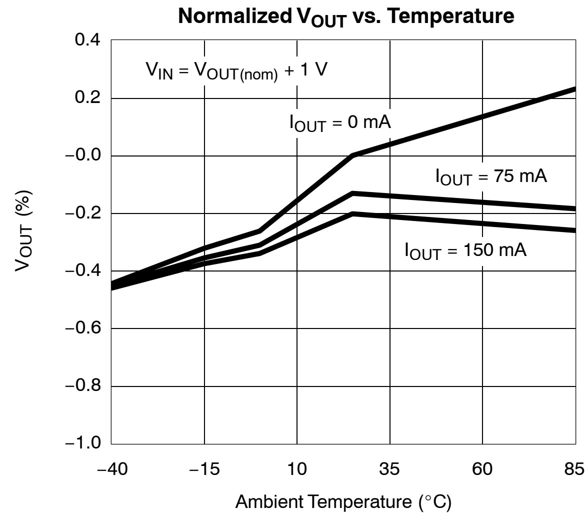
ORDERING INFORMATION—Si91841

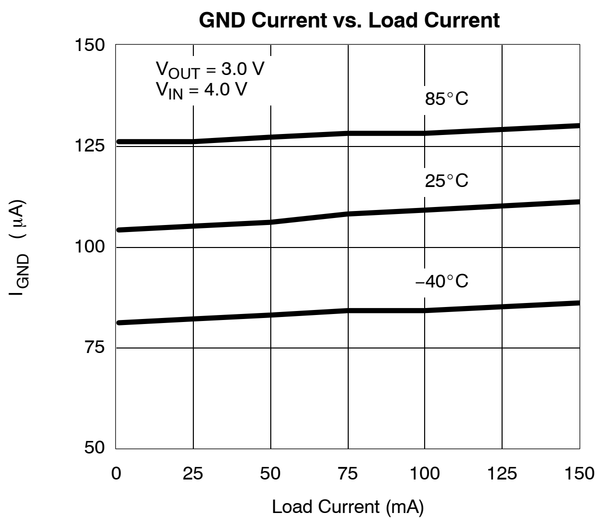
Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si91841DT-18-T1	Si91841DT-18-T1—E3	B4LL	1.8	−40 to 85°C	Thin SOT23-5
Si91841DT-20-T1	Si91841DT-20-T1—E3	B5LL	2.0		
Si91841DT-26-T1	Si91841DT-26-T1—E3	B8LL	2.6		
Si91841DT-27-T1	Si91841DT-27-T1—E3	B9LL	2.7		
Si91841DT-285-T1	Si91841DT-285—E3	C1LL	2.85		
Si91841DT-29-T1	Si91841DT-29-T1—E3	C2LL	2.9		
Si91841DT-30-T1	Si91841DT-30-T1—E3	C3LL	3.0		
Si91841DT-33-T1	Si91841DT-33-T1—E3	C4LL	3.3		
Si91841DT-35-T1	Si91841DT-35-T1—E3	C5LL	3.5		

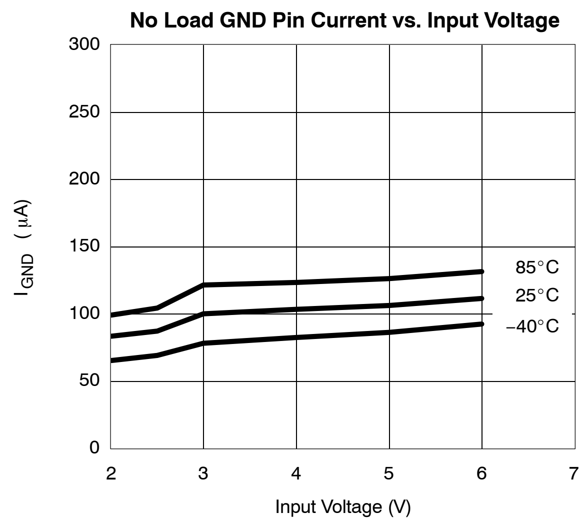
Note: LL = Lot Code

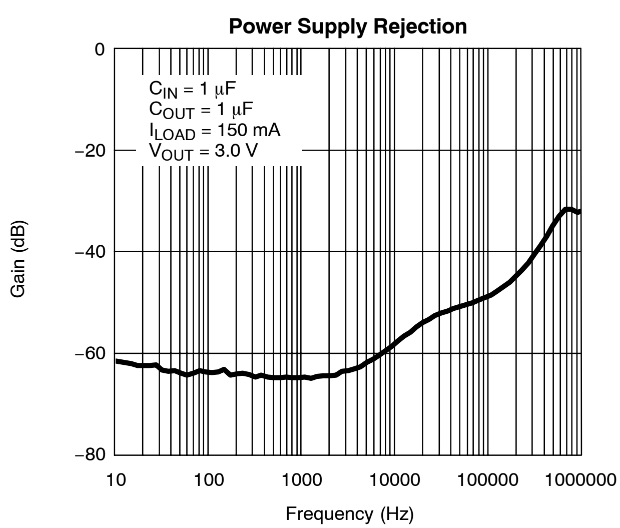
TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

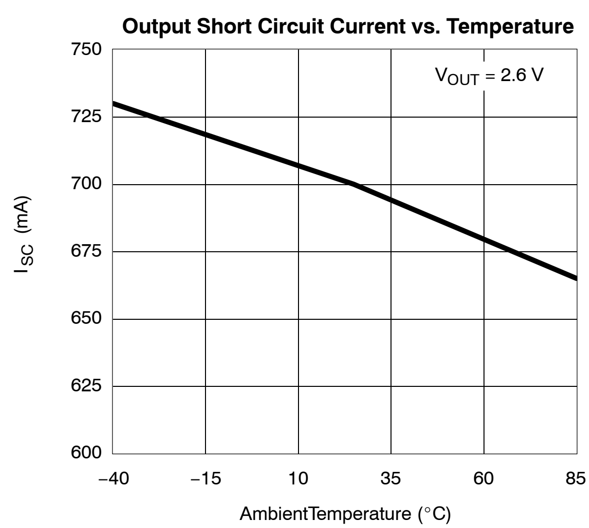




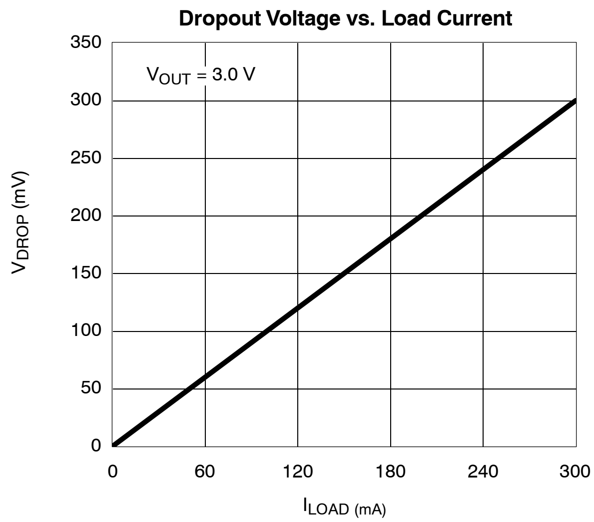


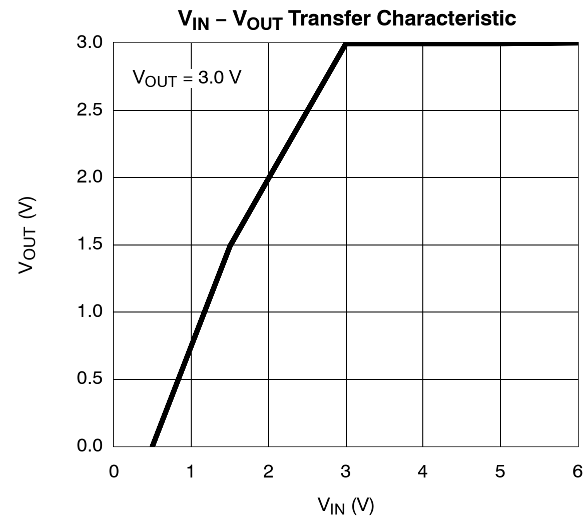


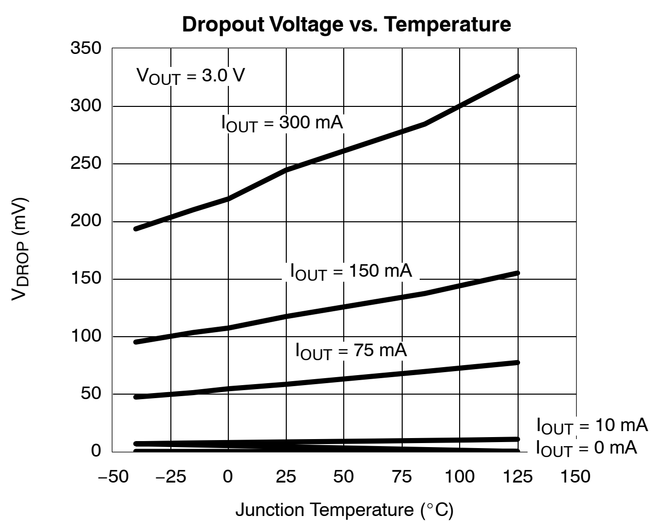


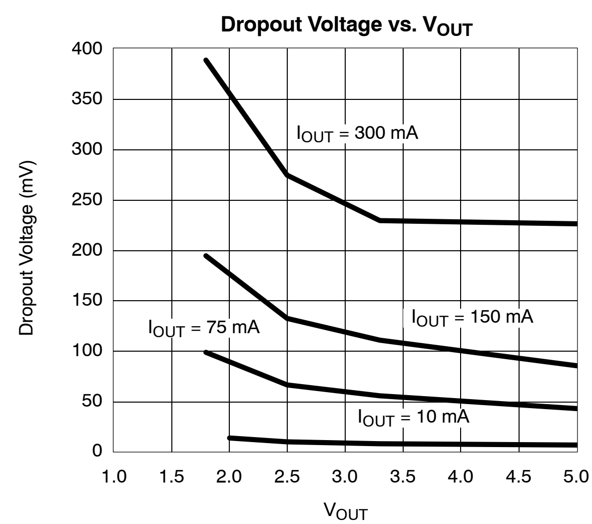


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)



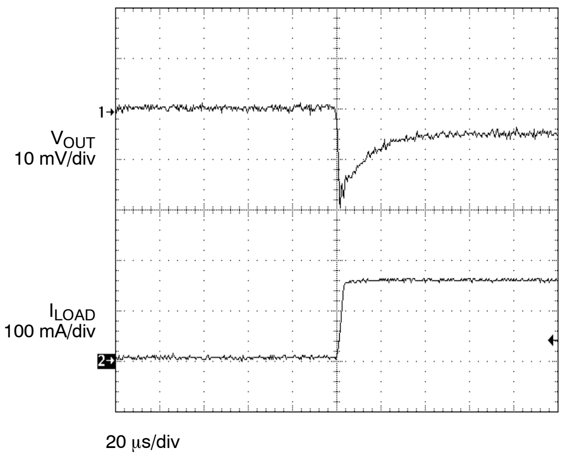






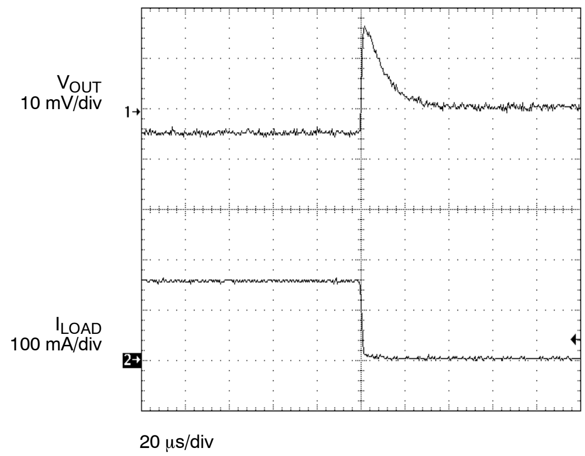
TYPICAL WAVEFORMS

Load Transient Response-1



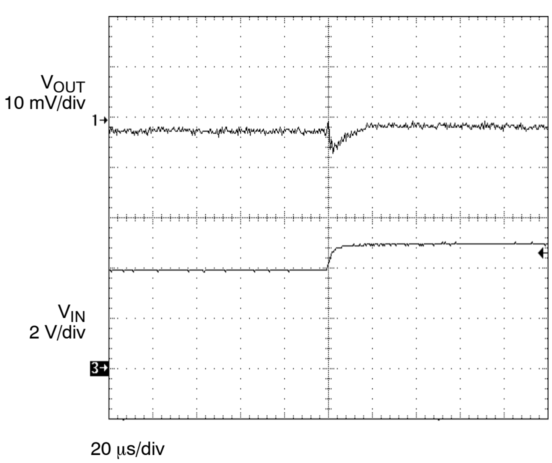
V_{OUT} = 3.0 V
C_{OUT} = 1 µF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 µsec

Load Transient Response-2



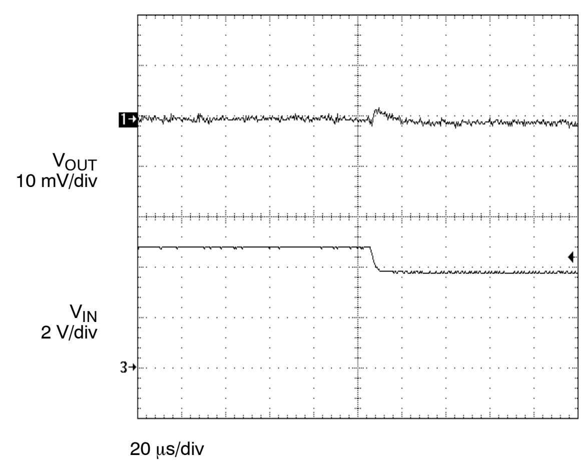
V_{OUT} = 3.0 V
C_{OUT} = 1 µF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 µsec

LineTransient Response-1



V_{INSTEP} = 4 to 5 V
V_{OUT} = 3 V
C_{OUT} = 1 µF
C_{IN} = 1 µF
I_{LOAD} = 150 mA
t_{rise} = 5 µsec

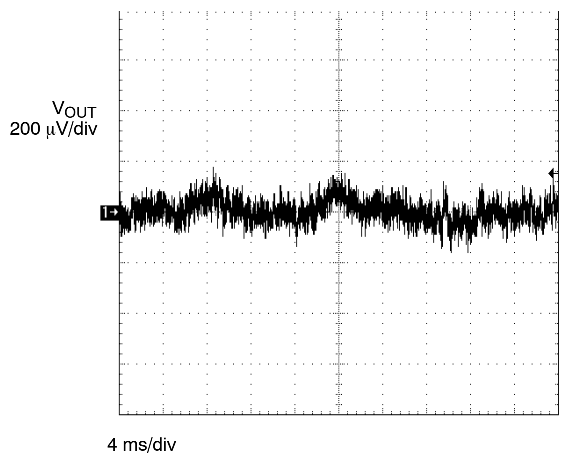
LineTransient Respons-2



V_{INSTEP} = 5 to 4 V
V_{OUT} = 3 V
C_{OUT} = 1 µF
C_{IN} = 1 µF
I_{LOAD} = 150 mA
t_{fall} = 5 µsec

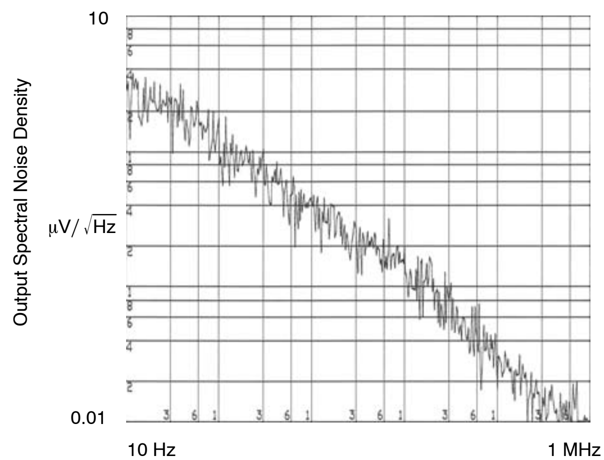
TYPICAL WAVEFORMS

Output Noise



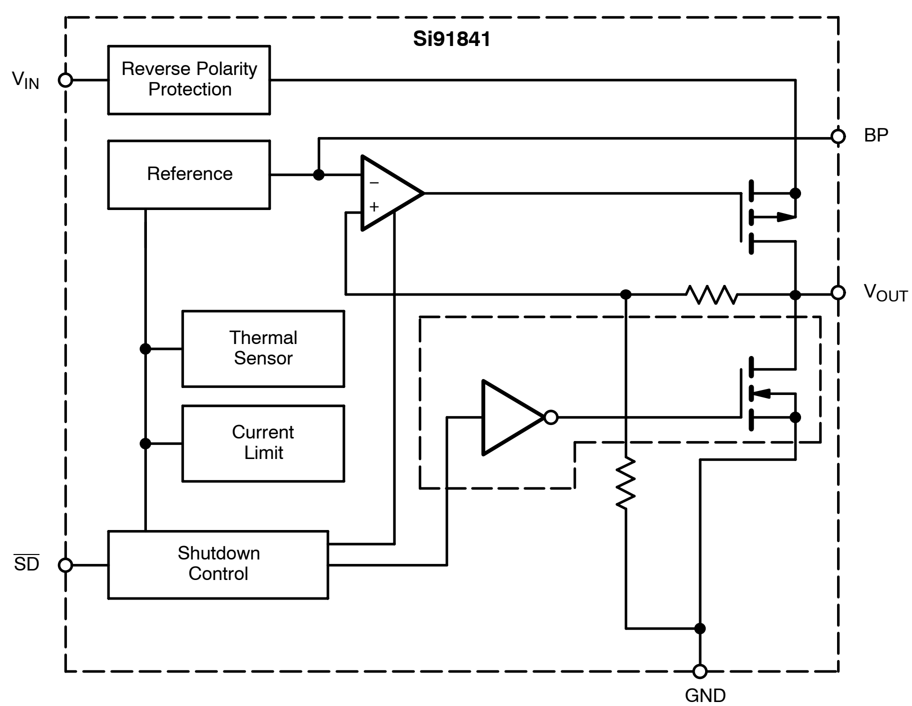
V_{IN} = 4 V
V_{OUT} = 3 V
I_{OUT} = 150 mA
C_{NOISE} = 0.01 µF
BW = 10 Hz to 100 kHz

Noise Spectrum



V_{IN} = 4 V
V_{OUT} = 3 V
I_{LOAD} = 150 mA
C_{NOISE} = 0.01 µF

BLOCK DIAGRAM



DETAILED DESCRIPTION

The Si91841 is a low-noise, low drop-out and low quiescent current linear voltage regulator, packaged in a small footprint Thin SOT23-5 package. The Si91841 can supply loads up to 150 mA. As shown in the block diagram, the circuit consists of a bandgap reference error, amplifier, p-channel pass transistor and feedback resistor string. An external bypass capacitor connected to the BP pin reduces noise at the output. Additional blocks, not shown in the block diagram, include a precise current limiter, reverse battery and current protection and thermal sensor.

Thermal Overload Protection

The thermal overload protection limits the total power dissipation and protects the device from being damaged. When the junction temperature exceeds 150°, the device turns the p-channel pass transistor off.

Reverse Battery Protection

The Si91841 has a battery reverse protection circuitry that disconnects the internal circuitry when V_{IN} drops below the GND voltage. There is no current drawn in such an event. When the $\overline{SD}$ pin is hardwired to V_{IN}, the user must connect the $\overline{SD}$ pin to V_{IN} via a 100-kΩ resistor if reverse battery protection is desired. Hardwiring the $\overline{SD}$ pin directly to the V_{IN} pin is allowed when reverse battery protection is not desired.

Noise Reduction

An external 10-nF bypass capacitor at BP is used to create a low pass filter for noise reduction. The start-up time is fast, since a power-on circuit pre-charges the bypass capacitor. After the power-up sequence the pre-charge circuit is switched to standby mode in order to save current. It is therefore not recommended to use larger bypass capacitor values than 50 nF. When the circuit is used without a capacitor, stable operation is guaranteed.

Auto-Discharge/No-Discharge

For Si91841 only, V_{OUT} has an internal 100-Ω (typ.) discharge path to ground when the $\overline{SD}$ pin is low. The Si91843 does not have a discharge path when the $\overline{SD}$ pin is low.

Stability

The circuit is stable with only a small output capacitor equal to 6 nF/mA (= 1 µF @ 150 mA). Since the bandwidth of the error amplifier is around 1–3 MHz and the dominant pole is at the output node, the capacitor should be capacitive in this range, i.e., for 150-mA load current, an ESR <0.4 Ω is necessary. Parasitic inductance of about 10 nH can be tolerated.