

74F620 • 74F623 Inverting Octal Bus Transceiver with TRI-STATE® Outputs

General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA and have TRI-STATE outputs. Dual enable pins (GAB, $\bar{G}BA$) allow data transmission from the A bus to the B bus or from the B bus to the A bus. The 'F620 is an inverting option of the 'F623.

Features

- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Dual enable inputs control direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F620 is an inverting option of the 'F623

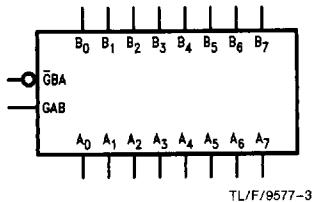
Ordering Code:

See Section 11

Commercial	Package Number	Package Description
74F620PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F623PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F623SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbol

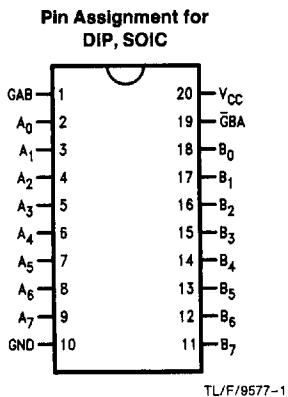


Unit Loading/Fan Out:

See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\bar{G}BA$, GAB A ₀ -A ₇	Enable Inputs A Inputs or TRI-STATE Outputs	1.0/1.0 3.5/1.083 150/40	20 μ A/-0.6 mA 70 μ A/-0.4 mA -3 mA/64 mA
B ₀ -B ₇	B Inputs or TRI-STATE Outputs	3.5/1.083 150/40	70 μ A/-0.4 mA -3 mA/64 mA

Connection Diagram



Functional Description

The enable inputs $\bar{G}BA$ and $\bar{G}AB$ control whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. If both $\bar{G}BA$ and $\bar{G}AB$ are disabled ($\bar{G}BA$ HIGH and $\bar{G}AB$ low), the outputs are in the high impedance state and data is stored at the A and B busses. When $\bar{G}BA$ is

active (LOW), B data is sent to the A bus. When $\bar{G}AB$ is active (HIGH), data from the A bus is sent to the B bus. If both enable inputs are active ($\bar{G}BA$ LOW and $\bar{G}AB$ HIGH) B data is sent to the A bus while A data is sent to the B bus.

Function Table

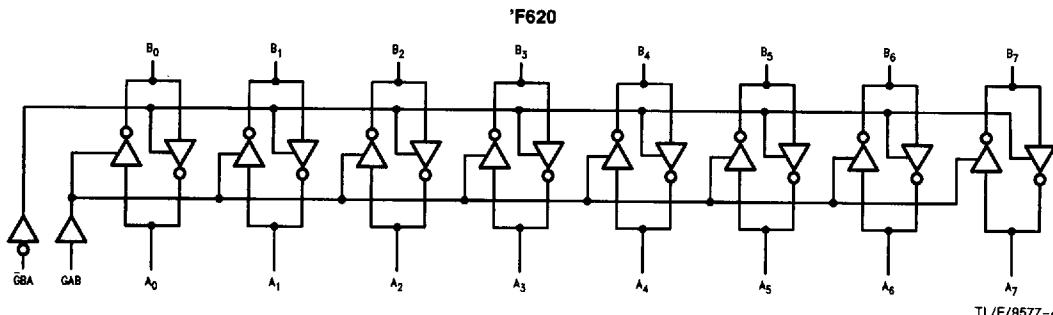
Enable Inputs		Operation	
$\bar{G}BA$	$\bar{G}AB$	'F620	'F623
L	L	\bar{B} Data to A Bus	B Data to A Bus
H	H	\bar{A} Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	\bar{B} Data to A Bus, \bar{A} Data to B Bus	B Data to A Bus, A Data to B Bus

H = HIGH Voltage Level

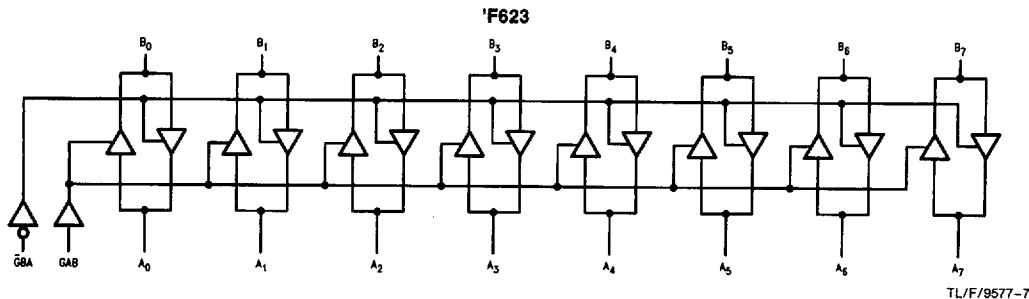
L = LOW Voltage Level

Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias Plastic	-55°C to +175°C -55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	-0.5V to V _{CC}
Standard Output	-0.5V to +5.5V
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output
in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		-1.2		V	Min	I _{IN} = -18 mA (Non I/O Pins)
V _{OH}	Output HIGH Voltage 74F 10% V _{CC}	2.0			V	Min	I _{OH} = -15 mA (A _n , B _n)
V _{OL}	Output LOW Voltage 74F 10% V _{CC}		0.55		V	Min	I _{OL} = 64 mA (A _n , B _n)
I _{IH}	Input HIGH Current 74F		5.0		μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test 74F		7.0		μA	Max	V _{IN} = 7.0V (GBA, GAB)
I _{BVIT}	Input HIGH Current Breakdown (I/O) 74F		0.5		mA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{ICEX}	Output HIGH Leakage Current 74F		50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test 74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current 74F		3.75		μA	0.0	V _{OD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6		mA	Max	V _{IN} = 0.5V (Non I/O Pins)
I _{IH} + I _{OZH}	Output Leakage Current		70		μA	Max	V _{OUT} = 2.7V (A _n , B _n)
I _{IL} + I _{OZL}	Output Leakage Current		-650		μA	Max	V _{OUT} = 0.5V (A _n , B _n)
I _{OS}	Output Short-Circuit Current	-100	-225		mA	Max	V _{OUT} = 0V
I _{IZZ}	Bus Drainage Test		500		μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current ('F620)		82		mA	Max	V _O = HIGH, V _{IN} = 0.2V
I _{CCL}	Power Supply Current ('F620)		82		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F620)		95		mA	Max	V _O = HIGH Z
I _{CCH}	Power Supply Current ('F623)		65		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F623)		82		mA	Max	V _O = LOW, V _{IN} = 0.2V
I _{CCZ}	Power Supply Current ('F623)		85		mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.		
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$					
		Min	Typ	Max	Min	Max				
t_{PLH}	Propagation Delay A Input to B Output ('F620)	2.5	7.5	2.0	8.0		ns	2-3		
t_{PHL}		2.0	7.0	2.0	7.0					
t_{PLH}	Propagation Delay B Input to A Output ('F620)	2.5	7.5	2.0	8.0		ns	2-3		
t_{PHL}		2.0	7.0	2.0	7.0					
t_{PLH}	Propagation Delay A Input to B Output ('F623)	1.5	6.5	1.5	7.5		ns	2-3		
t_{PHL}		2.0	7.0	2.0	7.5					
t_{PLH}	Propagation Delay B Input to A Output ('F623)	1.5	6.5	1.5	7.5		ns	2-3		
t_{PHL}		2.0	7.0	2.0	7.5					
t_{PZH}	Enable Time $\bar{G}BA$ Input to A Output	2.0	7.0	2.0	8.0		ns	2-5		
t_{PLZ}		2.5	8.0	2.0	8.5					
t_{PHZ}	Disable Time $\bar{G}BA$ Input to A Output	1.5	6.5	1.5	7.5		ns	2-5		
t_{PLZ}		1.0	5.5	1.0	5.5					
t_{PZH}	Enable Time GAB Input to B Output ('F620)	2.0	7.5	2.0	8.5		ns	2-5		
t_{PLZ}		3.0	8.0	2.0	8.5					
t_{PHZ}	Disable Time GAB Input to B Output ('F620)	2.5	8.0	2.0	9.0		ns	2-5		
t_{PLZ}		2.0	7.5	2.0	8.0					
t_{PZH}	Enable Time GAB Input to B Output ('F623)	2.0	7.5	2.0	8.5		ns	2-5		
t_{PLZ}		2.5	8.0	2.0	8.5					
t_{PHZ}	Disable Time GAB Input to B Output ('F623)	2.0	8.0	2.0	9.0		ns	2-5		
t_{PLZ}		2.0	8.0	2.0	8.0					