ADVANCE INFORMATION

Am29LV640GH/L

64 Megabit (8 M x 8-Bit/4 M x 16-Bit) CMOS 3.0 Volt-only Uniform Sector Flash Memory with VersatileI/O™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 2.7 to 3.6 volt read, erase, and program operations
- **SecSi™ (Secured Silicon) Sector region**
  - 256-byte sector for permanent, secure identification through an 8-word random Electronic Serial Number
  - May be programmed and locked at the factory or by the customer
  - Accessible through a command sequence
- **VersatileI/O™ control**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
- **Manufactured on 0.17 µm process technology**
- **Flexible sector architecture**
  - One hundred twenty-eight 64 Kbyte sectors
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash standard
- **Package options**
  - 56-pin TSOP
  - 64-ball Fortified BGA
- **Minimum 1 million erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARCTERISTICS

- **High performance**
  - Access time ratings as fast as 70 ns
- **Ultra low power consumption (typical values at 3.0 V, 5 MHz)**
  - 9 mA typical active read current
  - 26 mA typical erase/program current
  - 200 nA typical standby mode current
- **Program and erase performance (V_{HH} not applied to the ACC input pin)**
  - Byte program time: 5 µs typical
  - Word program time: 7 µs typical
  - Sector erase time: 0.6 s typical for each 64 Kbyte sector

SOFTWARE AND HARDWARE FEATURES

- **Hardware features**
  - *Ready/Busy# output (RY/BY#):* indicates program or erase cycle completion
  - *Hardware reset input (RESET#):* resets device for new operation
  - WP# input protects first or last 64 Kbyte sector regardless of sector protection settings
  - *ACC input:* Accelerates programming time for higher throughput during system production
- **Software features**
  - *Program Suspend & Resume:* read other sectors before programming operation is completed
  - *Sector Group Protection:* V_{CC}-level method of preventing program or erase operations within a sector
  - *Temporary Sector Group Unprotect:* V_{ID}-level method of changing in previously locked sectors
  - *CFI (Common Flash Interface) compliant:* allows host system to identify and accommodate multiple flash devices
  - *Erase Suspend/Erase Resume:* read/program other sectors before an erase operation is complete
  - *Data# Polling* and *toggle bits* provide erase and programming operation status
  - *Unlock Bypass Program* command reduces overall multiple-word programming time

Publication# **25293** Rev: **A** Amendment/**1**
Issue Date: **August 28, 2002**

GENERAL DESCRIPTION

The Am29LV640GH/L is a 64 Mbit, 3.0 volt (2.7 V to 3.6 V) single power supply flash memory devices organized as 4,194,304 words or 8,388,608 bytes. Data appears on DQ15–DQ0 in word mode and on DQ7–DQ0 in byte mode. The device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

Access times of 70, 90, and 100 ns are available for applications where $V_{IO} \geq V_{CC}$. Access times of 90 and 100 ns are available for applications where $V_{IO} < V_{CC}$. The device is offered in 56-pin TSOP and 64-ball Fortified BGA packages. To eliminate bus contention each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in 1.8 V or 3 V system environment as required.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The device offers a **standby mode** as a power-saving feature. Once the system places the device into the standby mode power consumption is greatly reduced.

The **SecSi™ (Secured Silicon) Sector** provides an minimum 128-word area for code or data that can be permanently protected. Once this sector is protected, no further programming or erasing within the sector can occur.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP# pin. The protected sector will still be protected even during accelerated programming.

The **accelerated program (ACC)** feature allows the system to program the device at a much faster rate. When ACC is pulled high to V_{HH}, the device enters the Unlock Bypass mode, enabling the user to reduce the time needed to do the program operation. This feature is intended to increase factory throughput during system production, but may also be used in the field if desired.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

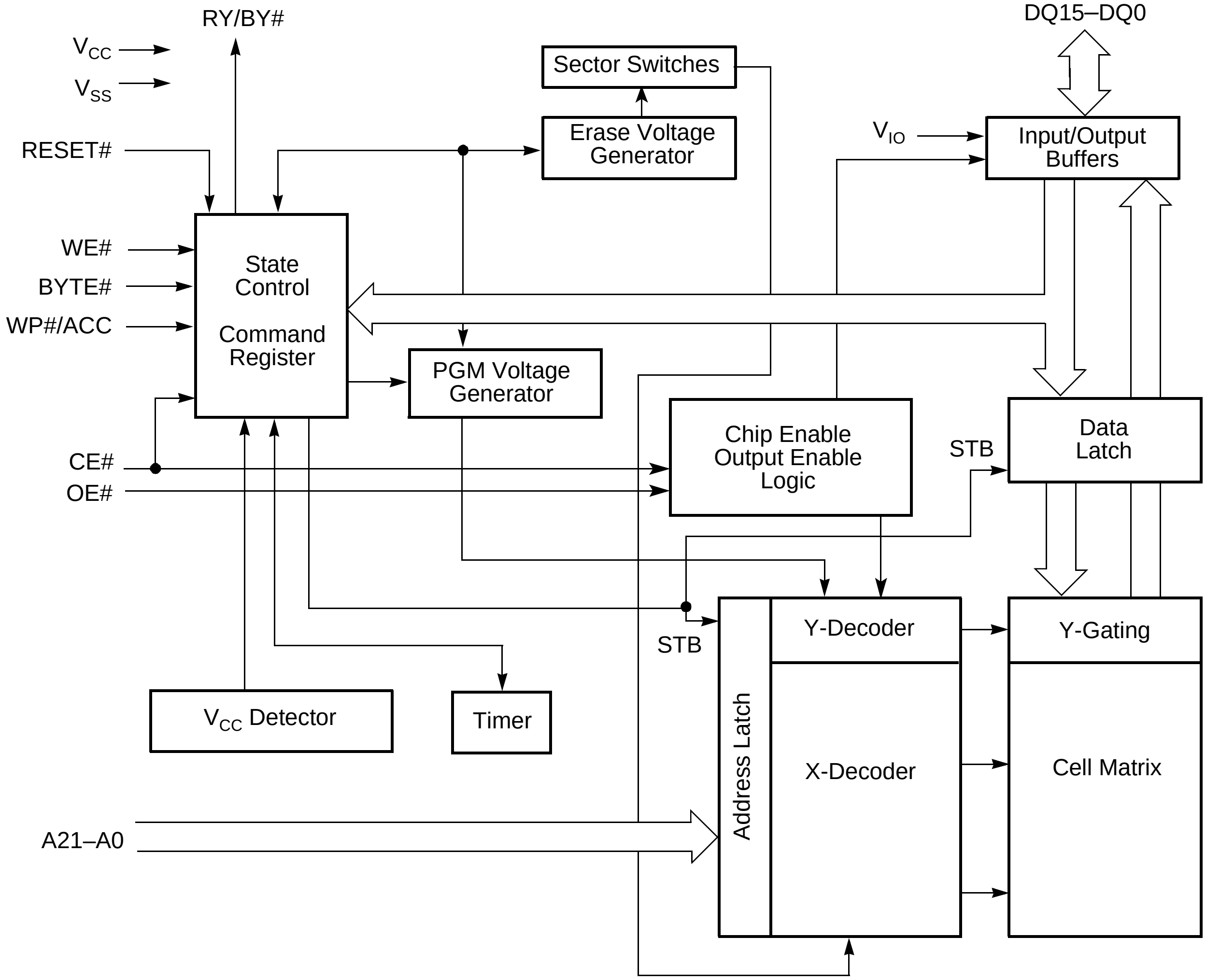
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

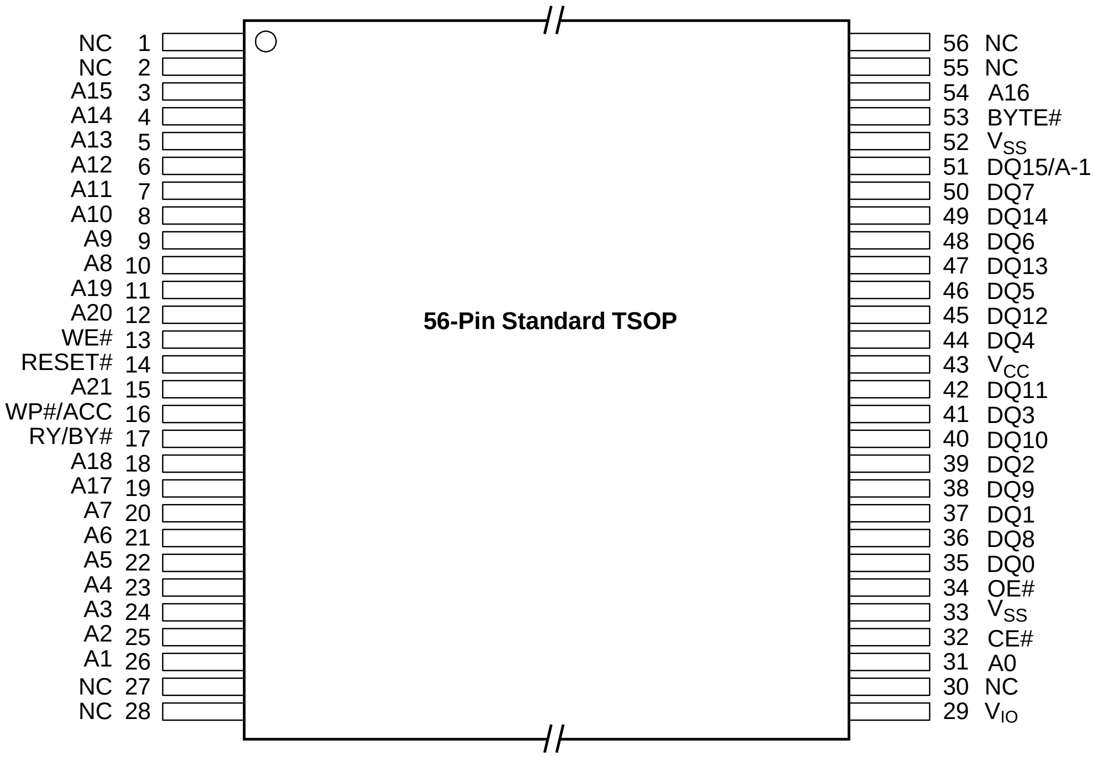
Family Part Number		**Am29LV640GH/L**		
Speed Option	Standard Voltage Range: V_{CC} = 2.7–3.6 V	**70**	**90**	**100**
Max Access Time (ns)		70	90	100
CE# Access (ns)		70	90	100
OE# Access (ns)		35	35	50

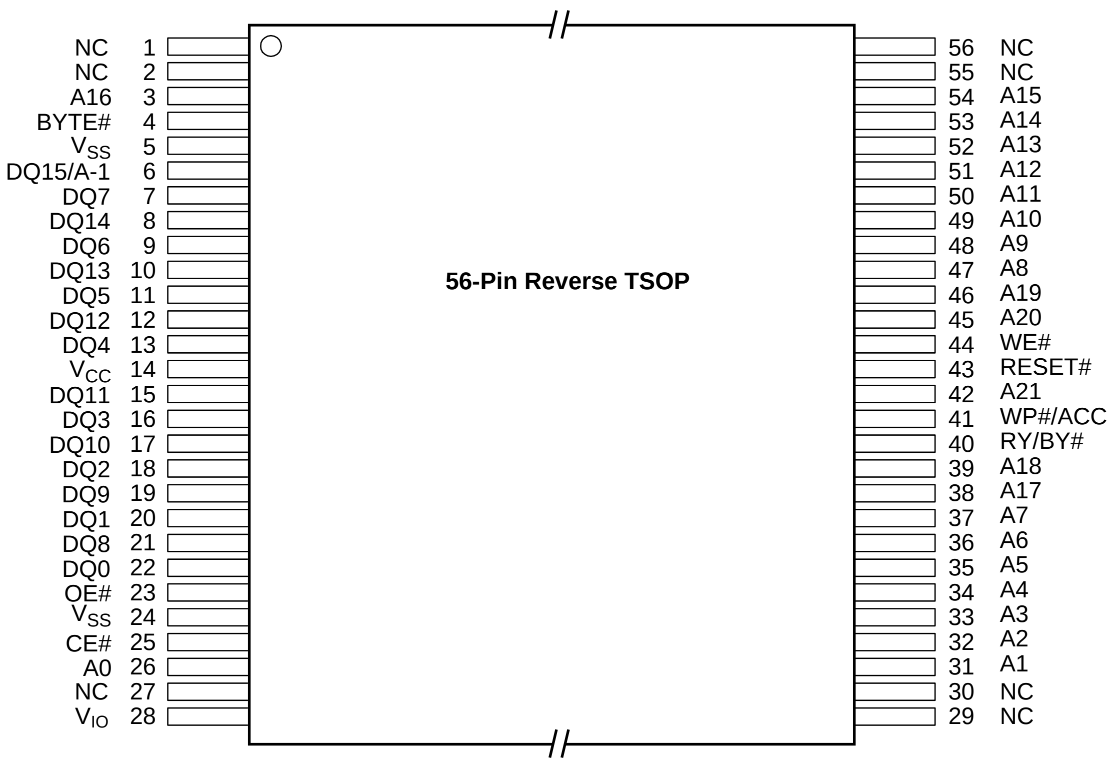
Note: *See “AC Characteristics” for full specifications.*

BLOCK DIAGRAM



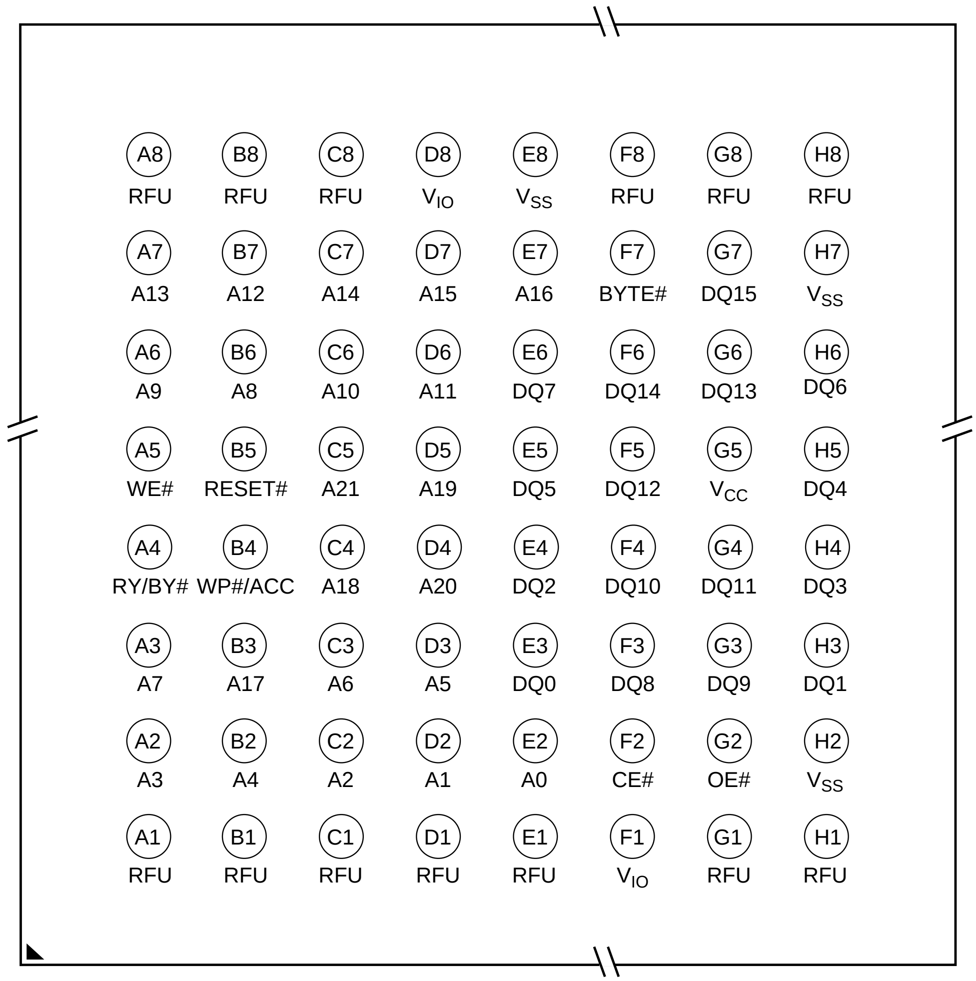
CONNECTION DIAGRAMS





CONNECTION DIAGRAMS

64-Ball Fortified BGA
Top View, Balls Facing Down



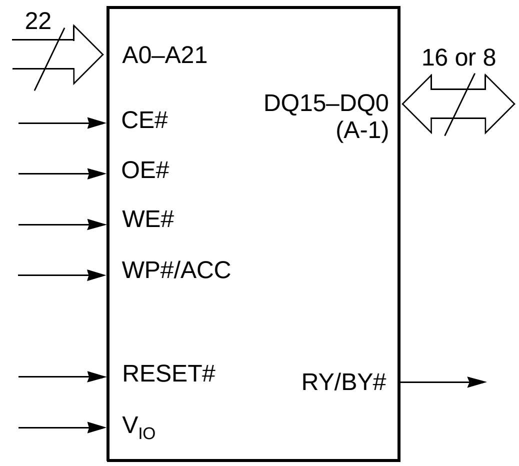
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, SSOP, BGA, PLCC, PDIP). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A21–A0	=	22 Addresses inputs
DQ14–DQ0	=	16 Data inputs/outputs
DQ15/A-1	=	DQ15 data input/output, word mode A-1 LSB address input, byte mode
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input / Acceleration Input
RESET#	=	Hardware Reset Pin input
BYTE#	=	Selects 8-bit or 16-bit mode
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer power
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV640G H 90R E I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
E = 56-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 056)
F = 56-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR056)
PC = 64-Ball Fortified Ball Grid Array (Fortified BGA)
1.0 mm pitch, 13 x 11 mm package (LAA064)

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE AND SECTOR WRITE PROTECTION (WP# = 0)
H = Uniform sector device, highest address sector protected
L = Uniform sector device, lowest address sector protected

DEVICE NUMBER/DESCRIPTION
Am29LV640GH/L
64 Megabit (8 M x 8-Bit / 4 M x 16-Bit) CMOS Uniform Sector Flash Memory with VersatileIO™ Control
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Packages		Speed/V_{IO} Range
AM29LV640GH78R, AM29LV640GL78R	EI, FI	70 ns V_{IO} = 1.65 V – 1.95 V
AM29LV640GH93R, AM29LV640GL93R	EI, FI	90 ns V_{IO} = 2.7 V – 3.6 V
AM29LV640GH98R, AM29LV640GL98R	EI, EE, FI, FE	90 ns, V_{IO} = 1.65 V – 1.95 V
AM29LV640GH103R, AM29LV640GL103R	EI, EE, FI, FE	100 ns V_{IO} = 2.7 V – 3.6 V

Marking Convention

For the Am29xxxxx Enhanced-Vio device, the last digit of the speed indicator specifies Vio range. Speed grades ending in 3 (e.g. 93, 103, etc.) indicate a 3 Volt Vio range; speed grades ending in 8 (e.g. 98, 108, etc.) indicate a 1.8 Volt Vio range.

Valid Combinations for Fortified BGA Packages				Speed/ V_{IO} Range
Order Number		Package Marking		
AM29LV640GH78R, AM29LV640GL78R,	PCI	L640GH78N, L640GL78N	I	70 ns V_{IO} = 1.65 V – 1.95 V
AM29LV640GH93R, AM29LV640GL93R	PCI	L640GH93N, L640GL93N	I	90 ns V_{IO} = 2.7 V – 3.6 V
AM29LV640GH98R, AM29LV640GL98R	PCI, PCE	L640GH98N, L640GL98N	I, E	90 ns, V_{IO} = 1.65 V – 1.95 V
AM29LV640GH103R, AM29LV640GL103R	PCI, PCE	L640GH103N, L640GL103N	I, E	100 ns V_{IO} = 2.7 V – 3.6 V

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 2)	DQ0–DQ7	DQ15–DQ8: BYTE# = V_{IH}	DQ15–DQ8: BYTE# = V_{IL}
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ14–DQ8 = High-Z, DQ15 = A-1
Write	L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	(Note 4)	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	SA, A6 = H, A1 = H, A0 = L	(Note 4)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 8.5– 9.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Addresses are A21:A0 in word mode (BYTE# = V_{IH}), A21:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Unprotection" section.*
3. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector Group Protection and Unprotection". If WP#/ACC = V_{HH}, all sectors will be unprotected.*
4. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.*

VersatileI/O™ (V_{IO}) Control

The VersatileI/O (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in 1.8 V or 3 V system environment 1.65–1.95 volts allows for I/O at the 3 volt level, driving and receiving signals to and from other 3 V devices on the same bus.

Word/Byte Configuration

The DS42615 pin controls whether the device data I/O pins operate in the byte or word configuration. If the i pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ7–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ14–DQ8 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Requirements for Reading Array Data” for more information. Refer to the AC Read-Only Operations table for timing specifications and to Figure 13 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput during system production.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the ACC pin returns the device to normal operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3 V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 14 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2. Sector Address Table

Sector	A21	A20	A19	A18	A17	A16	A15	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	0	000000–00FFFF	000000–007FFF
SA1	0	0	0	0	0	0	1	010000–01FFFF	008000–00FFFF
SA2	0	0	0	0	0	1	0	020000–02FFFF	010000–017FFF
SA3	0	0	0	0	0	1	1	030000–03FFFF	018000–01FFFF
SA4	0	0	0	0	1	0	0	040000–04FFFF	020000–027FFF
SA5	0	0	0	0	1	0	1	050000–05FFFF	028000–02FFFF
SA6	0	0	0	0	1	1	0	060000–06FFFF	030000–037FFF
SA7	0	0	0	0	1	1	1	070000–07FFFF	038000–03FFFF
SA8	0	0	0	1	0	0	0	080000–08FFFF	040000–047FFF
SA9	0	0	0	1	0	0	1	090000–09FFFF	048000–04FFFF
SA10	0	0	0	1	0	1	0	0A0000–0AFFFF	050000–057FFF
SA11	0	0	0	1	0	1	1	0B0000–0BFFFF	058000–05FFFF
SA12	0	0	0	1	1	0	0	0C0000–0CFFFF	060000–067FFF
SA13	0	0	0	1	1	0	1	0D0000–0DFFFF	068000–06FFFF
SA14	0	0	0	1	1	1	0	0E0000–0EFFFF	070000–077FFF
SA15	0	0	0	1	1	1	1	0F0000–0FFFFF	078000–07FFFF
SA16	0	0	1	0	0	0	0	100000–10FFFF	080000–087FFF
SA17	0	0	1	0	0	0	1	110000–11FFFF	088000–08FFFF
SA18	0	0	1	0	0	1	0	120000–12FFFF	090000–097FFF
SA19	0	0	1	0	0	1	1	130000–13FFFF	098000–09FFFF
SA20	0	0	1	0	1	0	0	140000–14FFFF	0A0000–0A7FFF
SA21	0	0	1	0	1	0	1	150000–15FFFF	0A8000–0AFFFF
SA22	0	0	1	0	1	1	0	160000–16FFFF	0B0000–0B7FFF

Table 2. Sector Address Table (Continued)

Sector	A21	A20	A19	A18	A17	A16	A15	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA23	0	0	1	0	1	1	1	170000–17FFFF	0B8000–0BFFFF
SA24	0	0	1	1	0	0	0	180000–18FFFF	0C0000–0C7FFF
SA25	0	0	1	1	0	0	1	190000–19FFFF	0C8000–0CFFFF
SA26	0	0	1	1	0	1	0	1A0000–1AFFFF	0D0000–0D7FFF
SA27	0	0	1	1	0	1	1	1B0000–1BFFFF	0D8000–0DFFFF
SA28	0	0	1	1	1	0	0	1C0000–1CFFFF	0E0000–0E7FFF
SA29	0	0	1	1	1	0	1	1D0000–1DFFFF	0E8000–0EFFFF
SA30	0	0	1	1	1	1	0	1E0000–1EFFFF	0F0000–0F7FFF
SA31	0	0	1	1	1	1	1	1F0000–1FFFFF	0F8000–0FFFFF
SA32	0	1	0	0	0	0	0	200000–20FFFF	100000–107FFF
SA33	0	1	0	0	0	0	1	210000–21FFFF	108000–10FFFF
SA34	0	1	0	0	0	1	0	220000–22FFFF	110000–117FFF
SA35	0	1	0	0	0	1	1	230000–23FFFF	118000–11FFFF
SA36	0	1	0	0	1	0	0	240000–24FFFF	120000–127FFF
SA37	0	1	0	0	1	0	1	250000–25FFFF	128000–12FFFF
SA38	0	1	0	0	1	1	0	260000–26FFFF	130000–137FFF
SA39	0	1	0	0	1	1	1	270000–27FFFF	138000–13FFFF
SA40	0	1	0	1	0	0	0	280000–28FFFF	140000–147FFF
SA41	0	1	0	1	0	0	1	290000–29FFFF	148000–14FFFF
SA42	0	1	0	1	0	1	0	2A0000–2AFFFF	150000–157FFF
SA43	0	1	0	1	0	1	1	2B0000–2BFFFF	158000–15FFFF
SA44	0	1	0	1	1	0	0	2C0000–2CFFFF	160000–167FFF
SA45	0	1	0	1	1	0	1	2D0000–2DFFFF	168000–16FFFF
SA46	0	1	0	1	1	1	0	2E0000–2EFFFF	170000–177FFF
SA47	0	1	0	1	1	1	1	2F0000–2FFFFF	178000–17FFFF
SA48	0	1	1	0	0	0	0	300000–30FFFF	180000–187FFF
SA49	0	1	1	0	0	0	1	310000–31FFFF	188000–18FFFF
SA50	0	1	1	0	0	1	0	320000–32FFFF	190000–197FFF
SA51	0	1	1	0	0	1	1	330000–33FFFF	198000–19FFFF
SA52	0	1	1	0	1	0	0	340000–34FFFF	1A0000–1A7FFF
SA53	0	1	1	0	1	0	1	350000–35FFFF	1A8000–1AFFFF
SA54	0	1	1	0	1	1	0	360000–36FFFF	1B0000–1B7FFF
SA55	0	1	1	0	1	1	1	370000–37FFFF	1B8000–1BFFFF
SA56	0	1	1	1	0	0	0	380000–38FFFF	1C0000–1C7FFF
SA57	0	1	1	1	0	0	1	390000–39FFFF	1C8000–1CFFFF
SA58	0	1	1	1	0	1	0	3A0000–3AFFFF	1D0000–1D7FFF
SA59	0	1	1	1	0	1	1	3B0000–3BFFFF	1D8000–1DFFFF

Table 2. Sector Address Table (Continued)

Sector	A21	A20	A19	A18	A17	A16	A15	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA60	0	1	1	1	1	0	0	3C0000–3CFFFF	1E0000–1E7FFF
SA61	0	1	1	1	1	0	1	3D0000–3DFFFF	1E8000–1EFFFF
SA62	0	1	1	1	1	1	0	3E0000–3EFFFF	1F0000–1F7FFF
SA63	0	1	1	1	1	1	1	3F0000–3FFFFF	1F8000–1FFFFF
SA64	1	0	0	0	0	0	0	400000–40FFFF	200000–207FFF
SA65	1	0	0	0	0	0	1	410000–41FFFF	208000–20FFFF
SA66	1	0	0	0	0	1	0	420000–42FFFF	210000–217FFF
SA67	1	0	0	0	0	1	1	430000–43FFFF	218000–21FFFF
SA68	1	0	0	0	1	0	0	440000–44FFFF	220000–227FFF
SA69	1	0	0	0	1	0	1	450000–45FFFF	228000–22FFFF
SA70	1	0	0	0	1	1	0	460000–46FFFF	230000–237FFF
SA71	1	0	0	0	1	1	1	470000–47FFFF	238000–23FFFF
SA72	1	0	0	1	0	0	0	480000–48FFFF	240000–247FFF
SA73	1	0	0	1	0	0	1	490000–49FFFF	248000–24FFFF
SA74	1	0	0	1	0	1	0	4A0000–4AFFFF	250000–257FFF
SA75	1	0	0	1	0	1	1	4B0000–4BFFFF	258000–25FFFF
SA76	1	0	0	1	1	0	0	4C0000–4CFFFF	260000–267FFF
SA77	1	0	0	1	1	0	1	4D0000–4DFFFF	268000–26FFFF
SA78	1	0	0	1	1	1	0	4E0000–4EFFFF	270000–277FFF
SA79	1	0	0	1	1	1	1	4F0000–4FFFFF	278000–27FFFF
SA80	1	0	1	0	0	0	0	500000–50FFFF	280000–287FFF
SA81	1	0	1	0	0	0	1	510000–51FFFF	288000–28FFFF
SA82	1	0	1	0	0	1	0	520000–52FFFF	290000–297FFF
SA83	1	0	1	0	0	1	1	530000–53FFFF	298000–29FFFF
SA84	1	0	1	0	1	0	0	540000–54FFFF	2A0000–2A7FFF
SA85	1	0	1	0	1	0	1	550000–55FFFF	2A8000–2AFFFF
SA86	1	0	1	0	1	1	0	560000–56FFFF	2B0000–2B7FFF
SA87	1	0	1	0	1	1	1	570000–57FFFF	2B8000–2BFFFF
SA88	1	0	1	1	0	0	0	580000–58FFFF	2C0000–2C7FFF
SA89	1	0	1	1	0	0	1	590000–59FFFF	2C8000–2CFFFF
SA90	1	0	1	1	0	1	0	5A0000–5AFFFF	2D0000–2D7FFF
SA91	1	0	1	1	0	1	1	5B0000–5BFFFF	2D8000–2DFFFF
SA92	1	0	1	1	1	0	0	5C0000–5CFFFF	2E0000–2E7FFF
SA93	1	0	1	1	1	0	1	5D0000–5DFFFF	2E8000–2EFFFF
SA94	1	0	1	1	1	1	0	5E0000–5EFFFF	2F0000–2F7FFF
SA95	1	0	1	1	1	1	1	5F0000–5FFFFF	2F8000–2FFFFF
SA96	1	1	0	0	0	0	0	600000–60FFFF	300000–307FFF

Table 2. Sector Address Table (Continued)

Sector	A21	A20	A19	A18	A17	A16	A15	8-bit Address Range (in hexadecimal)	16-bit Address Range (in hexadecimal)
SA97	1	1	0	0	0	0	1	610000–61FFFF	308000–30FFFF
SA98	1	1	0	0	0	1	0	620000–62FFFF	310000–317FFF
SA99	1	1	0	0	0	1	1	630000–63FFFF	318000–31FFFF
SA100	1	1	0	0	1	0	0	640000–64FFFF	320000–327FFF
SA101	1	1	0	0	1	0	1	650000–65FFFF	328000–32FFFF
SA102	1	1	0	0	1	1	0	660000–66FFFF	330000–337FFF
SA103	1	1	0	0	1	1	1	670000–67FFFF	338000–33FFFF
SA104	1	1	0	1	0	0	0	680000–68FFFF	340000–347FFF
SA105	1	1	0	1	0	0	1	690000–69FFFF	348000–34FFFF
SA106	1	1	0	1	0	1	0	6A0000–6AFFFF	350000–357FFF
SA107	1	1	0	1	0	1	1	6B0000–6BFFFF	358000–35FFFF
SA108	1	1	0	1	1	0	0	6C0000–6CFFFF	360000–367FFF
SA109	1	1	0	1	1	0	1	6D0000–6DFFFF	368000–36FFFF
SA110	1	1	0	1	1	1	0	6E0000–6EFFFF	370000–377FFF
SA111	1	1	0	1	1	1	1	6F0000–6FFFFF	378000–37FFFF
SA112	1	1	1	0	0	0	0	700000–70FFFF	380000–387FFF
SA113	1	1	1	0	0	0	1	710000–71FFFF	388000–38FFFF
SA114	1	1	1	0	0	1	0	720000–72FFFF	390000–397FFF
SA115	1	1	1	0	0	1	1	730000–73FFFF	398000–39FFFF
SA116	1	1	1	0	1	0	0	740000–74FFFF	3A0000–3A7FFF
SA117	1	1	1	0	1	0	1	750000–75FFFF	3A8000–3AFFFF
SA118	1	1	1	0	1	1	0	760000–76FFFF	3B0000–3B7FFF
SA119	1	1	1	0	1	1	1	770000–77FFFF	3B8000–3BFFFF
SA120	1	1	1	1	0	0	0	780000–78FFFF	3C0000–3C7FFF
SA121	1	1	1	1	0	0	1	790000–79FFFF	3C8000–3CFFFF
SA122	1	1	1	1	0	1	0	7A0000–7AFFFF	3D0000–3D7FFF
SA123	1	1	1	1	0	1	1	7B0000–7BFFFF	3D8000–3DFFFF
SA124	1	1	1	1	1	0	0	7C0000–7CFFFF	3E0000–3E7FFF
SA125	1	1	1	1	1	0	1	7D0000–7DFFFF	3E8000–3EFFFF
SA126	1	1	1	1	1	1	0	7E0000–7EFFFF	3F0000–3F7FFF
SA127	1	1	1	1	1	1	1	7F0000–7FFFFF	3F8000–3FFFFF

Note: *All sectors are 64 Kbytes in size.*

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 3. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). Table 3 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10. This method does not require V_{ID}. Refer to the Autoselect Command Sequence section for more information.

Table 3. Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A15	A14 to A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	L	L	L	L	L	L	L	XX01h
Autoselect Device Code	Read Cycle 1	L	L	H	X	X	V_{ID}	X	L	L	L	L	L	L	H	227Eh
	Read Cycle 2	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	L	220Ch
	Read Cycle 3	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	H	XX00h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	01h (protected), 00h (unprotected)
SecSi™ Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	L	L	L	L	H	H	XX98h (factory locked), XX18h (not factory locked)
SecSi™ Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	L	L	L	L	H	H	XX88h (factory locked), XX08h (not factory locked)

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.*

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 4). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

The primary method requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 22367 contains further details; contact an AMD representative to request a copy.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the Autoselect Mode section for details.

Table 4. Sector Group Protection/Unprotection Address Table

Sector Group	A21–A15
SA0	0000000
SA1	0000001
SA2	0000010
SA3	0000011
SA4–SA7	00001XX
SA8–SA11	00010XX
SA12–SA15	00011XX
SA16–SA19	00100XX
SA20–SA23	00101XX
SA24–SA27	00110XX
SA28–SA31	00111XX
SA32–SA35	01000XX
SA36–SA39	01001XX
SA40–SA43	01010XX
SA44–SA47	01011XX
SA48–SA51	01100XX
SA52–SA55	01101XX
SA56–SA59	01110XX
SA60–SA63	01111XX
SA64–SA67	10000XX
SA68–SA71	10001XX
SA72–SA75	10010XX
SA76–SA79	10011XX
SA80–SA83	10100XX
SA84–SA87	10101XX
SA88–SA91	10110XX
SA92–SA95	10111XX
SA96–SA99	11000XX
SA100–SA103	11001XX
SA104–SA107	11010XX
SA108–SA111	11011XX
SA112–SA115	11100XX
SA116–SA119	11101XX
SA120–SA123	11110XX
SA124–SA127	11111XX

Note: *All sector groups are 256 Kbytes in size.*

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the first or last sector without using V_{ID}.

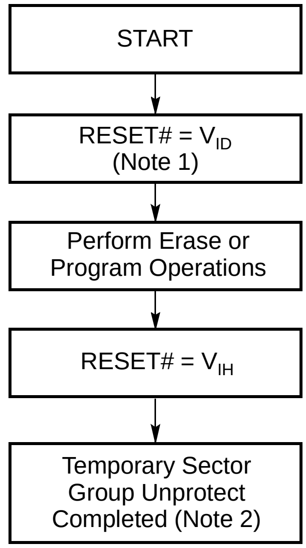
If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected using the method described in "Sector Group Protection and Unprotection". Note that if WP# is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in "DC Characteristics".

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the first or last sector was previously set to be protected or unprotected using the method described in "Sector Group Protection and Unprotection".

Temporary Sector Group Unprotect

(*Note:* *In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 4)).*

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID} (11.5 V – 12.5 V). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected (If WP# = V_{IL}, the first or last sector will remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

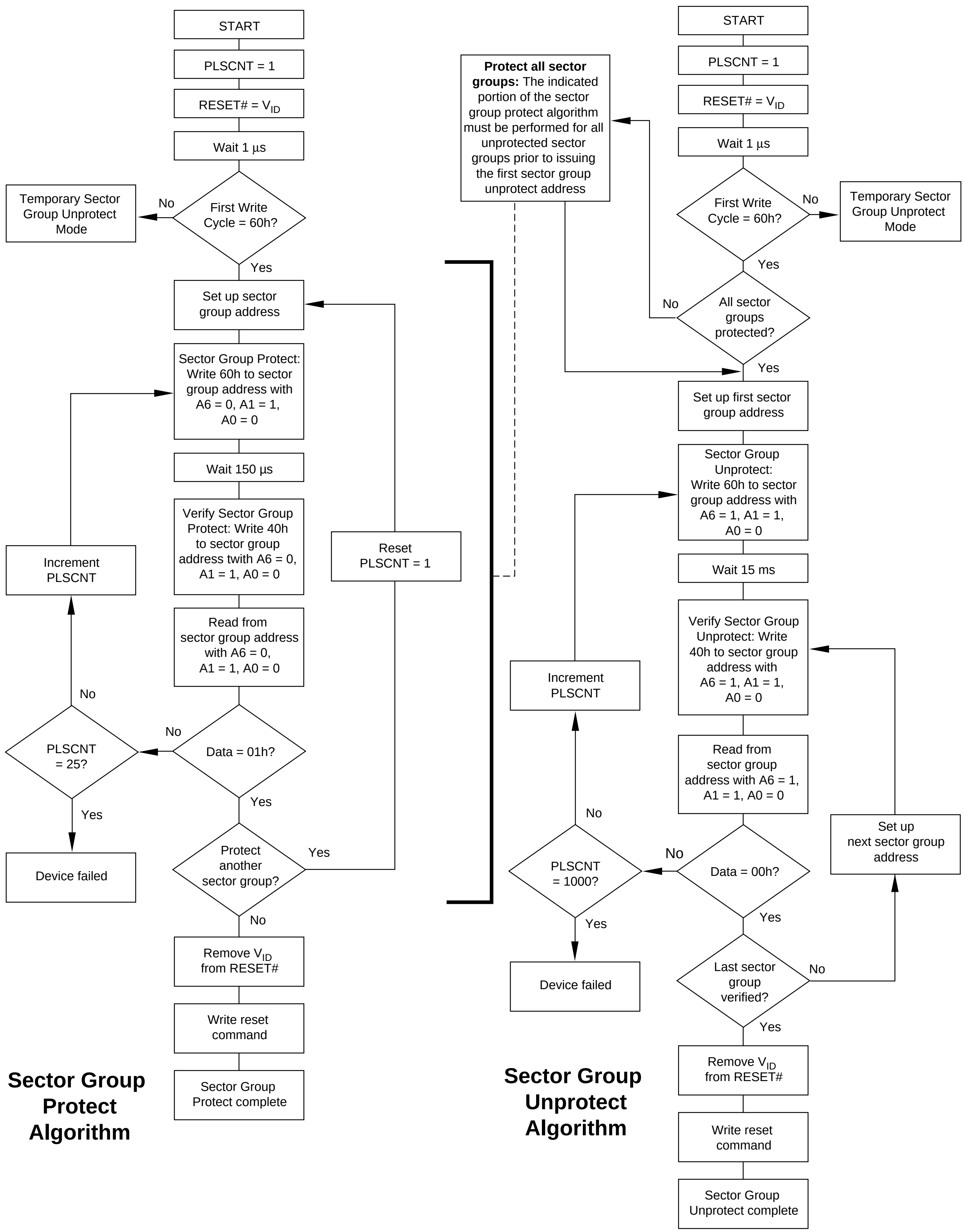


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes or 128 words in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize that sector in any manner they choose. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The SecSi sector address space in this device is allocated as follows:

Table 5. SecSi Sector Contents

SecSi Sector Address Range	Standard Factory Locked	ExpressFlash Factory Locked	Customer Lockable
Uniform Low 000000h–00000Fh (byte mode) 000000h–000007h (word mode)	ESN	ESN or determined by customer	Determined by customer
Uniform High 7FFFF0h–7FFFFFh (byte mode) 3FFFF8h–3FFFFFh (word mode)			
Uniform Low 000010h–0000FFh (byte mode) 000008h–00007Fh (word mode)	Unavailable	Determined by customer	
Uniform High 7FFF00h–7FFFEF (byte mode) 3FFF80h–3FFFF7h (word mode)			

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. A factory locked device has an 16-byte or 8-word random ESN at addresses 000000h–00000Fh or 000000h-000007h.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 256-byte SecSi sector. Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either* V_{IH} *or* V_{ID}. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- Write the three-cycle Enter SecSi Sector Region command sequence, and then use the alternate method of sector protection described in the "Sector Group Protection and Unprotection" section.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 10 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6–9. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6–9. The system must write the reset command to return the device to the reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 6. CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 7. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0002h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 8. Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0017h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0001h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	007Fh 0000h 0000h 0001h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 9. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0004h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 5-2)
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00XXh	Top/Bottom Boot Sector Flag 02h = Bottom Boot Device, 03h = Top Boot Device
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 10 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Figure 13 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 10 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- A read cycle at address XX01h returns the device code.
- A read cycle to an address containing a sector group address (SA), and the address 02h on A7–A0 in word mode returns 01h if the sector group is protected, or 00h if it is unprotected. (Refer to Table 4 for valid sector addresses).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 16-byte random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Table 10 shows the address and data requirements for both command sequences. See also "SecSi™ (Secured Silicon) Sector Flash Memory Region" for further information.

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 10 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a

hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

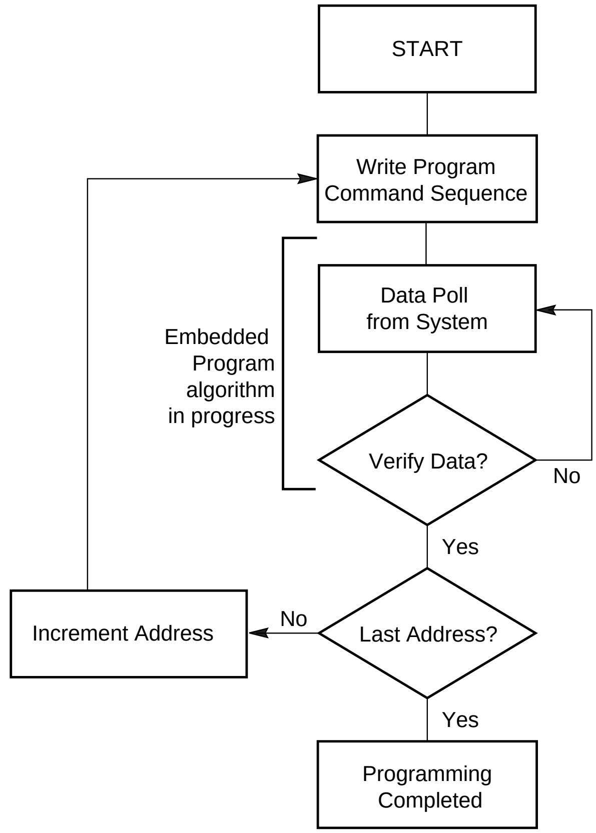
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 10 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

The device offers accelerated program operations through the ACC pin. When the system asserts V_{HH} on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the ACC pin to accelerate the operation. *Note that the ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.*

Figure 3 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Note: *See Table 10 for program command sequence.*

Figure 3. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 10 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 10 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing sector. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 4 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation.

Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

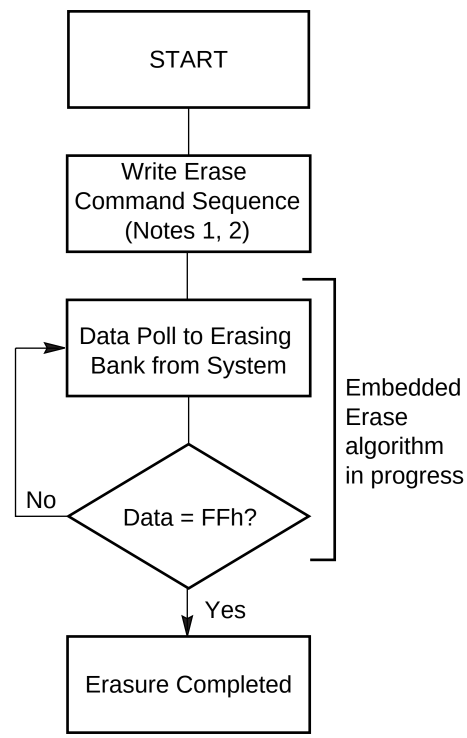
To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Program Suspend/Program Resume Commands

The Program Suspend command, B0h, allows the system to interrupt a programming operation so that data can be read from a non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 1 microsecond and updates the status bits. Addresses are “don’t cares” when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command can also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area, then the user must use the proper command sequences to enter or exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.



Notes:

1. *See Table 10 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Command Definitions

Table 10. Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)		1	RA	RD										
Reset (Note 7)		1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
Autoselect (Note 8)	Device ID	4	555	AA	2AA	55	555	90	X01/ X02	227E	X0E/ X1C	220C	X0F/ X1E	2200
Autoselect (Note 8)	SecSi™ Sector Factory Protect (Note 9)	4	555	AA	2AA	55	555	90	X03	(see Note 9)				
Autoselect (Note 8)	Sector Group Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	XX00/ XX01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 11)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 12)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend (Note 13)		1	BA	B0										
Erase Resume/Program Suspend (Note 14)		1	BA	30										
CFI Query (Note 15)		1	55	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A21–A15 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A21–A15 are don't cares.*
6. *No unlock or command cycles required when device is in read mode.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
9. *If WP# protects the highest address sector, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the lowest address sector, the data is 88h for factory locked and 08h for not factor locked.*
10. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
12. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
13. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation. The Program Suspend is also valid during Erase Suspend.*
14. *The Erase Resume and Program Resume commands are valid only during the Erase Suspend and Program Suspend modes.*
15. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
16. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

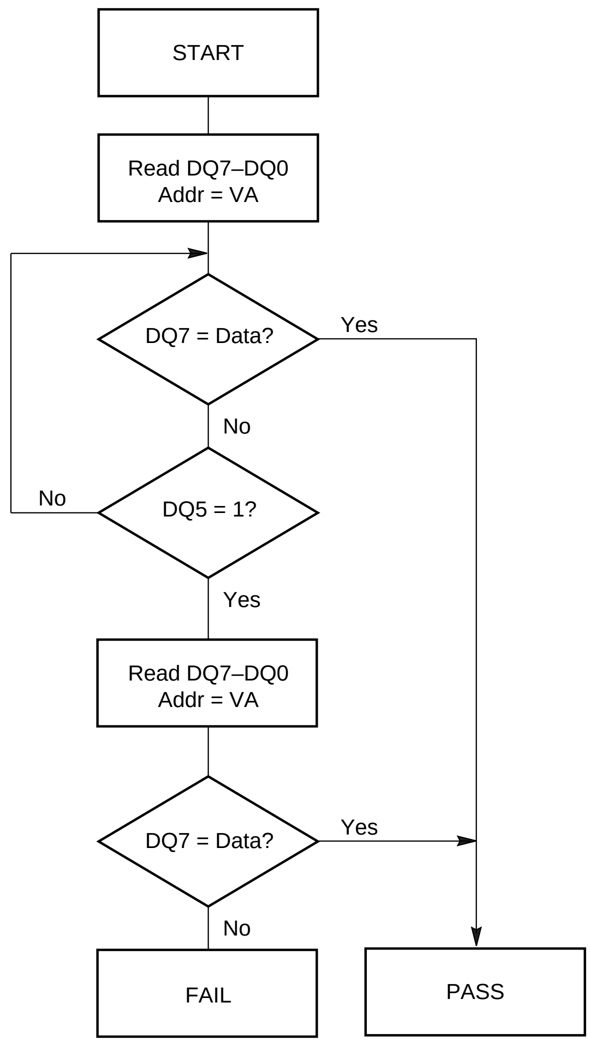
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6–DQ0 may be still invalid. Valid data on DQ7–DQ0 will appear on successive read cycles.

Table 11 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 5. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or the device is in the erase-suspend-read mode.

Table 11 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

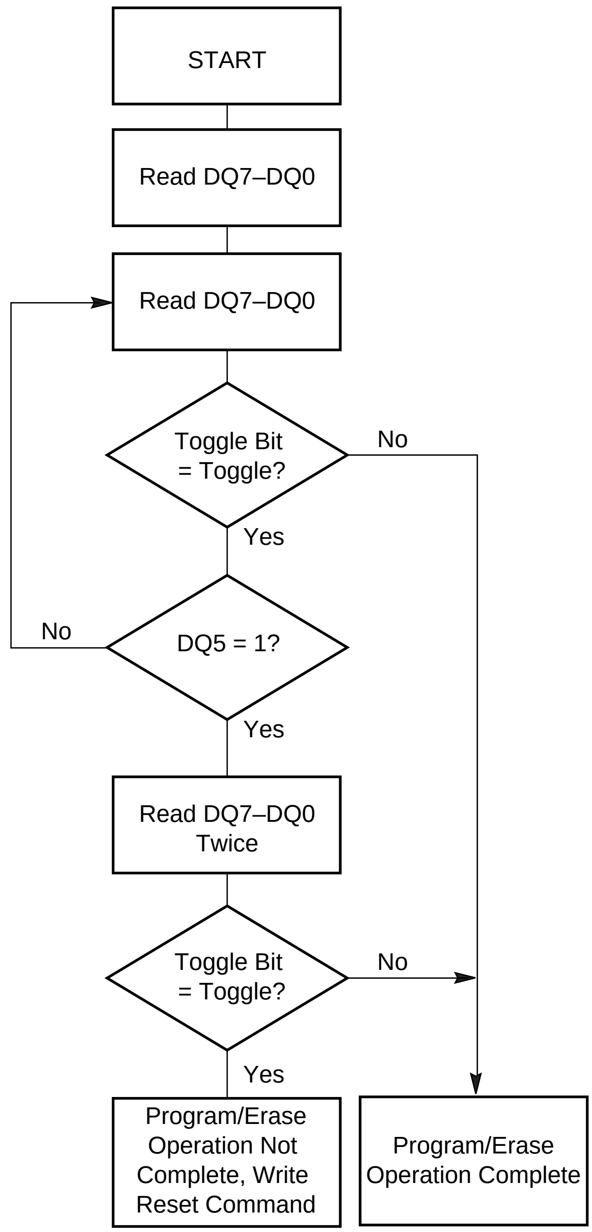
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11 shows the outputs for Toggle Bit I on DQ6. Figure 6 shows the toggle bit algorithm. Figure 21 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 6. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 to compare outputs for DQ2 and DQ6.

Figure 6 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 6).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11 shows the status of DQ3 relative to the other status bits.

Table 11. Write Operation Status

<table>
<tr><th colspan="3">Status</th><th>DQ7
(Note 2)</th><th>DQ6</th><th>DQ5
(Note 1)</th><th>DQ3</th><th>DQ2
(Note 2)</th><th>RY/BY#</th></tr>
<tr><td rowspan="2">Standard Mode</td><td colspan="2">Embedded Program Algorithm</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>No toggle</td><td>0</td></tr>
<tr><td colspan="2">Embedded Erase Algorithm</td><td>0</td><td>Toggle</td><td>0</td><td>1</td><td>Toggle</td><td>0</td></tr>
<tr><td rowspan="2">Program Suspend Mode</td><td rowspan="2">Program-Suspend-Read</td><td>Program-Suspended Sector</td><td>Not Allowed</td><td>Not Allowed</td><td>Not Allowed</td><td>Not Allowed</td><td>Not Allowed</td><td>1</td></tr>
<tr><td>Non-Program Suspended Sector</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>1</td></tr>
<tr><td rowspan="3">Erase Suspend Mode</td><td rowspan="2">Erase-Suspend-Read</td><td>Erase Suspended Sector</td><td>1</td><td>No toggle</td><td>0</td><td>N/A</td><td>Toggle</td><td>1</td></tr>
<tr><td>Non-Erase Suspended Sector</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>Data</td><td>1</td></tr>
<tr><td colspan="2">Erase-Suspend-Program</td><td>DQ7#</td><td>Toggle</td><td>0</td><td>N/A</td><td>N/A</td><td>0</td></tr>
</table>

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *Data are invalid for addresses in a Program Suspended Sector.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . .–0.5 V to +4.0 V

V_{IO} . . . .–0.5 V to +5.5 V

WP#/ACC . . . .–0.5 V to +9.5 V

A9, OE#, and RESET#
(Note 2). . . . .–0.5 V to +12.5 V

All other pins (Note 1) . . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 7. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.*
2. *Minimum DC input voltage on pins A9, OE#, RESET#, and WP#/ACC is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP# is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

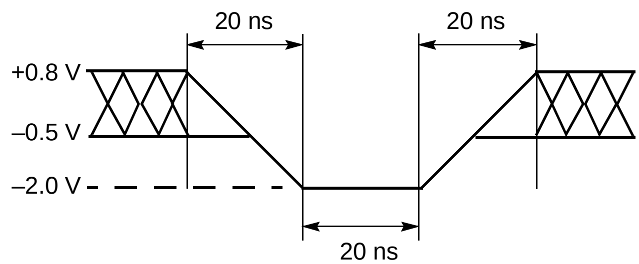


Figure 7. Maximum Negative Overshoot Waveform

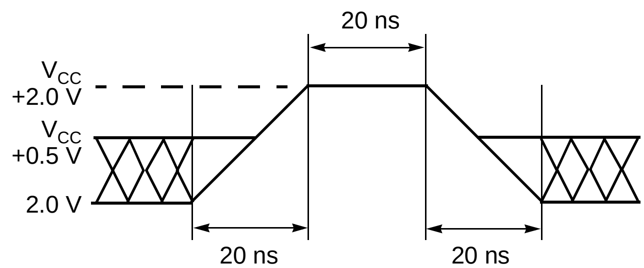


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for all devices . . . . .2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

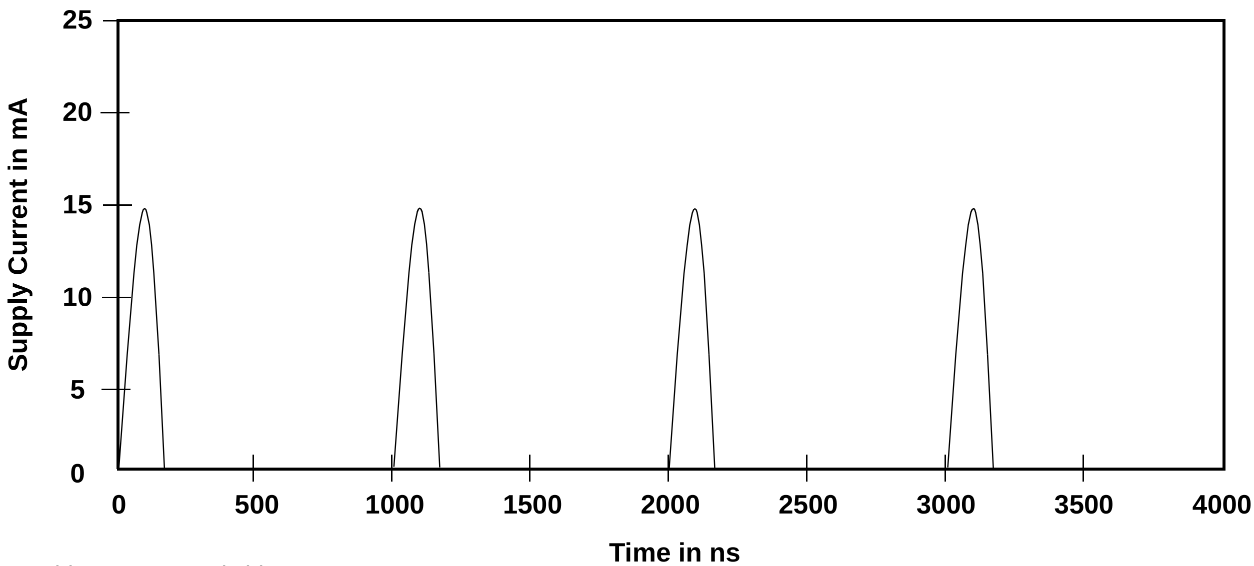
Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (Note 1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, OE#, RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; V_{ID} = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 2, 3)	CE# = $V_{IL,}$ OE# = V_{IH}	5 MHz		9	16	mA
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 3, 4)	CE# = $V_{IL,}$ OE# = V_{IH}, WE# = V_{IL}			15	26	mA
I_{CC3}	V_{CC} Standby Current (Note 3)	CE#, RESET# = V_{CC} ± 0.3 V, WP# = V_{IH}			0.2	5	µA
I_{CC4}	V_{CC} Reset Current (Note 3)	RESET# = V_{SS} ± 0.3 V, WP# = V_{IH}			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Notes 3, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V, WP# = V_{IH}			0.2	5	µA
V_{IL}	Input Low Voltage (Note 6)			–0.5		0.8	V
V_{IH}	Input High Voltage (Note 6)			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{HH}	Voltage for ACC Program Acceleration	V_{CC} = 3.0 V ± 10%		8.5		9.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.0 V ± 10%		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage (Note 7)	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 x V_{IO}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{IO}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 7)			2.3		2.5	V

Notes:

1. *On the WP# pin only, the maximum input load current when WP# = V_{IL} is ± 5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
6. *If $V_{IO} < V_{CC}$, maximum V_{IL} for CE# is 0.3 x V_{IO}. If $V_{IO} < V_{CC}$, minimum V_{IH} for CE# is 0.3 x V_{IO}.*
7. *Not 100% tested.*

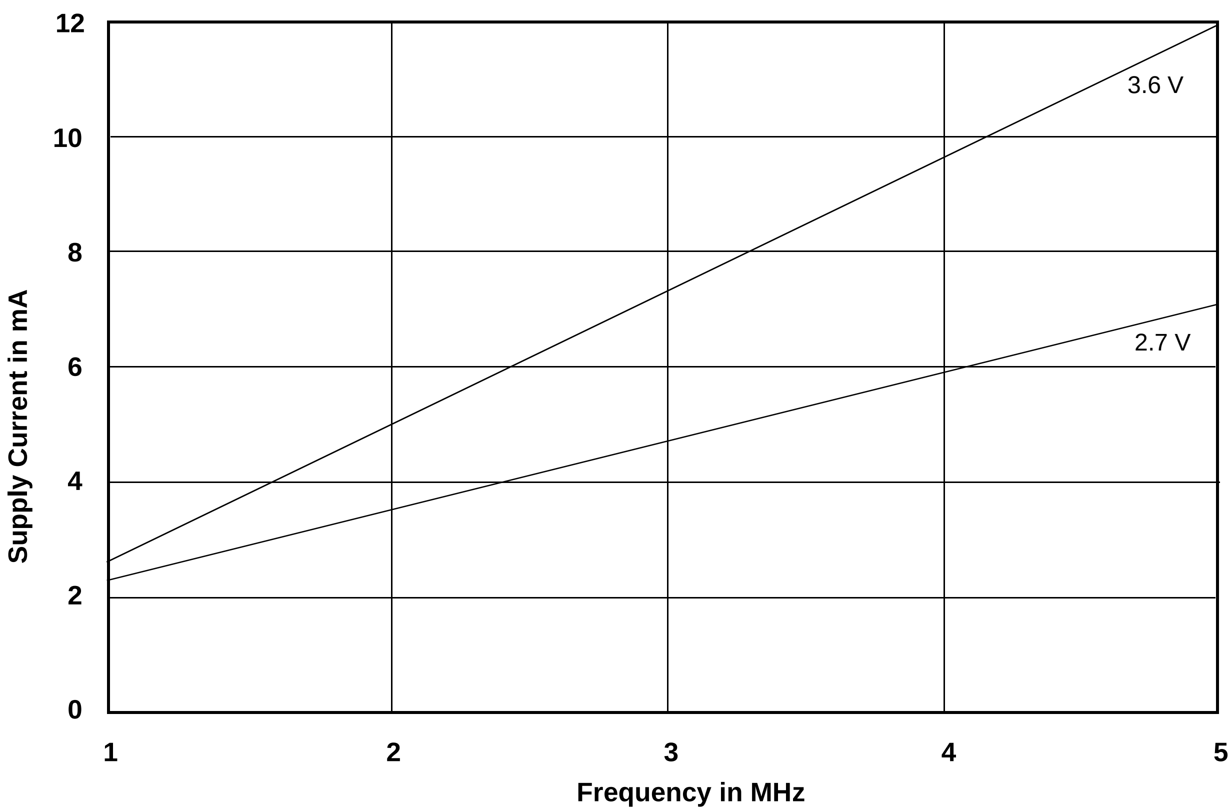
DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

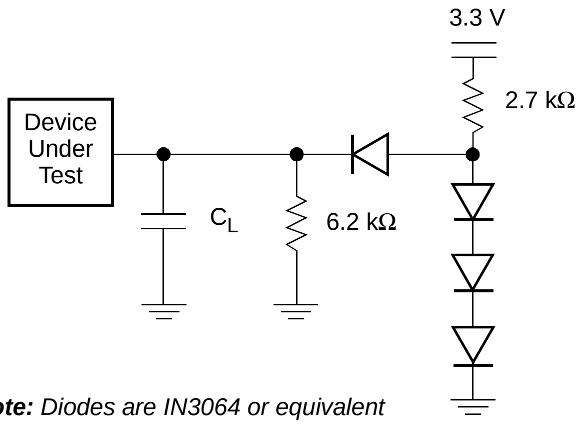
Figure 9. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 10. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



***Note:** Diodes are IN3064 or equivalent*

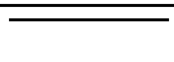
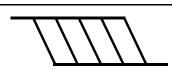
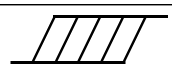
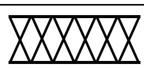
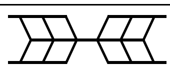
Figure 11. Test Setup

Table 12. Test Specifications

Test Condition	70	90R, 100R	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels (See Note)	1.5		V
Output timing measurement reference levels	0.5 V_{IO}		V

***Note:** If V_{IO} < V_{CC}, the reference level is 0.5 V_{IO}.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

***Note:** If V_{IO} < V_{CC}, the input measurement reference level is 0.5 V_{IO}.*

Figure 12. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read-Only Operations

Parameter						Speed Options			
JEDEC	Std.	Description		Test Setup		70	90R	100R	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	70	90	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	70	90	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	90	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	35	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	16			ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	16			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns

Notes:

1. Not 100% tested.

2. See Figure 11 and Table 12 for test specifications.

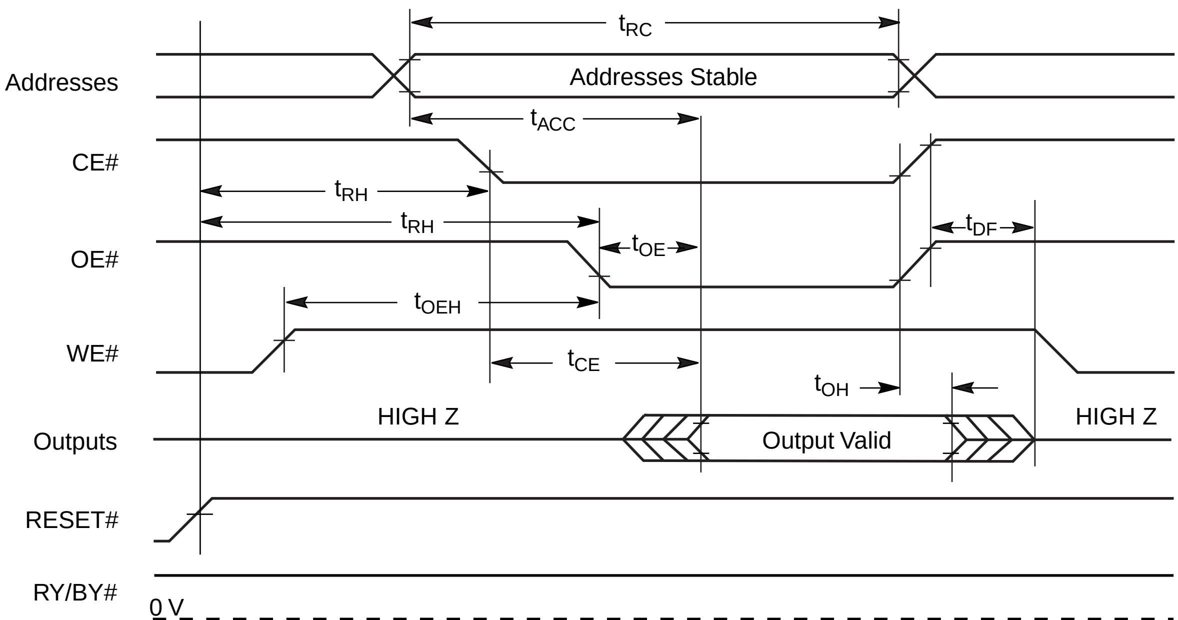


Figure 13. Read Operation Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

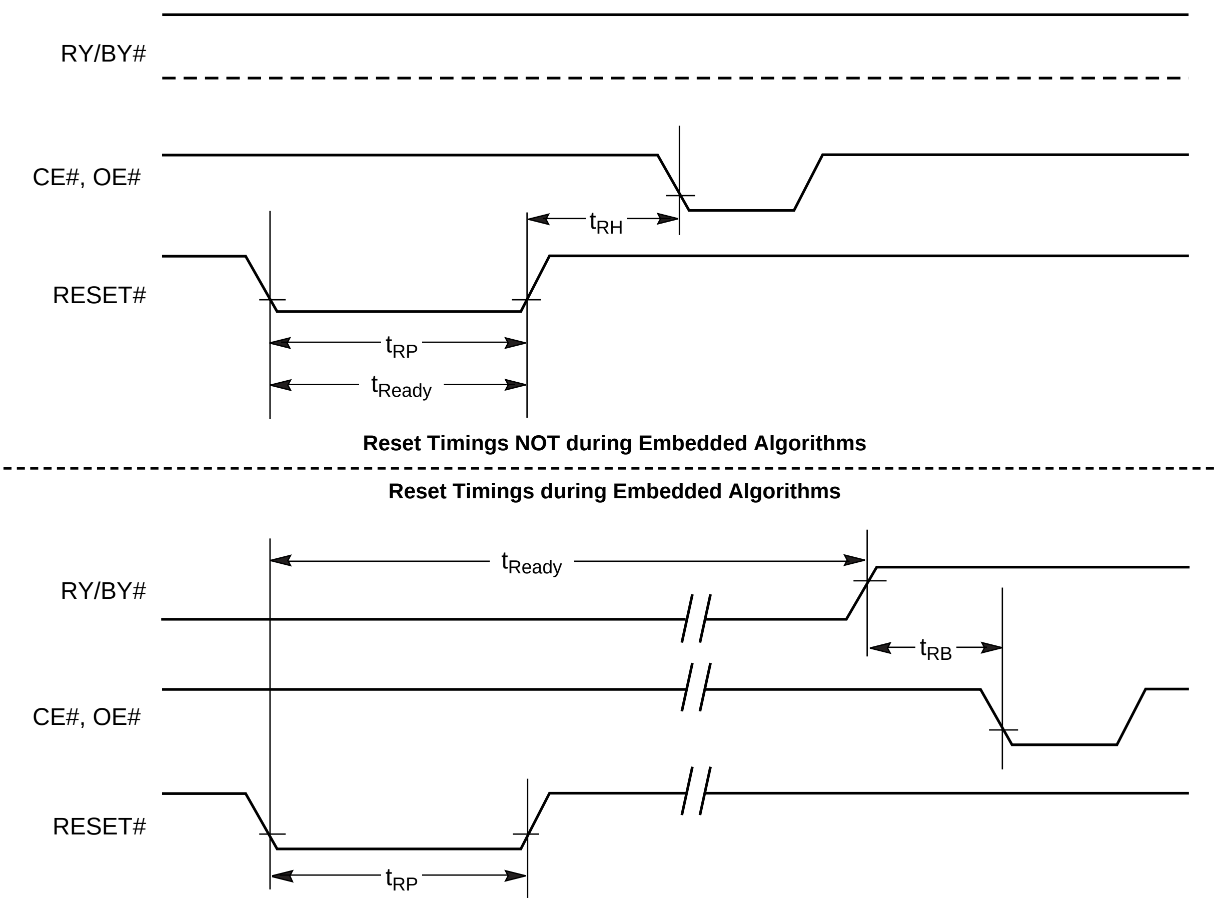


Figure 14. Reset Timings

CHARACTERISTICS

Word/Byte Configuration (BYTE#)

Parameter		Description		Speed Options			Unit
JEDEC	Std.			70	90	100	
	t_{ELFL}/t_{ELFH}	CE# to BYTE# Switching Low or High	Max	5			ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	16			ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	70	90	100	ns

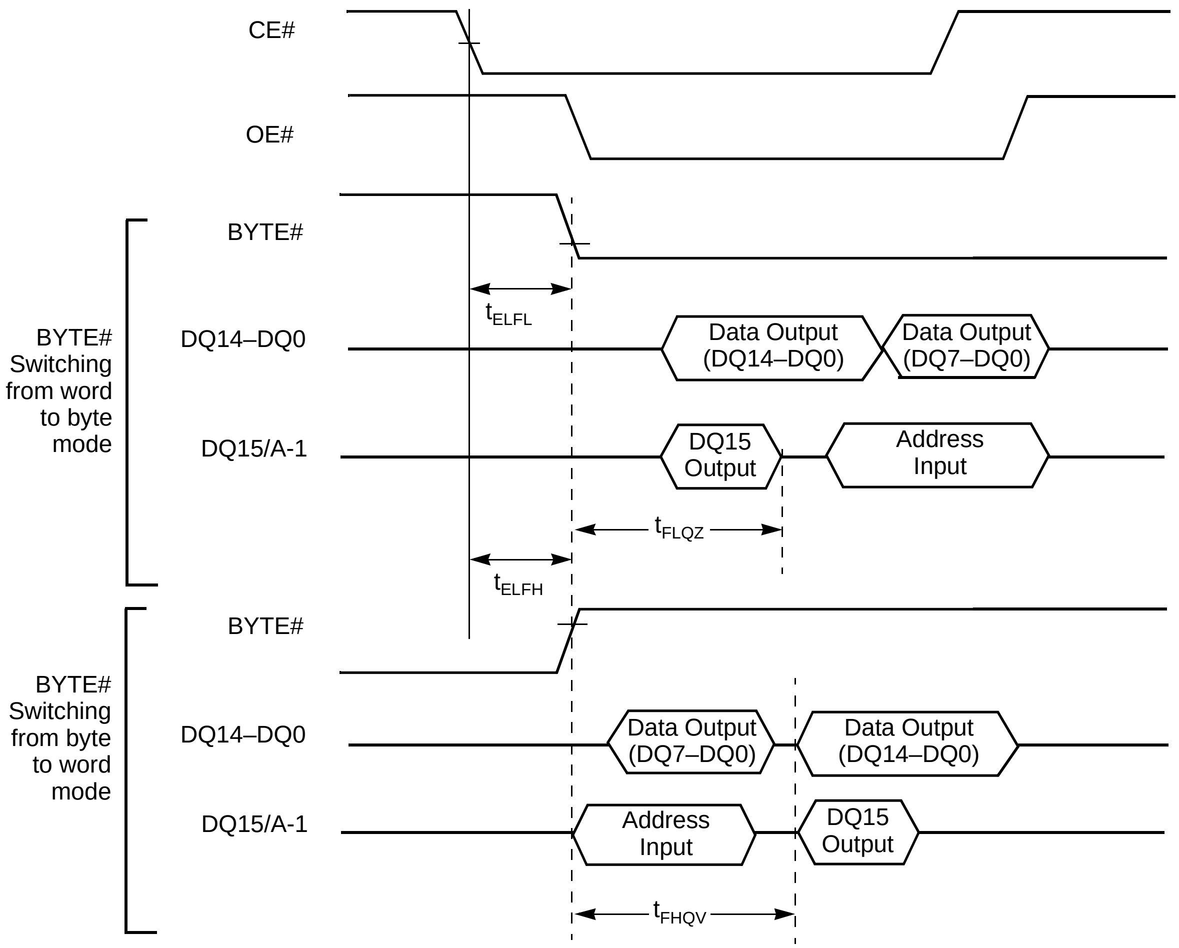
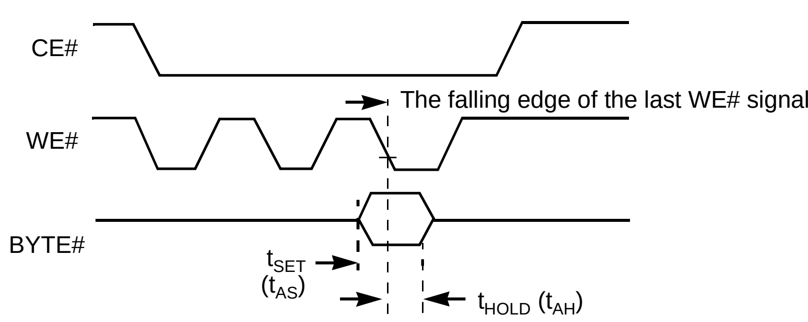


Figure 15. BYTE# Timings for Read Operations



Note: *Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.*

Figure 16. BYTE# Timings for Write Operations

AC CHARACTERISTICS

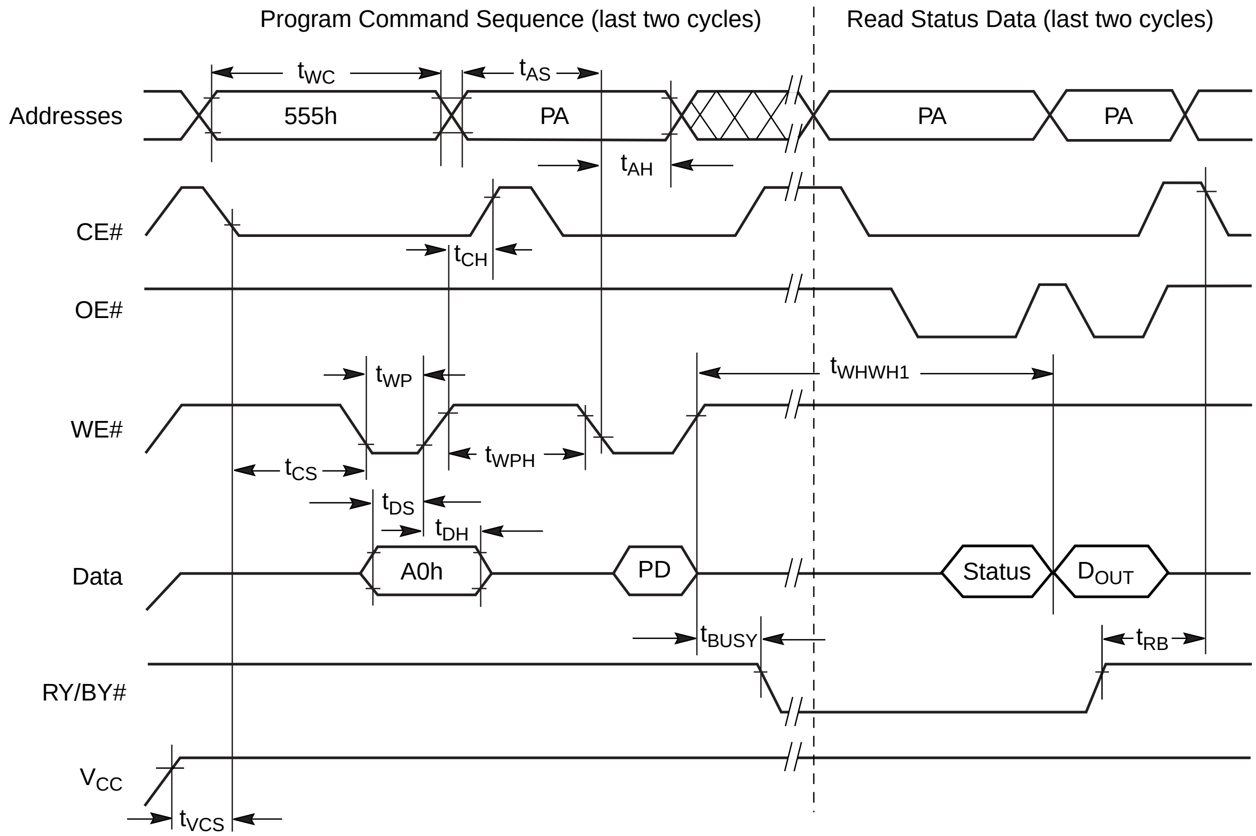
Erase and Program Operations

Parameter				Speed Options			
JEDEC	Std.	Description		70	90R	100R	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	70	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling	Min	15			ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	50	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0			ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0			ns
	t_{OEPH}	Output Enable High during toggle bit polling	Min	20			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0			ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High	Min	25	30		ns
t_{WHWH1}	t_{WHWH1}	Word Programming Operation (Note 2)	Typ	7			µs
t_{WHWH1}	t_{WHWH1}	Accelerated Word Programming Operation (Note 2)	Typ	4			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.4			sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)	Min	250			ns
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50			µs
	t_{RB}	Write Recovery Time from RY/BY#	Min	0			ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90			ns

Notes:

1. *Not 100% tested.*
2. *See the “Erase And Programming Performance” section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

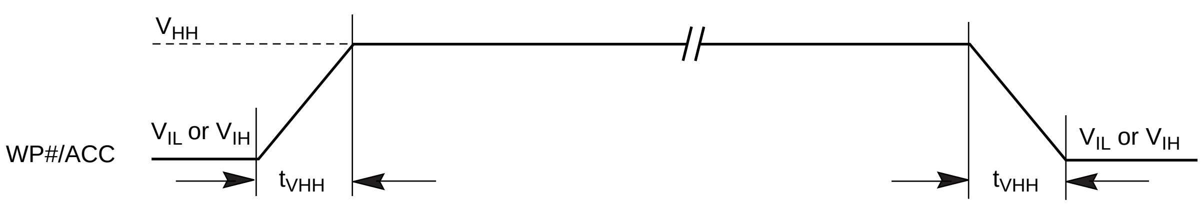
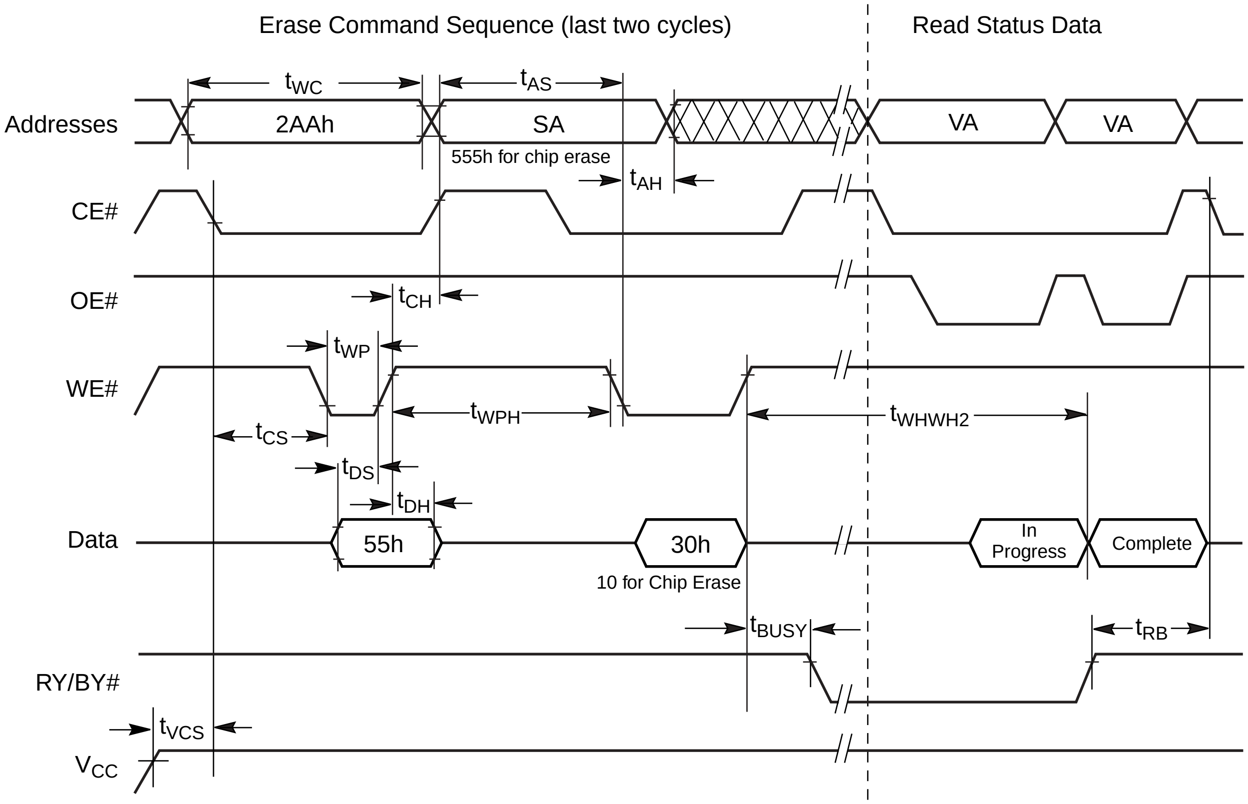


Figure 18. Accelerated Program Timing Diagram

AC CHARACTERISTICS

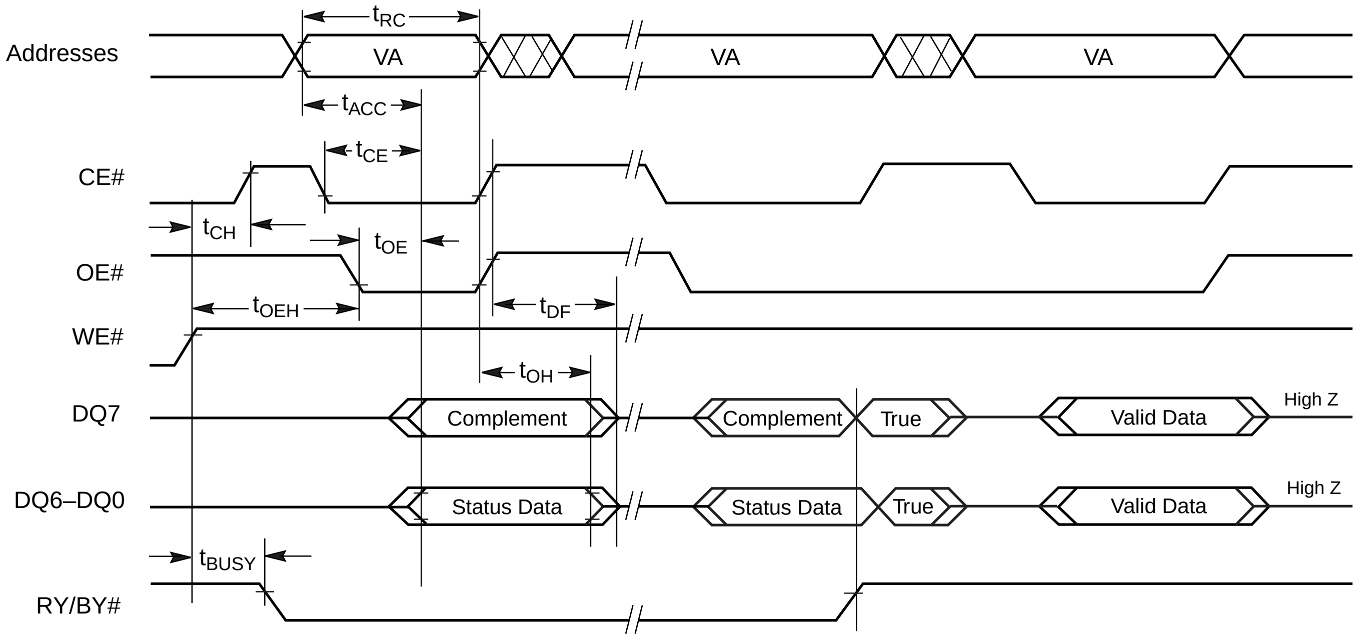


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see “Write Operation Status”.*
2. *These waveforms are for the word mode.*

Figure 19. Chip/Sector Erase Operation Timings

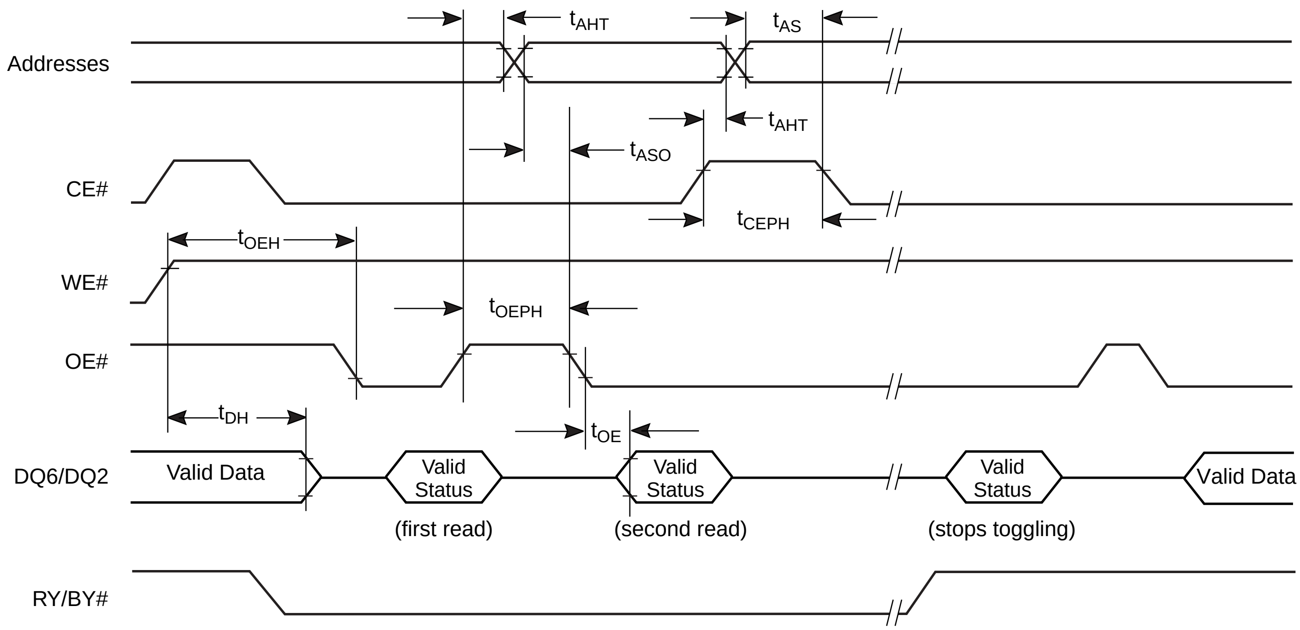
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

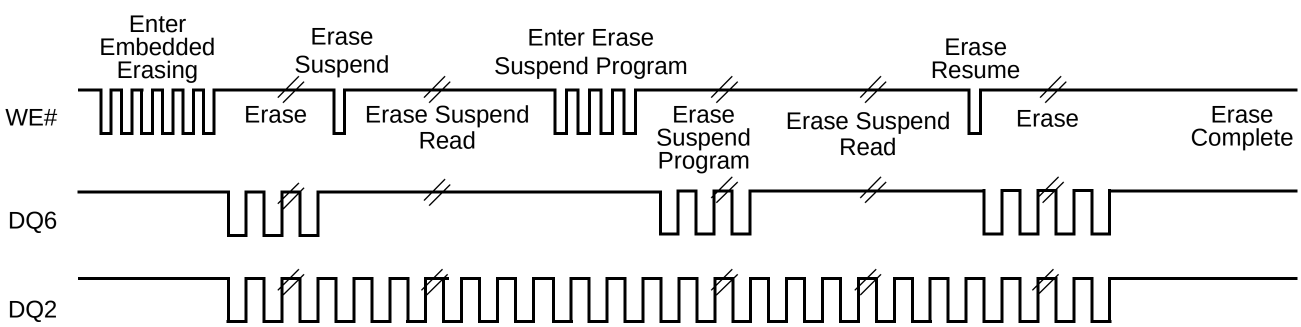
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotect	Min	4	µs

Note: *Not 100% tested.*

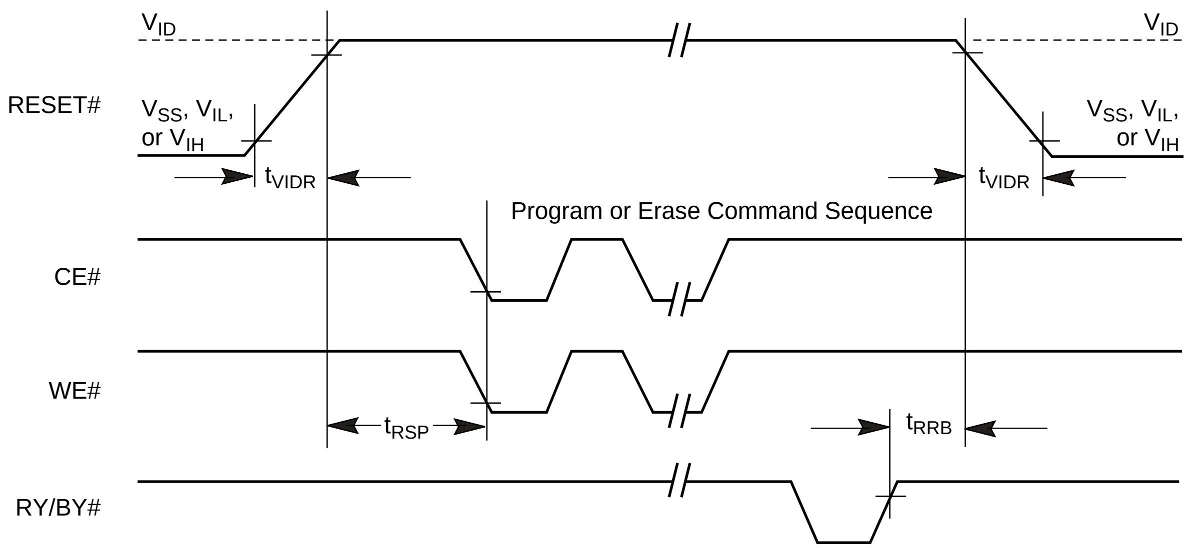
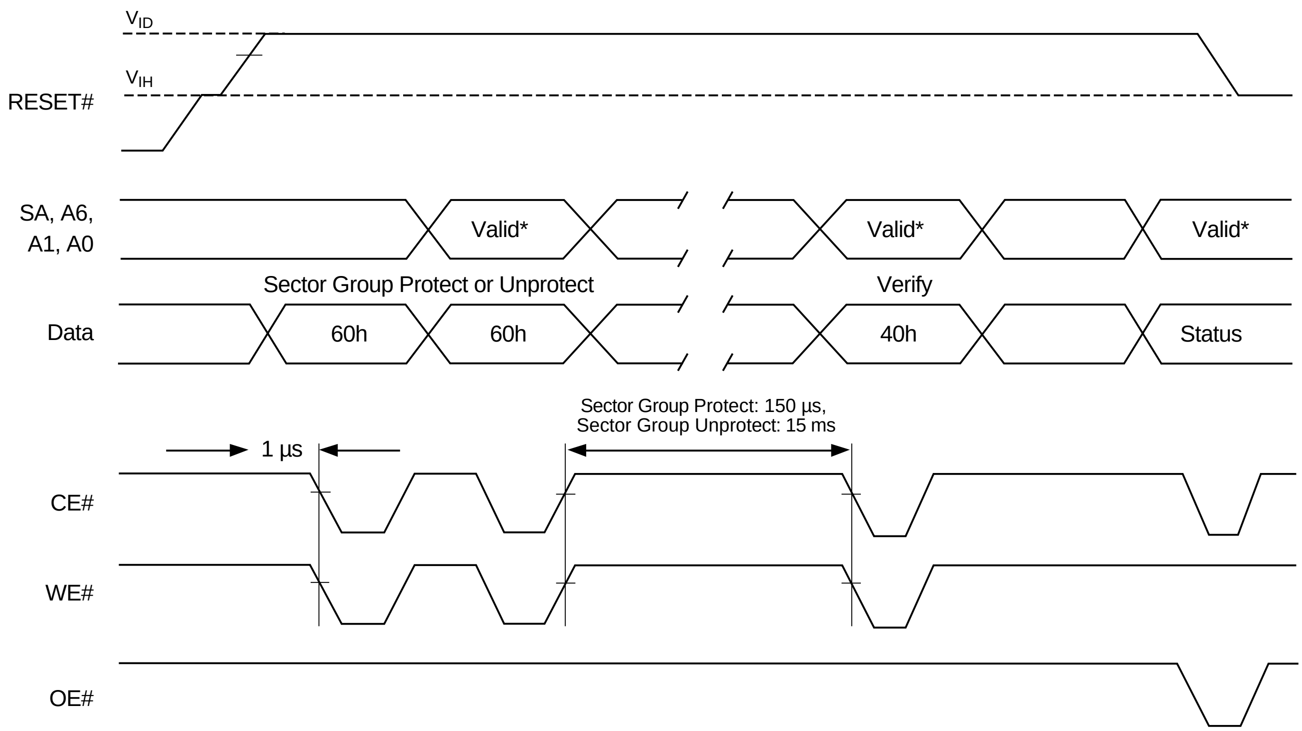


Figure 23. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector group protect, A6 = 0, A1 = 1, A0 = 0. For sector group unprotect, A6 = 1, A1 = 1, A0 = 0.*

Figure 24. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

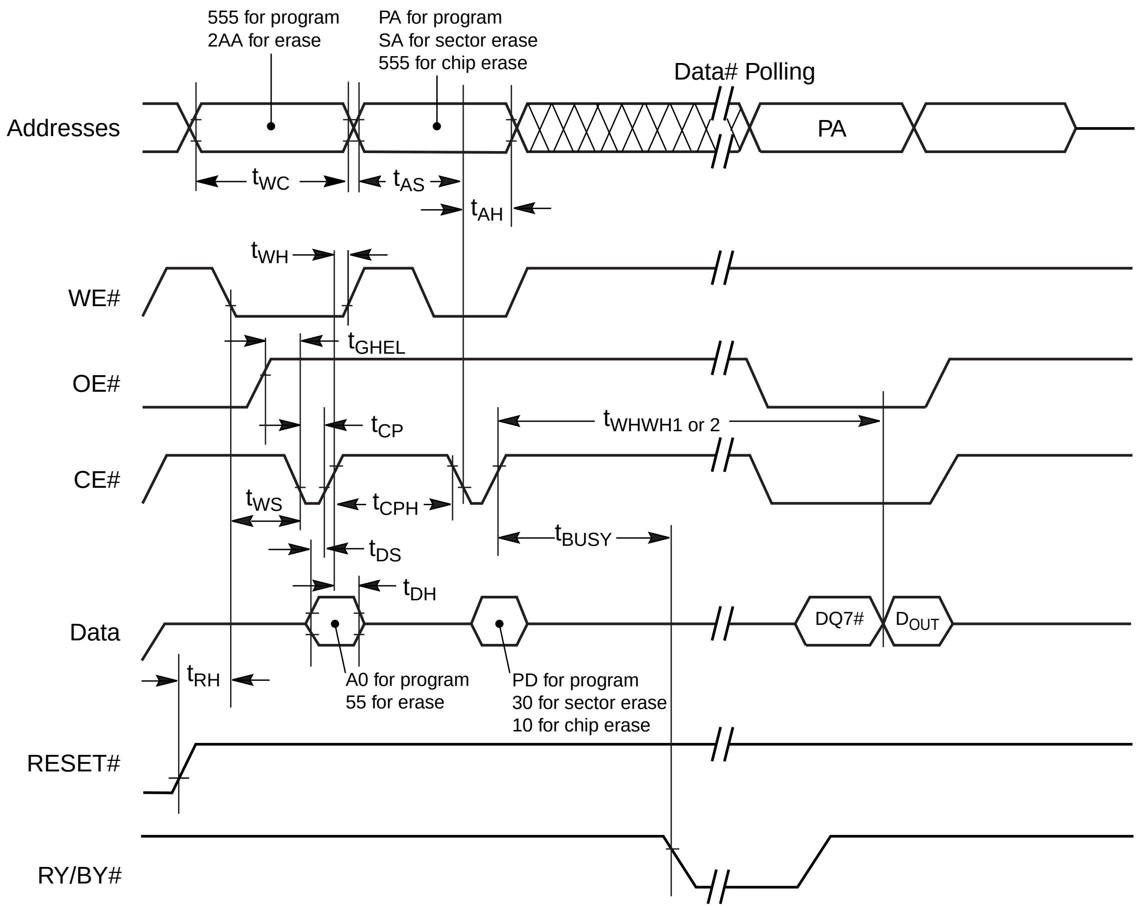
Alternate CE# Controlled Erase and Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std				70	90R	100R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70	90	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	40	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	40	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	40	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	5			µs
			Word		7			µs
t_{WHWH1}	t_{WHWH1}	Accelerated Word Programming Operation (Note 2)		Typ	4			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.6			sec

Notes:

1. *Not 100% tested.*
2. *See the “Erase And Programming Performance” section for more information.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.6	4	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		50		sec	
Program Time	Byte	5	150	µs	Excludes system level overhead (Note 5)
	Word	7	210	µs	
Accelerated Word Program Time		4	120	µs	
Chip Program Time (Note 3)	Byte	42	54	sec	
	Word	29.4	36	sec	

Notes:
1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 3.0 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most words program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 10 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

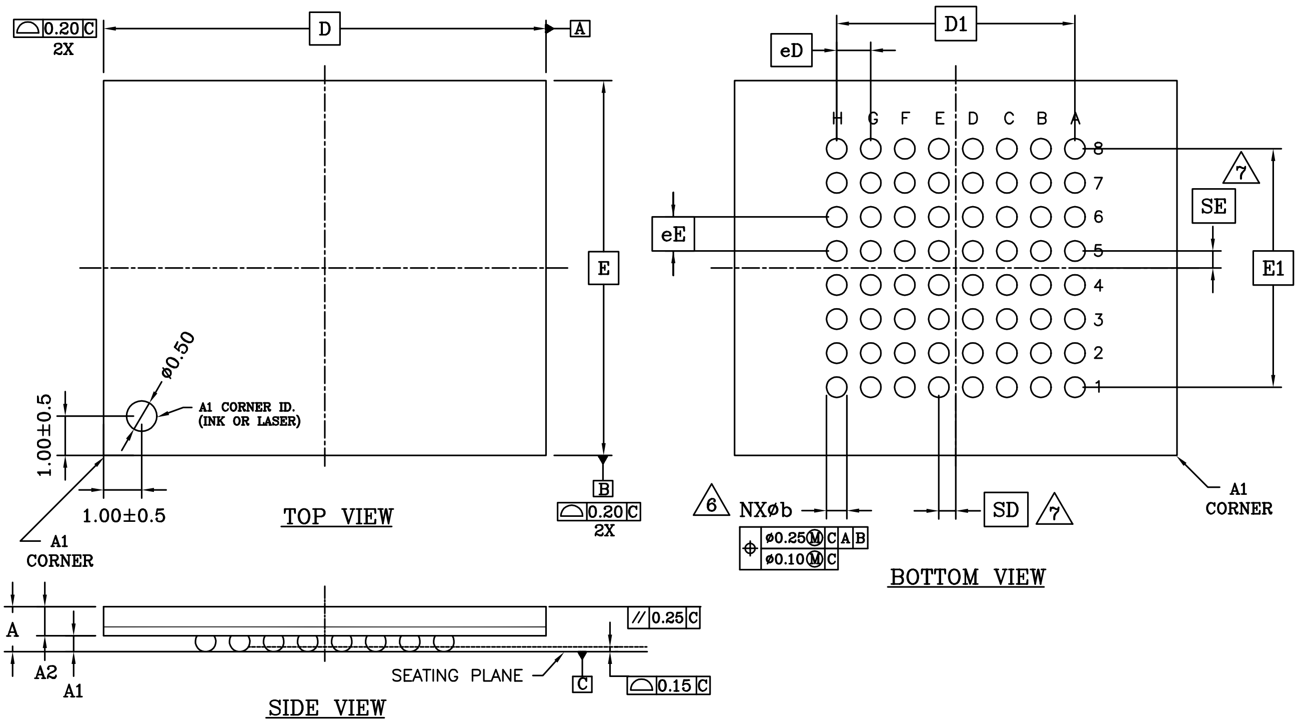
Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

LAA064—64-Ball Fortified Ball Grid Array (Fortified BGA) 13 x 11 mm package



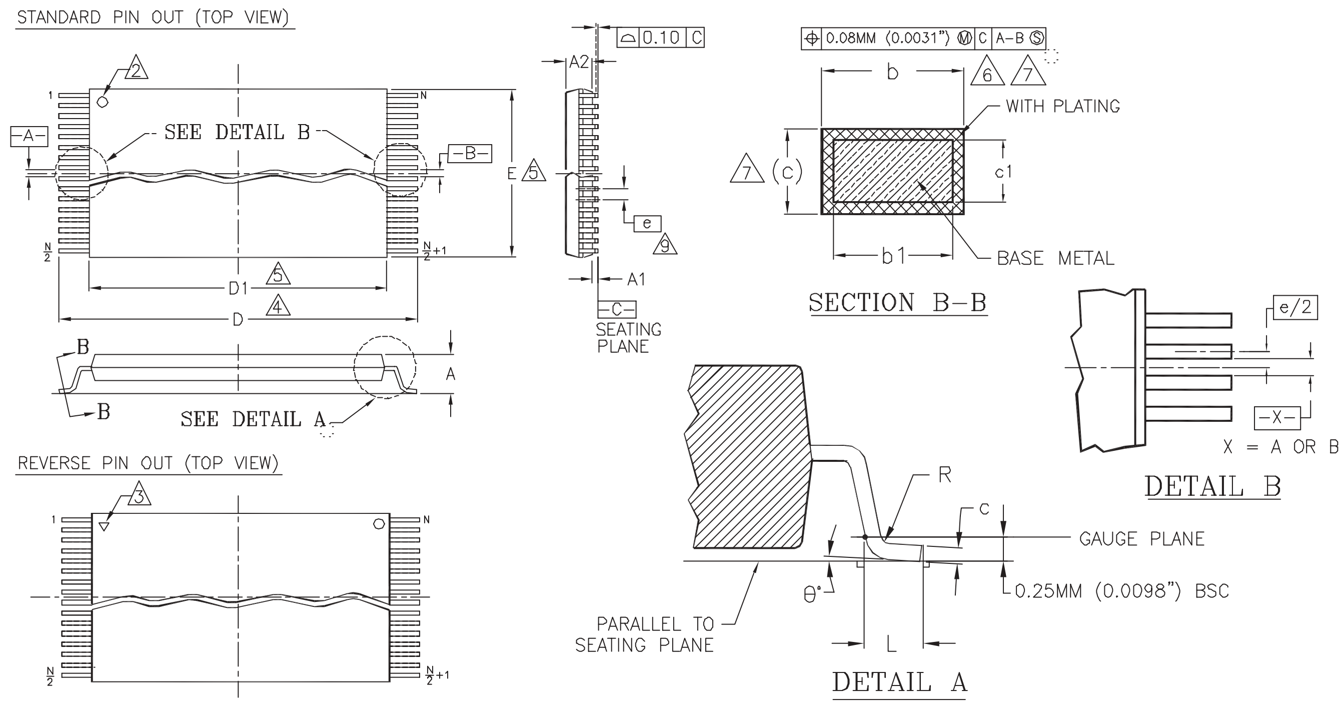
PACKAGE	[redacted] 064			NOTE
JEDEC	N/A			
	13.00mm X 11.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	[redacted]	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	1.00	---	---	BODY THICKNESS
D	13.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	7.00 BSC			MATRIX FOOTPRINT
E1	7.00 BSC			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	64			BALL COUNT
Øb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC			BALL PITCH – D DIRECTION
eE	1.00 BSC			BALL PITCH – E DIRECTION
SD/SE	0.50 BSC			SOLDER BALL PLACEMENT
				DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.

PHYSICAL DIMENSIONS

TS 056/TSR056—56-Pin Standard/Reverse Thin Small Outline Package (TSOP)



PACKAGE	TS/TSR 56		
JEDEC	MO-142 (B) EC		
SYMBOL	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.90	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
Ø	0°	3°	5°
R	0.08	---	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15 mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF b DIMENSION AT MAX MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 mm.
7. THESE DIMESIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

3160\38.10A

Note: *For reference only. BSC is an ANSI standard for Basic Space Centering.*

REVISION SUMMARY

Revison A (August 9, 2002)

Initial Release.

Revision A + 1 (August 28, 2002)

Ordering Information

Corrected order numbers and package markings.

Added Marking Convention explanation about Enhanced-Vio markings.