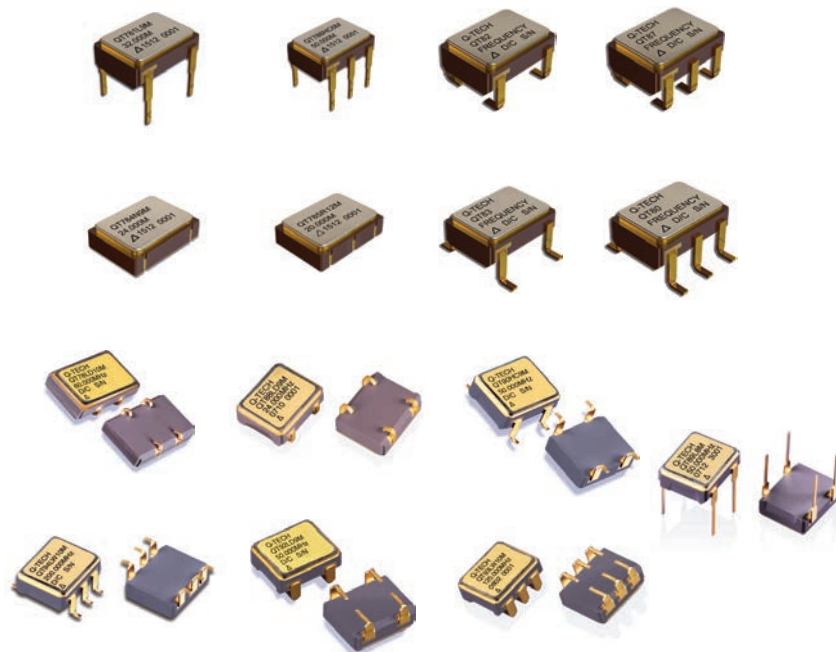


Description

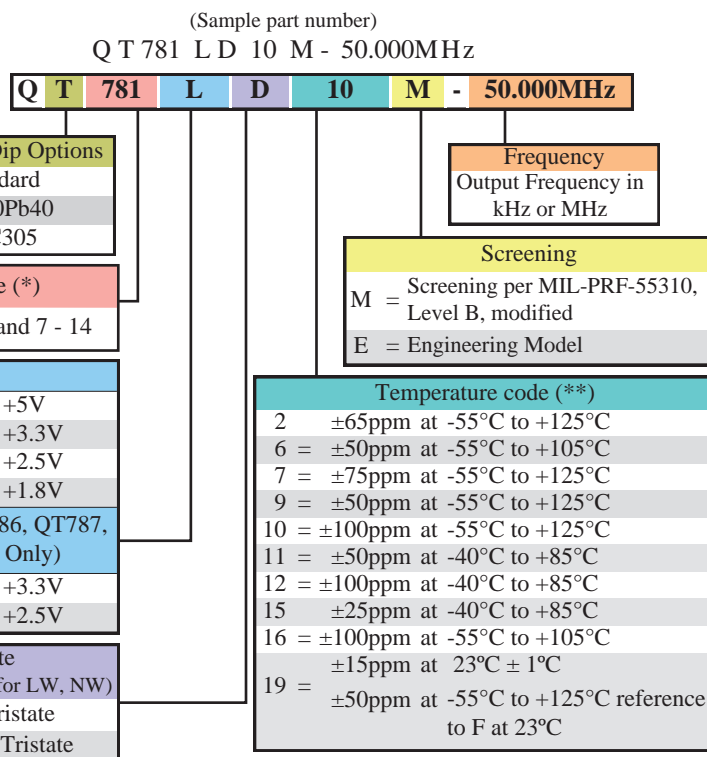
Q-Tech's low profile extreme high shock hybrid oscillators consist of an IC operating at various supply voltages from 1.8V, 2.5V, 3.3V, and 5.0Vdc and a miniature strip quartz crystal. The series is offered in various ceramic package configurations from true Surface-Mount SMT to straight leads and formed leads. This is the smallest package offered with a 50kRad(Si) TID for Low Earth Orbit (LEO) with high shock and high reliability space applications.



Features

- Made in the USA
- ECCN: EAR99
- 50kRad(Si) Total Dose Ionization
- Broad Frequency Range, 230kHz to 162.5MHz
- Small Footprint
- CMOS, LVHCMOS, LVDS
- Various Supply Voltages, 1.8Vdc to 5.0Vdc
- Wide Operating Temperature Range, -55°C to 125°C
- Tri-State Output (Option D)
- Hermetically sealed package
- Fundamental and 3rd Overtone Designs
- Screening per MIL-PRF-55310, Level B, with PIND
- High Shock Resistant Tested Up to 20,000g Mechanical Shock, Half-Sine, 0.3ms, All Axes
- Tape and Reel Packaging is available for an additional cost (for SMD parts).
- Optional Hot Solder Dip, Sn60Pb40 or SAC305
- RoHS Compliant

Ordering Information


















Applications

- Commercial satellites
- Low Earth Orbit

(*) See package outlines for sizes (Pages 7 - 14)

(**) Frequency stability vs. temperature codes may not be available in all frequencies.

PRODUCT OFFERINGS

Photo	Product QT	Package	Output Logic	Vdd (V)	Frequency Range	Outline	Pin Connection
	QT781	5x7mm 4 Pin Thru-hole	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	7	
	QT786	5x7mm 6 Pin Thru-hole	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT784	5x7mm Surface Mount (SMD) 4 Pad SMT	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	8	
	QT785	5x7mm Surface Mount (SMD) 6 Pad SMT	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT782	5x7mm Surface Mount (SMD) 4 Pin Formed Lead	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	9	
	QT787	5x7mm Surface Mount (SMD) 6 Pin Formed Lead	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT783	5x7mm Surface Mount (SMD) 4 Pin Gull Wing	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	10	
	QT780	5x7mm Surface Mount (SMD) 6 Pin Gull Wing	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT778	Surface Mount (SMD) 4 Pin J-Lead	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	225kHz to 162.5MHz	11	
	QT788	Surface Mount (SMD) 4 Pin J-Lead	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT790	Surface Mount (SMD) 4 Pin Gull Wing	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	12	
	QT794	Surface Mount (SMD) 6 Pin Gull Wing	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT792	Surface Mount (SMD) 4 Pin Formed Lead	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	13	
	QT793	Surface Mount (SMD) 6 Pin Formed Lead	CMOS LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz		
	QT789	4 Pin Thru-hole	CMOS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	250kHz to 162.5MHz	14	

Electrical Performance Characteristics 225kHz to 162.5MHz CMOS

PARAMETERS	R	N	L	HC
Output Frequency Range (Fo)	225kHz – 85MHz	225kHz – 100MHz	225kHz – 162.5MHz	225kHz – 85MHz
Supply Voltage (Vdd)	+1.8Vdc ± 10%	+2.5Vdc ± 10%	+3.3Vdc ± 10%	+5Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	+5Vdc	+5Vdc	+5Vdc	+7Vdc
Operating Temperature (Top)	See Ordering Information			
Storage temperature (Tsto)	-62°C to +125°C			
Supply current (Idd) Note 1/	4mA Max. 225kHz – <40MHz 10mA Max. 40MHz – <50MHz 20mA Max. 50MHz – 85MHz	6mA Max. 225kHz – <40MHz 15mA Max. 40MHz – <60MHz 25mA Max. 60MHz – <85MHz 30mA Max. 85MHz – 100MHz	6mA Max. 225kHz – <16MHz 10mA Max. 16MHz – <32MHz 20mA Max. 32MHz – <70MHz 30mA Max. 70MHz – <125MHz 40mA Max. 125MHz – <140MHz 50mA Max. 140MHz – 162.5MHz	20mA Max. 225kHz – <16MHz 25mA Max. 16MHz – <32MHz 35mA Max. 32MHz – 85MHz
Load Note 2/	15pF//10kΩ			
Duty Cycle (Sym) Note 3/	45/55% Max. 225kHz – <16MHz 40/60% Max. 16MHz – 85MHz	45/55% Max. 225kHz – <16MHz 40/60% Max. 16MHz – 100MHz	45/55% Max. 225kHz – <16MHz 40/60% Max. 16MHz – 162.5MHz	45/55% Max. 225kHz – <16MHz 40/60% Max. 16MHz – 85MHz
Rise and Fall Times (Tr/Tf) Note 4/	6ns Max. for Fo < 40MHz 3ns Max. for Fo ≥ 40MHz			
Start-Up Time (Tstup)	10ms Max.			
Output Voltage High (VOH)	0.9*Vdd Min.			
Output Voltage Low (VOL)	0.1*Vdd Max.			
Enable/Disable (Tristate Option – D)	VIH ≥ 0.7*Vdd Oscillation VIL ≤ 0.3*Vdd High Impedance		VIH ≥ 2.2Vdc Oscillation VIL ≤ 0.8Vdc High Impedance	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm max. Each Year Thereafter			
Period Jitter 1σ (RMS) Integrated Phase Jitter Note 5/	5ps Typ. 1ps Max.			
Phase Noise (Typical)	10Hz Offset -74dBc/Hz 100Hz Offset -107dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -145dBc/Hz 1MHz Offset -150dBc/Hz		10Hz Offset -78dBc/Hz 100Hz Offset -109dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -145dBc/Hz 1MHz Offset -150dBc/Hz	
Notes	1/ No Load. 2/ Consult factory for different load. Capable to drive up to: 50pF (5V) and 30pF (3.3V and 2.5V). 3/ Measured at 1/2 Vdd. 4/ Measured between 10% and 90%. 5/ Period Jitter: By design; not tested. Integrated Phase Jitter: 12kHz to 20MHz.			

Electrical Performance Characteristics 40MHz to 162.5MHz LVDS

(For BiCMOS +2.5Vdc and +3.3Vdc LVDS Outputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	°C

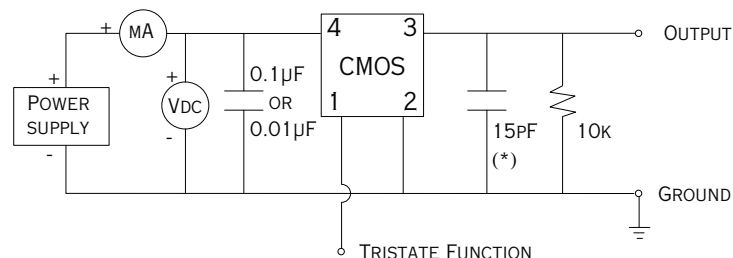
Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	80		162.5	MHz	
	+3.3Vdc	40		162.5		
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		3.135 2.375	3.3 2.5	3.465 2.625	Vdc Vdc	
Input Current	Measured without load at maximum Vdd			66	mA	
Output Voltage VOL		0.90	1.1		Vdc	
Output Voltage VOH			1.45	1.65	Vdc	
Differential Output Voltage (VOD)		247	330	454	mV	
Offset Voltage (VOS)		1.125	1.25	1.375	V	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	20% to 80%			600	ps	
Duty Cycle	50% of output	45	50	55	%	
Load		100Ω (Connected between Q & QNOT)			Ω	
Frequency Aging after 30 days	70°C±3°C			±1.5 ±2	ppm ppm	40MHz < F < 150MHz 150MHz < F < 162.5MHz (See Note 2)
Frequency Aging/Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100μs ramp			10	ms	
Output Enable VIH		0.7xVcc			Vdc	
Output Disable VIL				0.3xVcc	Vdc	Output High Impedance

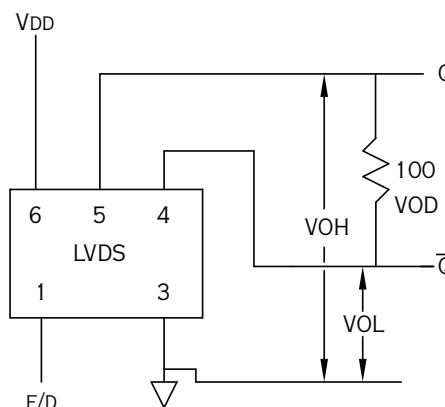
NOTES:

- Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±5%. Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.
- Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exceeds 30 day aging limit.
- Aging is ±5ppm after first year and ±2ppm/year thereafter.

TYPICAL TEST CIRCUIT FOR CMOS LOGIC

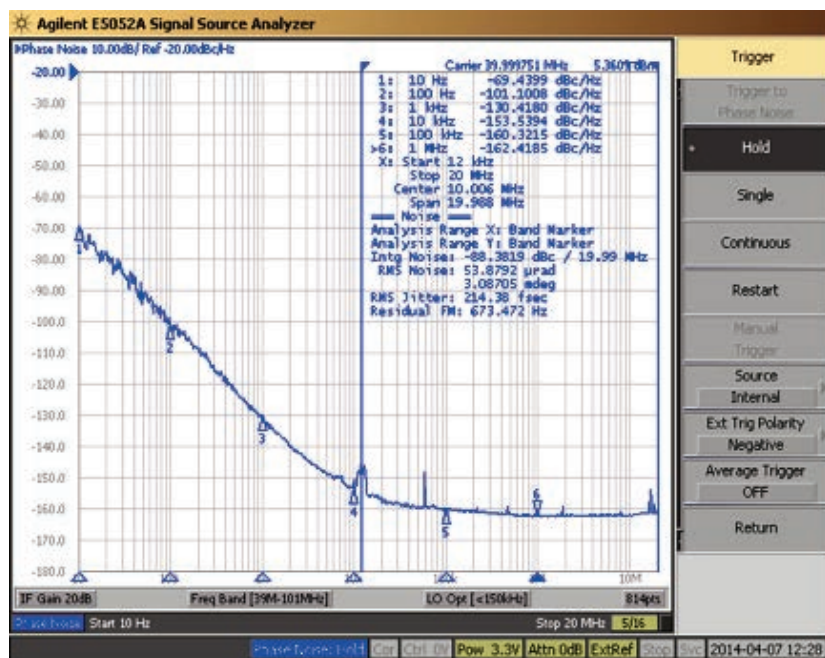


(*) CL INCLUDES PROBE AND JIG CAPACITANCE



LVDS TERMINATION

Figure 1 – Circuit Diagrams



Offset Frequency (Hz)	40MHz	80MHz
10	-70	-70
100	-101	-100
1E3	-131	-130
1E4	-153	-150
1E5	-160	-160
1E6	-160	-160

Figure 2 – Typical Phase Noise of a 40MHz QT781L-32.000MHz

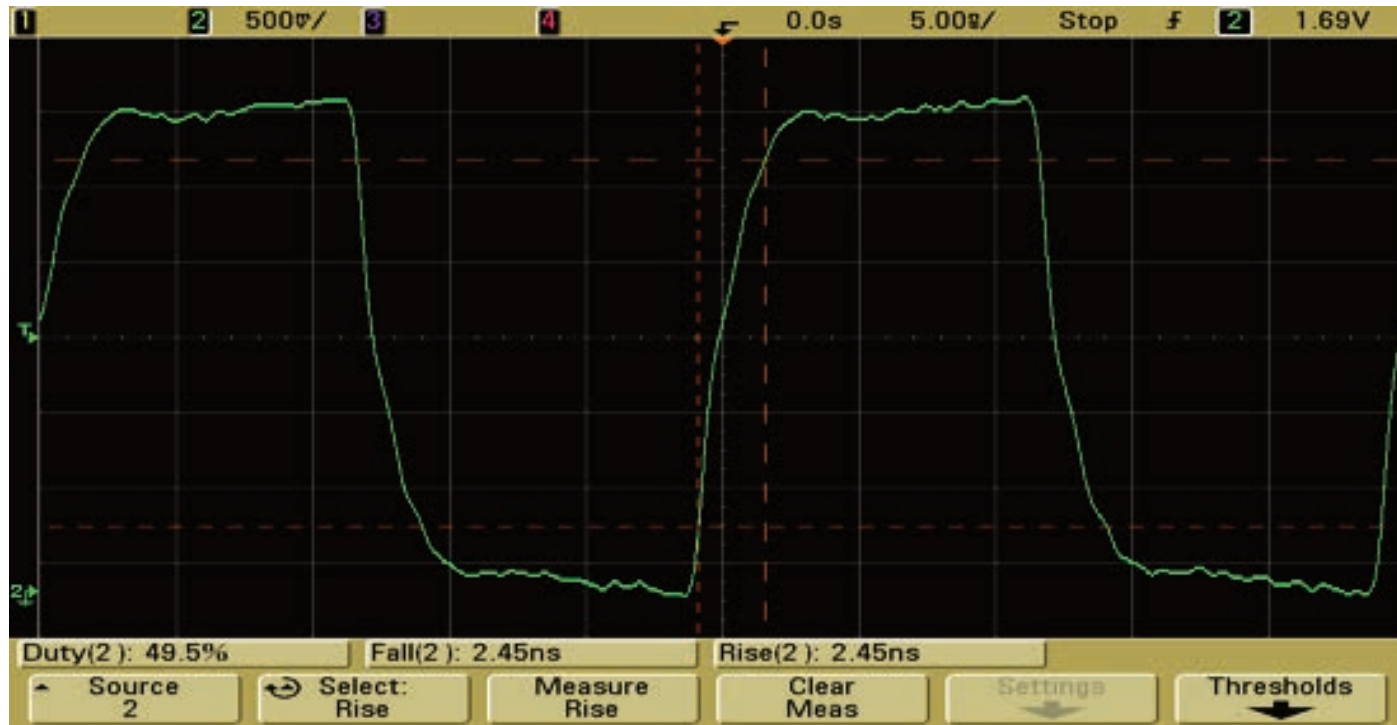
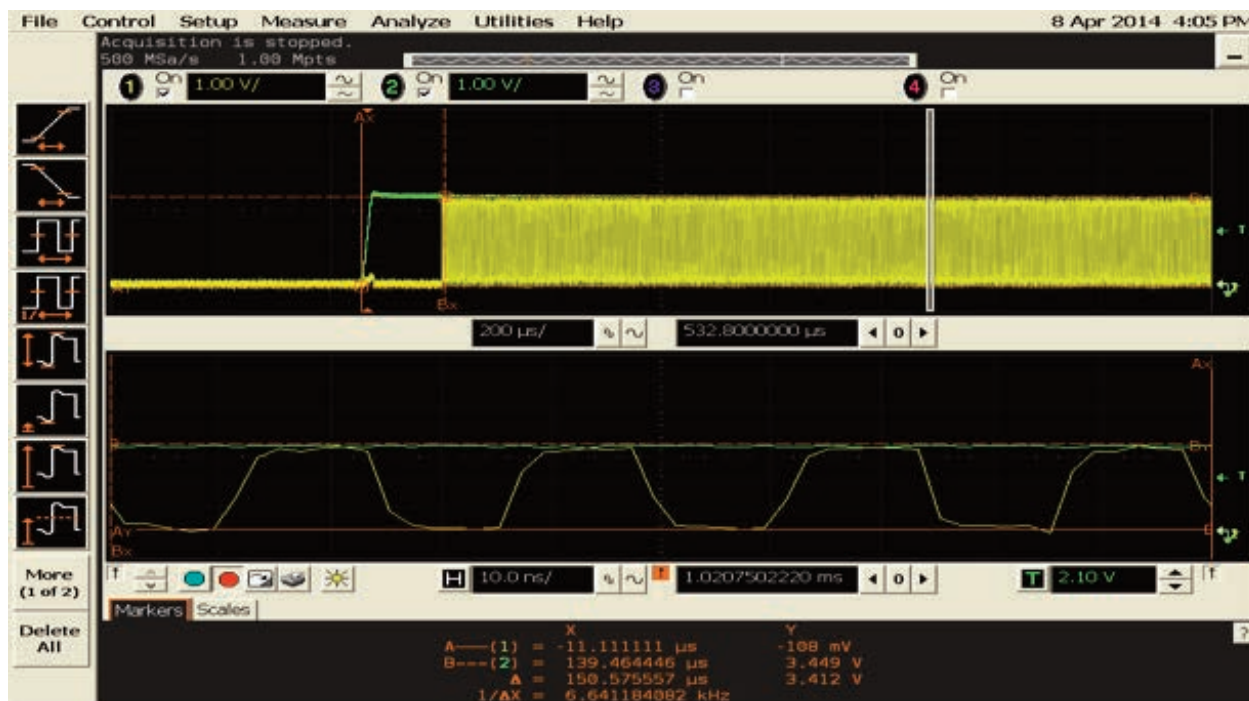
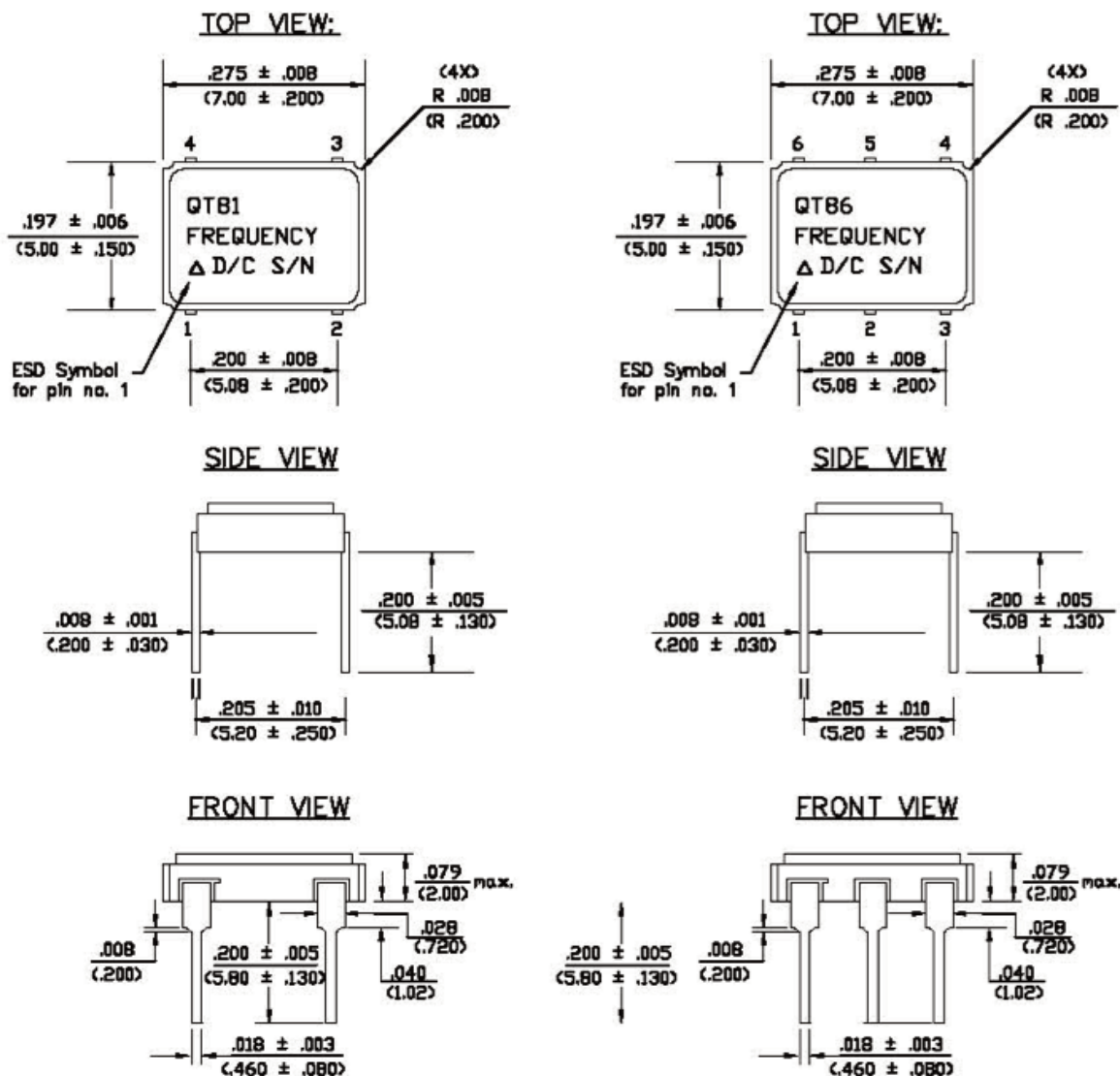


Figure 3 – Typical Start-Up Time and Output Waveform of a QT782L-40MHz 3.3Vdc

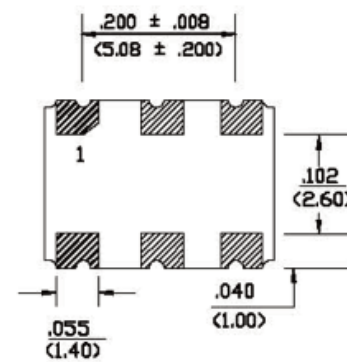
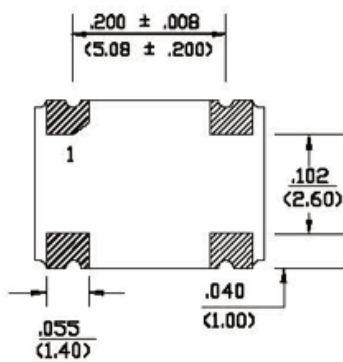
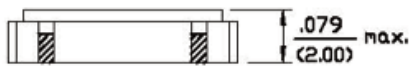
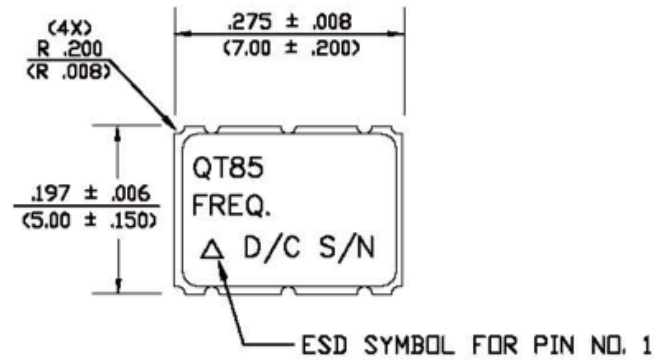
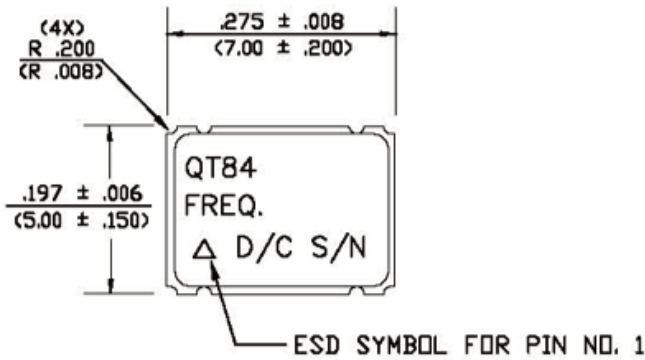


QT781 (Thru-hole, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT786 (Thru-hole 6 Leads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

Figure 4 – QT781 and QT786 Package Drawing and Pin Outputs

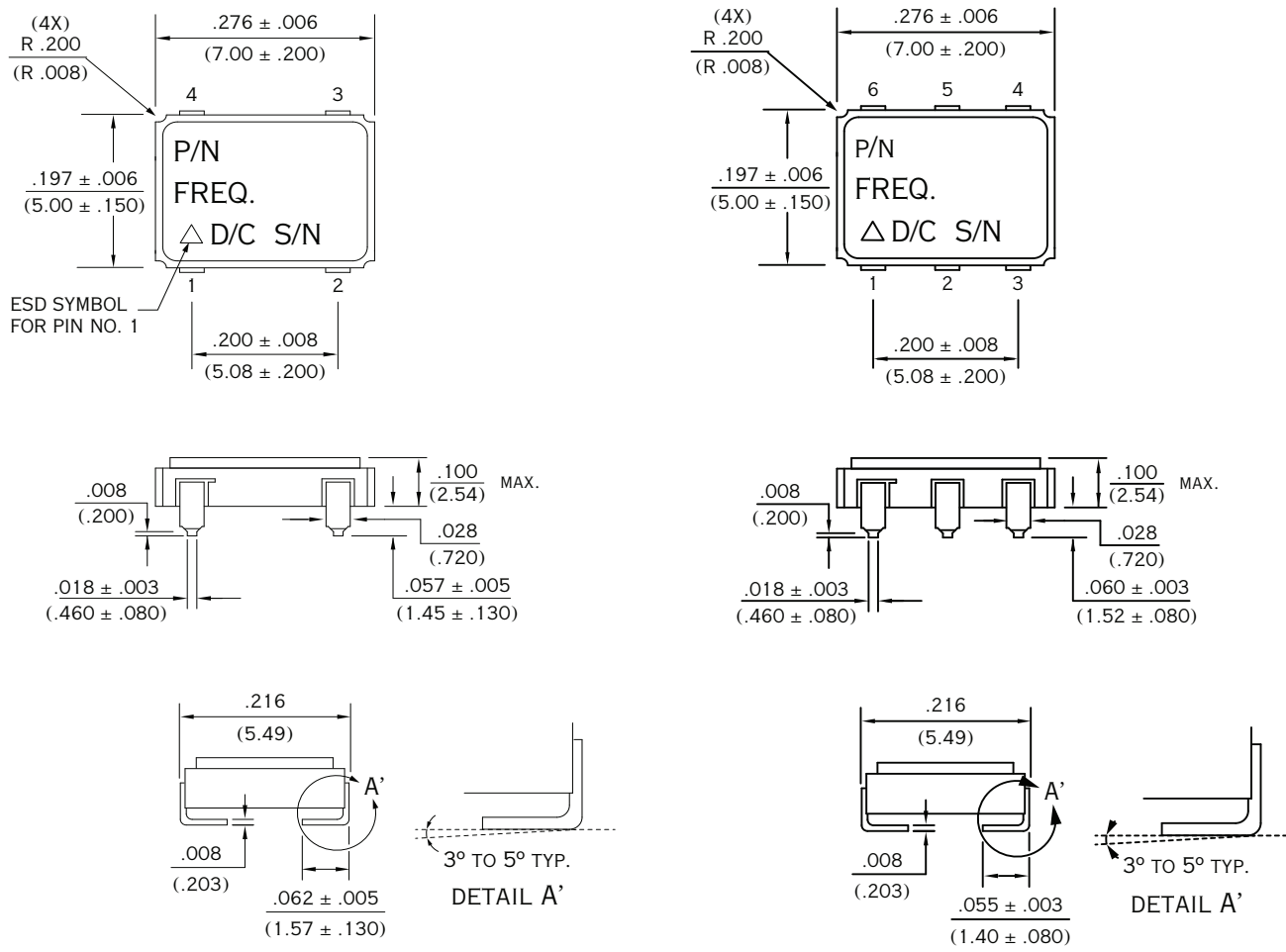
Dimensions are in inches (mm)



QT784 (SMT 4 Pads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT785 (SMT 6 Pads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

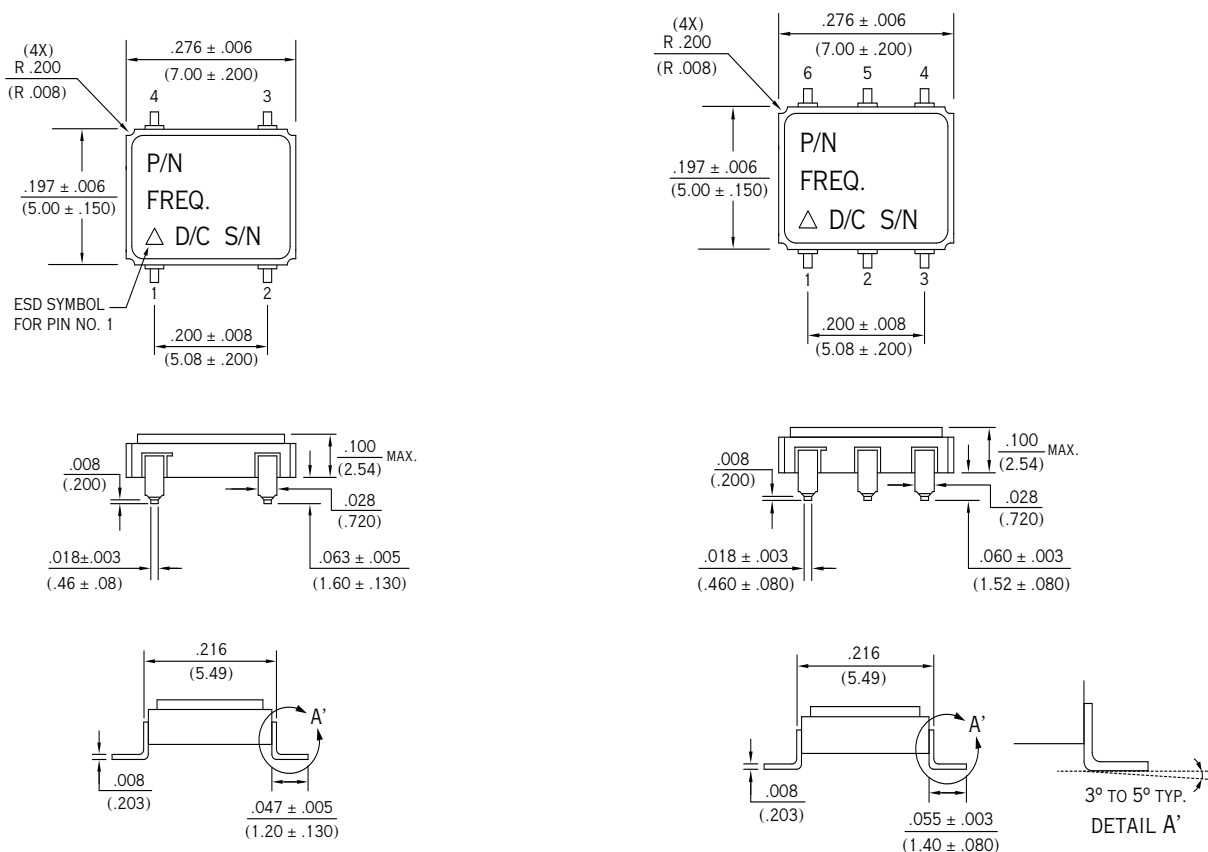
Figure 5 – QT784 and QT785 Package Drawing and Pin Outputs
Dimensions are in inches (mm)



QT782 (Formed Lead, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT787 (Formed Lead, 6 Leads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

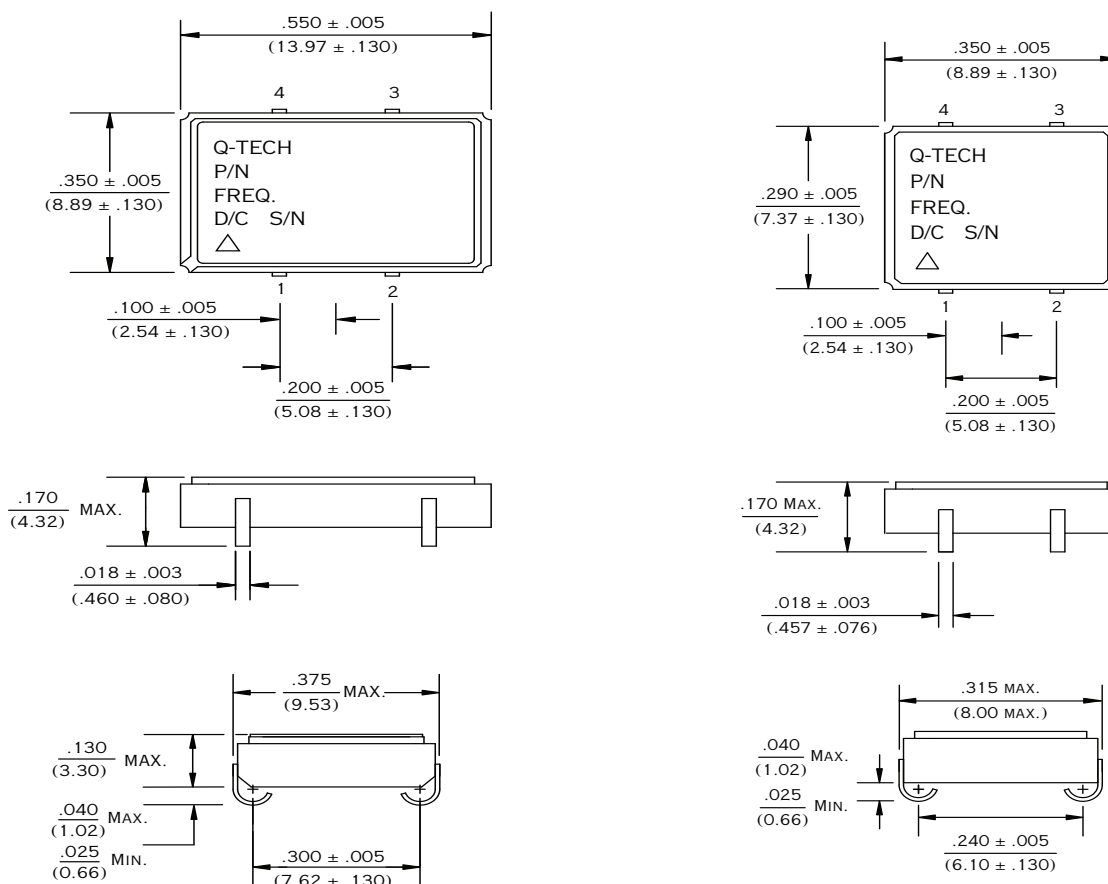
Figure 6 – QT782 and QT787 Package Drawing and Pin Outputs
Dimensions are in inches (mm)



QT783 (Gull Wing, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT780 (Gull Wing, 6 Leads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

Figure 7 – QT783 and QT780 Package Drawing and Pin Outputs
Dimensions are in inches (mm)

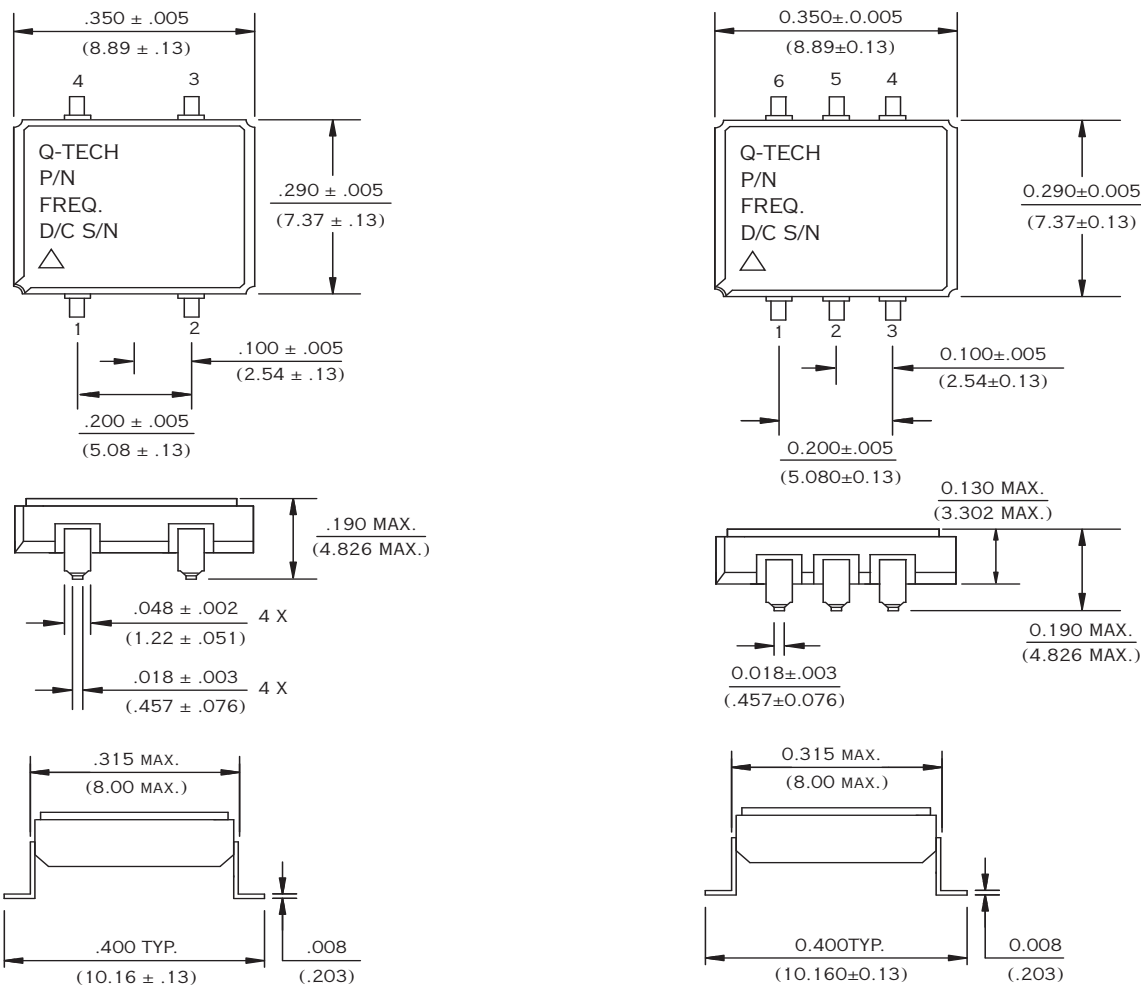


QT778 (J-Lead, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT788 (J-Lead, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

Figure 8 – QT778 and QT788 Package Drawing and Pin Outputs

Dimensions are in inches (mm)

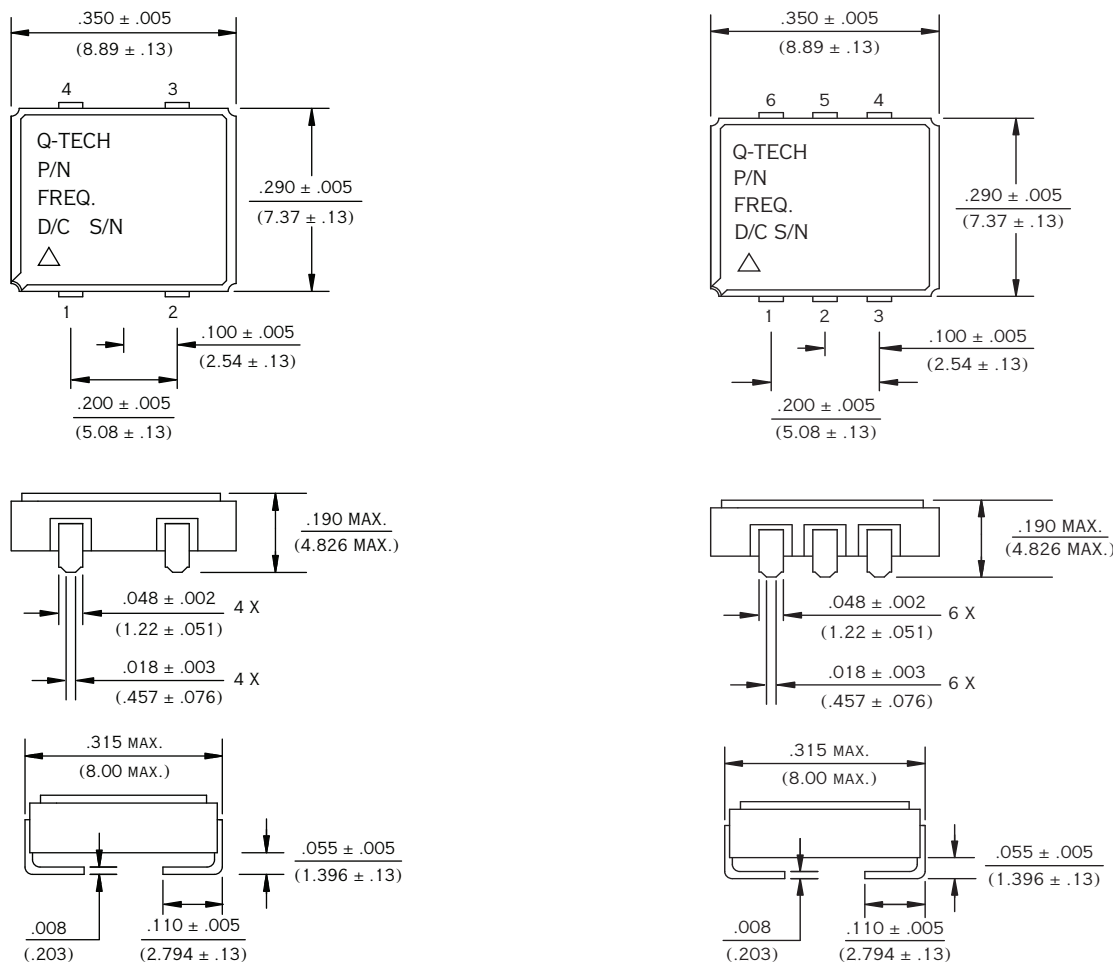


QT790 (Gull Wing, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT794 (Gull Wing, 6 Leads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

Figure 9 – QT790 and QT794 Package Drawing and Pin Outputs

Dimensions are in inches (mm)

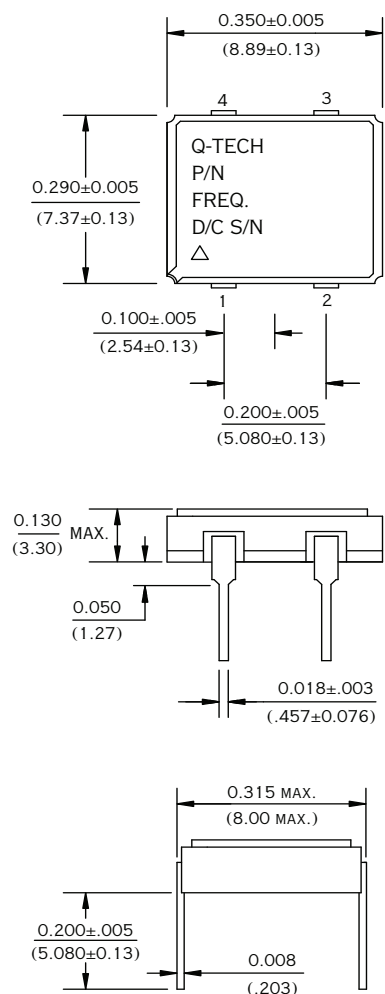


QT792 (Formed Lead, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT793 (Formed Lead, 6 Leads)	
Pin No.	Function
1	NC or ED
2	NC
3	GND/CASE
4	OUT (CMOS) OUTN (LVDS)
5	NC (CMOS) OUT (LVDS)
6	VDD

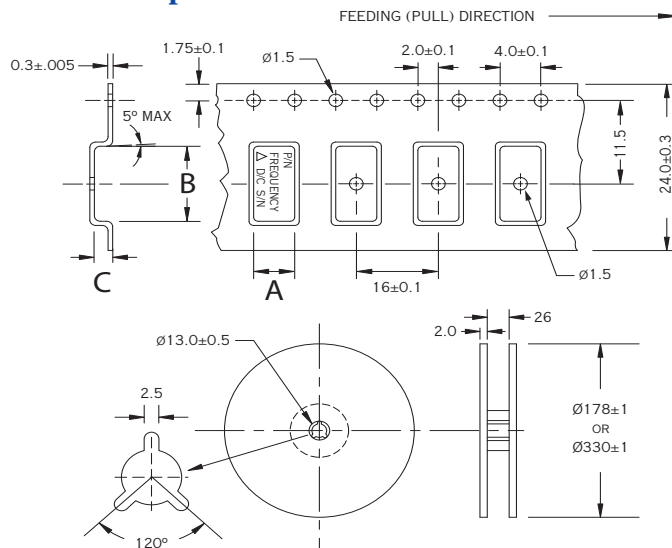
Figure 10 – QT792 and QT793 Package Drawing and Pin Outputs

Dimensions are in inches (mm)



QT789 (Thru-hole, 4 Leads)	
Pin No.	Function
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

Embossed Tape and Reel Information



Dimensions are in mm. Tape is compliant to EIA-481-A.

Package	A	B	C
QT778	10.01 ± 0.1	14.53 ± 0.1	4.80 ± 0.1
QT782, 787	5.72 ± 0.1	7.70 ± 0.1	4.10 ± 0.1
QT780, 783	7.65 ± 0.1	9.50 ± 0.1	4.70 ± 0.1
QT784, 785	5.35 ± 0.1	7.75 ± 0.1	1.85 ± 0.1
QT790, 794	9.470 ± 0.1	11.92 ± 0.1	6.16 ± 0.1
QT788, 792, 793	8.71 ± 0.1	9.55 ± 0.1	5.34 ± 0.1

Reel size vs. quantity:

Reel size (Diameter in mm)	Qty per reel (pcs)		
	QT778	QT784	QT780, 782, 788, 790
178	250	1000	150
330	1000		800

Figure 11 – QT789 Package Drawing and Pin Outputs

Dimensions are in inches (mm)

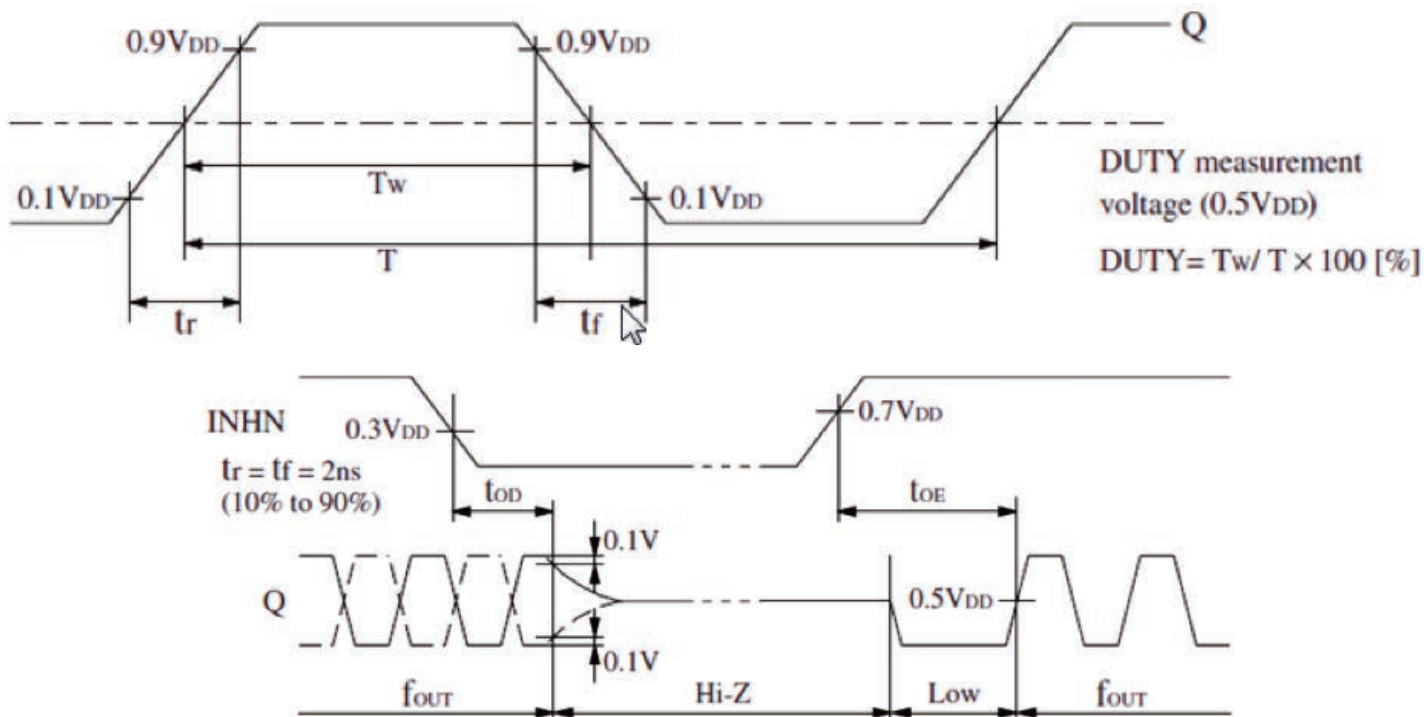


Figure 12 – Output Switching Waveform (Top) and Output Disable Timing Chart (Bottom)

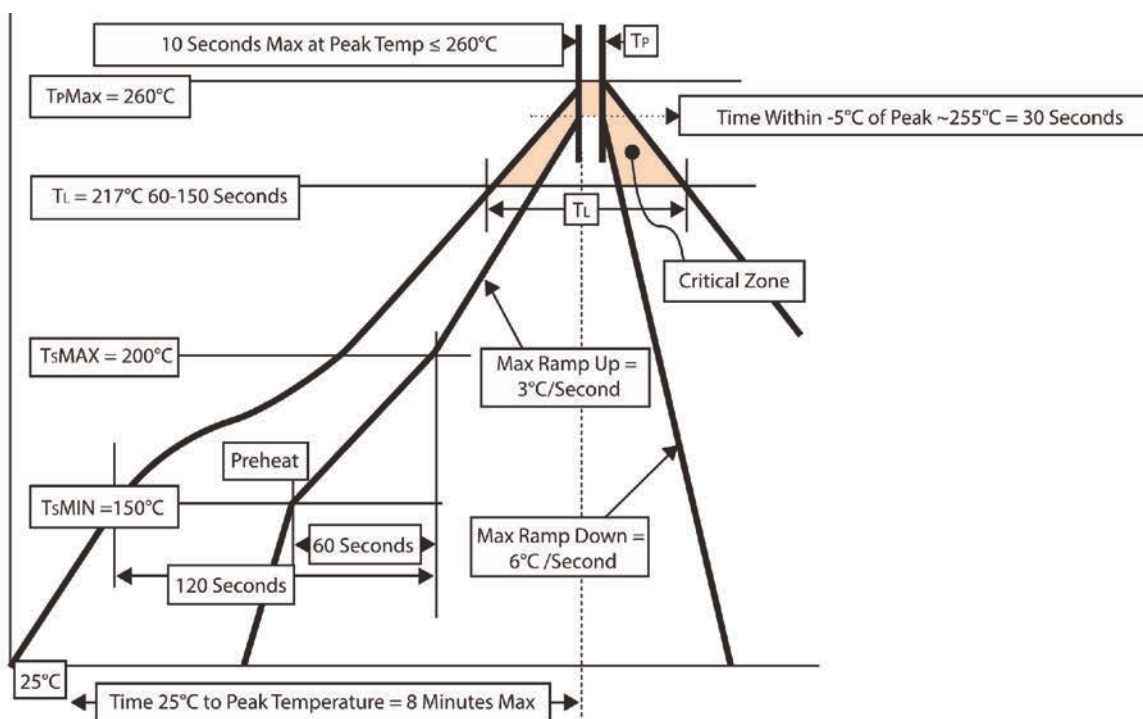


Figure 13 – Solder Reflow Profile Reflow Profile per IPC/JEDEC J-STD-020D.1, 240°C Reflow Profile Also Acceptable

SCREENING PER MIL-PRF-55310, LEVEL B PLUS PIND TEST

TEST	SPECIFICATION
Internal Visual	MIL-STD-883, Method 2017 and 2032
Stabilization Bake	MIL-STD-883, Method 1008, Condition C
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Constant Acceleration	MIL-STD-883, Method 2001, Test Condition A, Y1 axis only
Particle Impact Noise Detection	MIL-STD-883, Method 2020, Test Condition B
Fine Leak	MIL-STD-883, Method 1014, Condition A1
Gross Leak	MIL-STD-883, Method 1014, Condition C
Pre Burn-In	Electrical Test (Optional)
Burn-In (load)	Nominal Supply, +125°C for 160 hours minimum
Final Electrical Test	Electrical test at +25°C and frequency over temperature
External Visual	MIL-STD-883, Method 2009

SCREENING FOR ENGINEERING MODEL

TEST	SPECIFICATION
Internal Visual	MIL-STD-883, Method 2017 and 2032
Stabilization Bake	MIL-STD-883, Method 1008, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A1
Gross Leak	MIL-STD-883, Method 1014, Condition C
Final Electrical Test	Electrical test at +25°C and frequency over temperature
External Visual	MIL-STD-883, Method 2009

QUALITY CONFORMANCE INSPECTION TESTS (OPTIONAL)

GROUP	TEST METHOD	DESCRIPTION
A	MIL-PRF-55310, Level B, 100%	Electrical Tests (Supply voltage, Input Current, Output waveform, Rise and Fall times, Duty cycle, start-up time, overvoltage survivability, and 10 temperature frequency data points)
B	MIL-PRF-55310, Level B, 100%	Aging Test (Oscillator is energized in oven for a continuous period of 30 days at +70°C ± 3°C. The output frequency is measured within an interval of 72 hours maximum per MIL-PRF-55310)
C (Subgroups 1 to 4, excluded the "when specified" tests)	MIL-PRF-55310, Level B, sampling	4 (0)

ADDITIONAL INFORMATION

- 1) Design used a Class B integrated circuit, with Radiation features 50kRad(Si) Total Ionizing Dose and a high Q cultured quartz.
- 2) ESD HBM Class 1C.
- 3) Terminations are Gold plated 60 to 80 micro inches thick. Option Solder tinning Sn60Pb40 or SAC305 lead free solder.
- 4) Standard packaging in anti-static plastic tube.

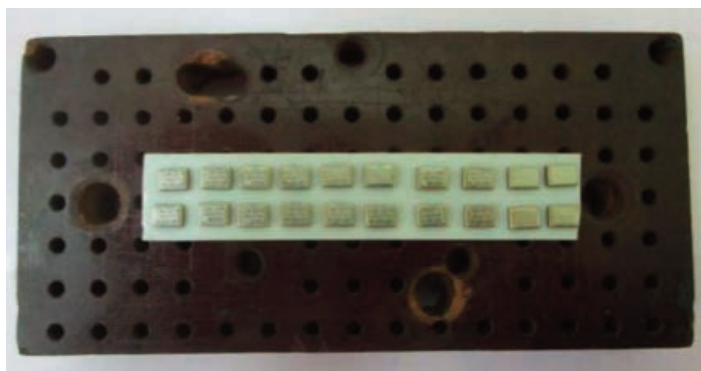


Figure 14 – Units to be Tested

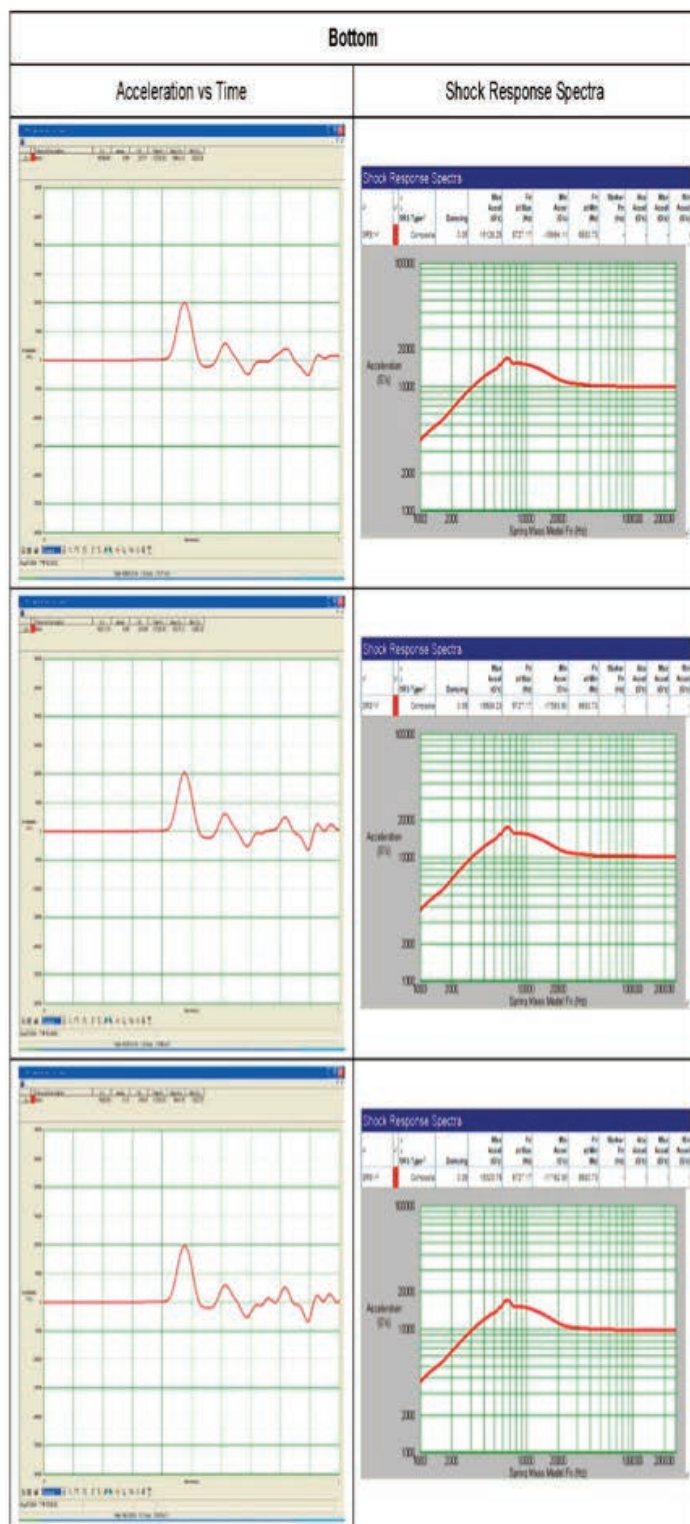


Figure 15 – Mechanical Shock Test Set Up

Figure 16 – Graph of Mechanical Shock Test

DCO	REV	REVISION SUMMARY	PAGE	DATE
6380	A	Rename from QT781 series to QT780 series	All	1/27/17
		Add QT78, 88, 89, 90, 92, 93, 94 options	All	
		Add 'Product Offerings' table	2	
		Change range of operating frequency to 230k - 162.5MHz	All	
		Combined multiple Electrical Parameters tables into one	3	
		Removed TTL option	All	
		Add tape and reel information	13	
		Add temperature code 16	1	
		Change 30kRad(Si) to 50kRad(Si)	1, 15	
		Add Fine Leak Rate	15	
		Remove 4 point mount information	1	
6482	B	Update package photos (All packages now have pictures)	1	3/2/17
		Add frequency codes 2, 15, and 19	1	
		Add LVDS options	1, 2	
		Add LVDS Electrical Characteristics	4	
		Add LVDS Test Circuit diagram	5	
		Revise pinouts to include LVDS outputs on applicable parts	7, 8, 9, 10, 12, 13	
12070	C	Add screening option 'E' Engineering Model and EM Screening Table	1, 16	09/04/2020
		Extend frequency range down to 225kHz for QT778 package	All	
		Fix VOS (typ) specification typo (was 1.125, changed to 1.25)	4	
		Remove note 1 (leak test) on screening table	16	