High-Speed CMOS 16Kx4 SRAM with Separate I/O

QS8881
QS8882

FEATURES/BENEFITS

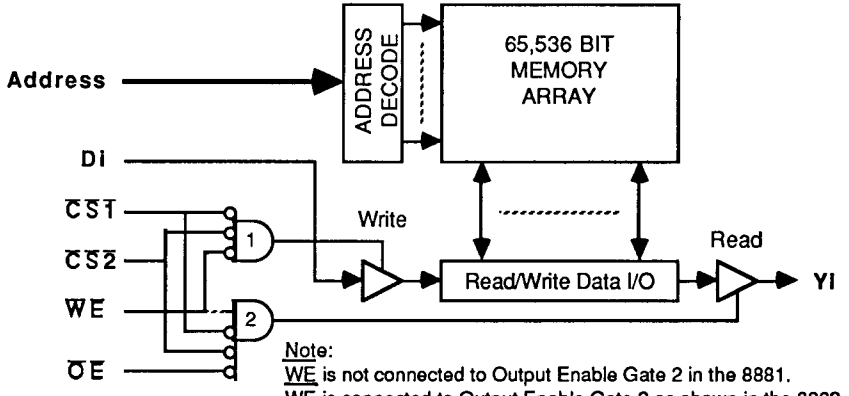
- High Speed Access and Cycle times
- 10ns/12ns/15ns/20ns Commercial
- JEDEC standard pinout
- TTL compatible I/O
- Low power, high-speed QCMOS™ technology
- 6-Transistor cell for high reliability
- Ideal for reliable,dense memory systems
- Available in 28-pin DIPs, 28-pin 300 mil SOJ , 28-pin LCC
- Low Standby current

2

DESCRIPTION

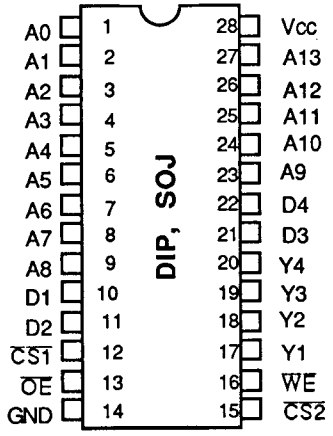
The QS8881 and QS8882 are high-speed 64K SRAMs organized as 16Kx4 with separate read and write data buses. In the 8881, the read data outputs follow the inputs during a write; in the 8882, the outputs are disabled during a write. The 8881 and 8882 are manufactured in a high-performance CMOS process, and they are based on a 6-transistor cell design for high reliability of data retention. Their high-speed access times make them useful in cache data RAM, cache tag RAMs, high-speed scratchpad memories, look-up tables, pipelined DSP and bit-slice systems. Low operating power and excellent latch-up and ESD protection are provided.

FUNCTIONAL BLOCK DIAGRAM



Note:
WE is not connected to Output Enable Gate 2 in the 8881.
WE is connected to Output Enable Gate 2 as shown in the 8882.

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
D	I	Write Data In
Y	O	Read Data Out
$\overline{CS}$	I	Chip Select
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

$\overline{CS1}$	$\overline{CS2}$	$\overline{WE}$	Y Outputs		Power	Function
			8881	8882		
H	X	X	High Z	High Z	Standby	Deselect
X	H	X	High Z	High Z	Standby	Deselect
L	L	H	Data Out	Data Out	Active	Read
L	L	L	Data In	High Z	Active	Write

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to V_{CC} + 0.5V
DC Input Voltage V_I ..... -0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Output Current Max. sink current/pin..... 50 mA
DC Output Current Max. source current/pin..... 30 mA
T_{BIAS} Temperature Under Bias, COM..... -65° to +125°C
T_{STG} Storage Temperature, COM..... -65° to +125°C
T_{BIAS} Temperature Under Bias, MIL..... -65° to +135°C
T_{STG} Storage Temperature, MIL..... -65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

2

CAPACITANCE

Ta=+25°C, f=1 MHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V PDIP Pkg.	3	6	pF
Cin	Input Capacitance	Vin = 0 V SOJ Pkg.	2.5	5	pF
Cout	Output Capacitance	Vout = 0 V PDIP Pkg.		7	pF
Cout	Output Capacitance	Vout = 0 V SOJ Pkg.		7	pF

Capacitance is guaranteed by design but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions	Min	Max	Unit
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4	
| Ili |	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5	µA
| Ilo |	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5	

Notes:
1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10%
Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-10	-12	15	-20	Unit
Icc1	Static Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = 0	100	100	100	100	mA
Icc2	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX	145	135	125	120	
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX	60	60	60	60	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc	15	15	15	15	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10%
See Read Timing Diagrams. All values in nanoseconds unless otherwise noted

Symbol	Parameter	-10 (3)		-12 (3)		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max
READ CYCLE									
t RC	Read Cycle Time (1)	10	-	12	-	15	-	19	-
t AA	Address Access Time	-	10	-	12	-	15	-	19
t ACS	Chip Select Access Time	-	10	-	12	-	15	-	19
t OH	Output Hold from Address Change	2	-	2	-	2	-	3	-
t CLZ	Chip Select to Output in Low Z (2)	2	-	2	-	2	-	2	-
t CHZ	Chip Select to Output in High Z (2)	-	5	-	5	-	7	-	8
t OE	Output Enable to Data Valid	-	5	-	6	-	6	-	8
t OLZ	Output Enable to Output in Low Z (2)	2	-	2	-	2	-	2	-
t OHZ	Output Enable to Output in High Z (2)	-	4	-	4	-	5	-	7
t PU	Chip Select to Power Up Time (2)	0	-	0	-	0	-	0	-
t PD	Chip Select to Power Down Time (2	10	-	12	-	15	-	19	-

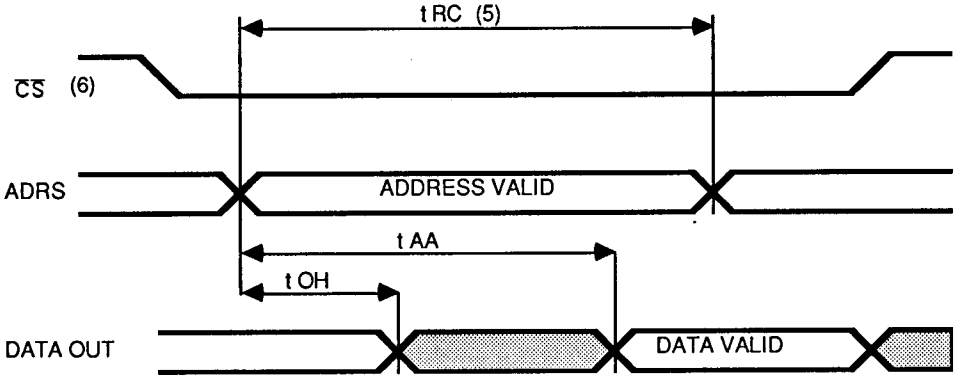
Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Vcc±5%

Commercial TA = 0° C to 70°C, Vcc = 5.0V±10%
See Write Timing Diagrams. All values in nanoseconds unless otherwise noted

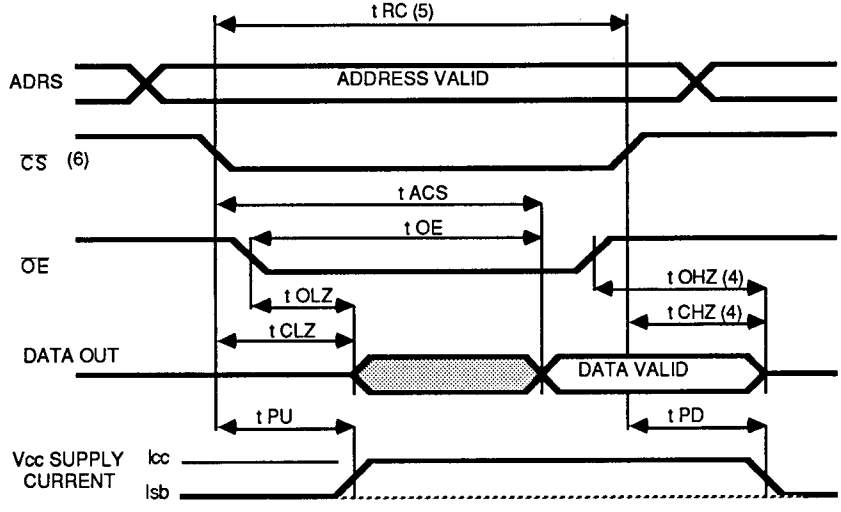
Symbol	Parameter	-10 (3)		-12 (3)		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE									
t WC	Write Cycle Time (1)	10	-	12	-	15	-	19	-
t CW	Chip Select Valid to End of Write	8	-	10	-	13	-	17	-
t AW	Address Valid to End of Write	8	-	10	-	13	-	17	-
t AS	Address Setup Time	0	-	0	-	0	-	0	-
t WP	Write Pulse width	8	-	10	-	12	-	16	-
t WR	Write Recovery Time	0	-	0	-	0	-	0	-
t DW	Data Valid to End of Write	5	-	6	-	8	-	10	-
t DH	Data Hold Time	0	-	0	-	0	-	0	-
t WZ	Write Enable to Output in Hi Z (2,4)	-	4	-	5	-	6	-	7
t OW	Output Active from End of Write (4)(2)	2	-	2	-	2	-	2	-
t IY	Data to Output Delay (5)	-	8	-	10	-	12	-	15
t WY	Write Enable to Output Delay (5)	-	8	-	10	-	12	-	15

Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Vcc±5%
4) 8882 Only. (8881 outputs remain on during write.)
5) 8881 Only. (8882 outputs go to Hi-Z during write.)

TIMING WAVEFORMS - READ CYCLE NO. 1 (1,2,6)



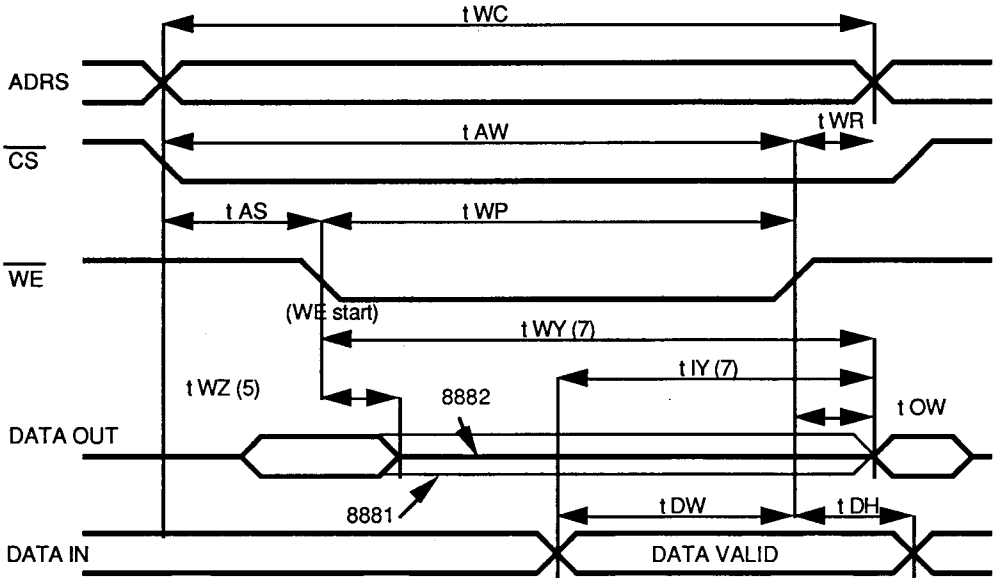
TIMING WAVEFORMS - READ CYCLE NO. 2 (1,3,6)



Notes:

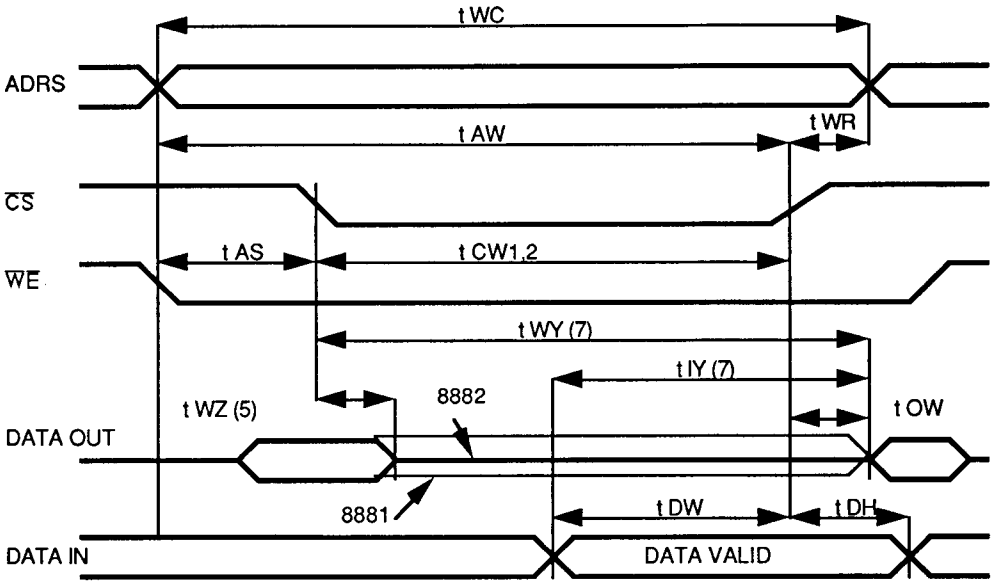
1. WE is high for Read cycle.
2. CS is low for Read cycle #1.
3. Address is valid to or coincident with CS transition time for Read Cycle #2.
4. Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.
5. All read timings are referenced from the last valid address to the first transitioning address.
6. CS is defined as active during the overlap of CS1 and CS2. Both CS1 and CS2 must be active for read or write.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (1,2,3,6 $\overline{WE}$ controlled timing)



Notes:
1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t WR is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.
6. $\overline{CS}$ is defined as active during the overlap of $\overline{CS1}$ and $\overline{CS2}$. Both $\overline{CS1}$ and $\overline{CS2}$ must be active for read or write.
7. t WY and t IY are data in to data out flow through times during write and are defined for 8881 only.

TIMING WAVEFORMS-WRITE CYCLE No. 2 (1,2,3,4,6 $\overline{CS}$ controlled timing)



Notes:
1. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t WR is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. Transition to Hi-Z is measured ± 200 mV change from the previous steady state voltage.
6. $\overline{CS}$ is defined as active during the overlap of $\overline{CS1}$ and $\overline{CS2}$. Both $\overline{CS1}$ and $\overline{CS2}$ must be active for read or write.
7. t WY and t IY are data in to data out flow through times during write and are defined for 8881 only.