Automotive 8K x 8 SRAM

Features

- ☐ 8192 x 8 bit static CMOS RAM
- ☐ 70 ns Access Time
- ☐ Common data inputs and outputs
- ☐ Three-state outputs
- ☐ Typ. operating supply current: 30 mA
- ☐ TTL/CMOS-compatible
- ☐ Automatic reduction of power dissipation in long Read or Write cycles
- ☐ Power supply voltage 5 V
- ☐ Operating temperature ranges -40 to 125 °C
- ☐ Quality assessment according to CECC 90000, CECC 90100 and CECC 90111
- ☐ ESD protection > 2000 V (MIL STD 883C M3015.7)
- ☐ Latch-up immunity > 100 mA
- ☐ Packages: SOP28 (300 mil) SOP28 (330 mil)

Description

The U6264ASA07 is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read - Standby
- Write - Data Retention

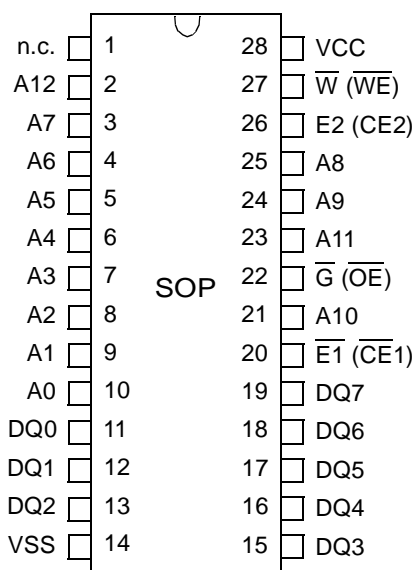The memory array is based on a 6-transistor cell.

The circuit is activated by the rising edge of E2 (at $\overline{E1}$ = L), or the falling edge of $\overline{E1}$ (at E2 = H). The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. During the active state ($\overline{E1}$ = L and E2 = H), each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word read will be available at the outputs DQ0 - DQ7. After the address change, the data outputs go High-Z until the new read information is available. The full CMOS data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current (at I_O = 0 mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or $\overline{W}$, or by the rising edge of $\overline{E1}$, respectively.

Data retention is guaranteed down to 2 V. With the exception of E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

If the circuit is inactivated by E2 = L, the standby current (TTL) drops to 150 µA typ.

Pin Configuration

n.c.	1		28	VCC
A12	2		27	$\overline{W}$ ($\overline{WE}$)
A7	3		26	E2 (CE2)
A6	4		25	A8
A5	5		24	A9
A4	6		23	A11
A3	7	SOP	22	$\overline{G}$ ($\overline{OE}$)
A2	8		21	A10
A1	9		20	$\overline{E1}$ ($\overline{CE1}$)
A0	10		19	DQ7
DQ0	11		18	DQ6
DQ1	12		17	DQ5
DQ2	13		16	DQ4
VSS	14		15	DQ3

Top View

Pin Description

Signal Name	Signal Description
A0 - A12	Address Inputs
DQ0 - DQ7	Data In/Outputs
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Enable
VCC	Power Supply Voltage
VSS	Ground
n.c.	not connected

U6264ASA07

Block Diagram
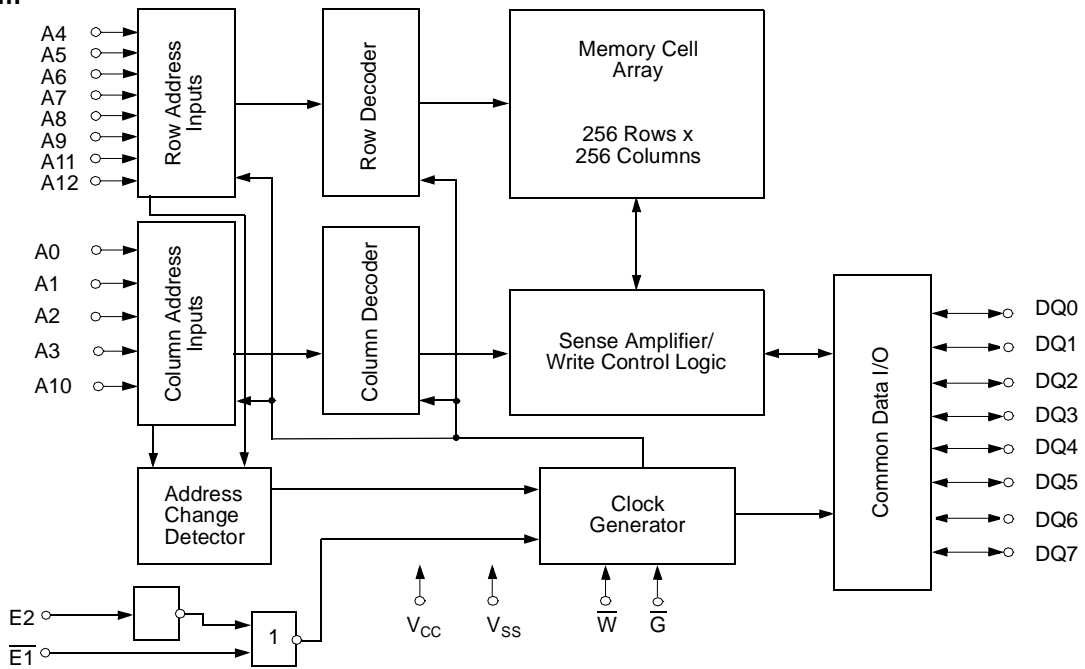
Truth Table

Operating Mode	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	*	L	*	*	High-Z
	H	*	*	*	High-Z
Internal Read	L	H	H	H	High-Z
Read	L	H	H	L	Data Outputs, Low-Z
Write	L	H	L	*	Data Inputs, High-Z

* H or L

Characteristics

All voltages are referenced to $V_{SS} = 0$ V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of $V_{IL} = 0$ V and $V_{IH} = 3$ V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times, in which cases transition is measured ± 200 mV from steady-state voltage.

Maximum Ratings	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{CC}	-0.3	7	V
Input Voltage	V_I	-0.3	$V_{CC} + 0.5$	V
Output Voltage	V_O	-0.3	$V_{CC} + 0.5$	V
Power Dissipation	P_D		1	W
Operating Temperature	T_a	-40	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Data Retention Voltage	$V_{CC(DR)}$		2.0	-	V
Input Low Voltage*	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC}+0.3	V

* -2 V at Pulse Width 10 ns

Electrical Characteristics	Symbol	Conditions		Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} V_{IL} V_{IH} t_{cW}	= 5.5 V = 0.8 V = 2.2 V = 70 ns		55	mA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} $V_{\overline{E1}} = V_{E2}$ or V_{E2}	= 5.5 V = 2.2 V = 0.8 V		3	mA
Output High Voltage		V_{CC} I_{OH}	= 4.5 V = -1.0 mA			
TTL compatible	V_{OH}			2.4	-	V
CMOS compatible	V_{OH}			0.85*V_{CC}	-	V
Output Low Voltage	V_{OL}	V_{CC} I_{OL}	= 4.5 V = 3.2 mA	-	0.4	V
Output High Current	I_{OH}	V_{CC} V_{OH}	= 4.5 V = 2.4 V	-	-1	mA
Output Low Current	I_{OL}	V_{CC} V_{OL}	= 4.5 V = 0.4 V	3.2	-	mA
Supply Current - Standby Mode (CMOS level)	$I_{CC(SB)}$	V_{CC} $V_{\overline{E1}} = V_{E2}$ or V_{E2}	= 5.5 V = V_{CC}-0.2 V = 0.2 V		30	µA
Supply Current - Data Retention Mode	$I_{CC(DR)}$	$V_{CC(DR)}$ $V_{\overline{E1}} = V_{E2}$ or V_{E2}	= 3 V = $V_{CC(DR)}$ - 0.2 V = 0.2 V		10	µA
Input High Leakage Current	I_{IH}	V_{CC} V_{IH}	= 5.5 V = 5.5 V	-	2	µA
Input Low Leakage Current	I_{IL}	V_{CC} V_{IL}	= 5.5 V = 0 V	-2	-	µA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	V_{CC} V_{OH}	= 5.5 V = 5.5 V	-	2	µA
Low at Three-State Outputs	I_{OLZ}	V_{CC} V_{OL}	= 5.5 V = 0 V	-2	-	µA

ZMD

Switching Characteristics	Symbol		Min.	Max.	Unit
	Alt.	**IEC**			
Time to Output in Low-Z	t_{LZ}	$t_{t(QX)}$	5	10	ns
Cycle Time					
Write Cycle Time	t_{WC}	t_{cW}	70	-	ns
Read Cycle Time	t_{RC}	t_{cR}	70	-	ns
Access Time					
$\overline{E1}$ LOW or E2 HIGH to Data Valid	t_{ACE}	$t_{a(E)}$	-	70	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$	-	40	ns
Address to Data Valid	t_{AA}	$t_{a(A)}$	-	70	ns
Pulse Widths					
Write Pulse Width	t_{WP}	$t_{w(W)}$	50	-	ns
Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	65	-	ns
Setup Times					
Address Setup Time	t_{AS}	$t_{su(A)}$	0	-	ns
Chip Enable to End of Write	t_{CW}	$t_{su(E)}$	65	-	ns
Write Pulse Width	t_{WP}	$t_{su(W)}$	50	-	ns
Data Setup Time	t_{DS}	$t_{su(D)}$	35	-	ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0	-	ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0	-	ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	5	-	ns
$\overline{E1}$ HIGH or E2 LOW to Output in High-Z	t_{HZCE}	$t_{dis(E)}$	0	25	ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$	0	30	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$	0	25	ns

Data Retention Mode $\overline{E1}$-Controlled
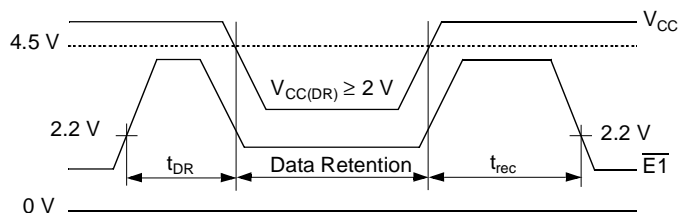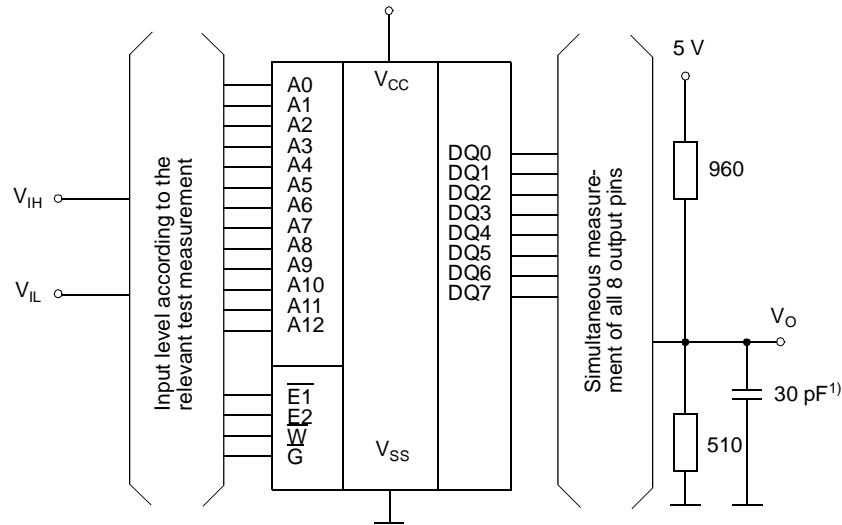
Data Retention Mode E2-Controlled
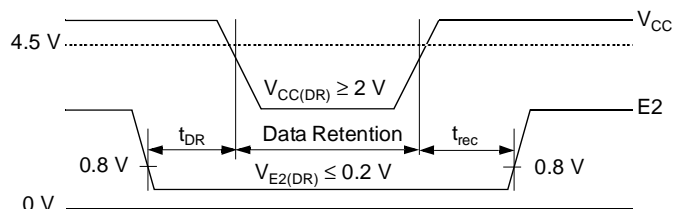
$V_{E2(DR)} \geq V_{CC(DR)} - 0.2\ V$ or $V_{E2(DR)} \leq 0.2\ V$
$V_{CC(DR)} - 0.2\ V \leq V_{\overline{E1}(DR)} \leq V_{CC(DR)} + 0.3\ V$

Chip Deselect to Data Retention Time	t_{DR}:	min 0 ns
Operating Recovery Time	t_{rec}:	min t_{cR}

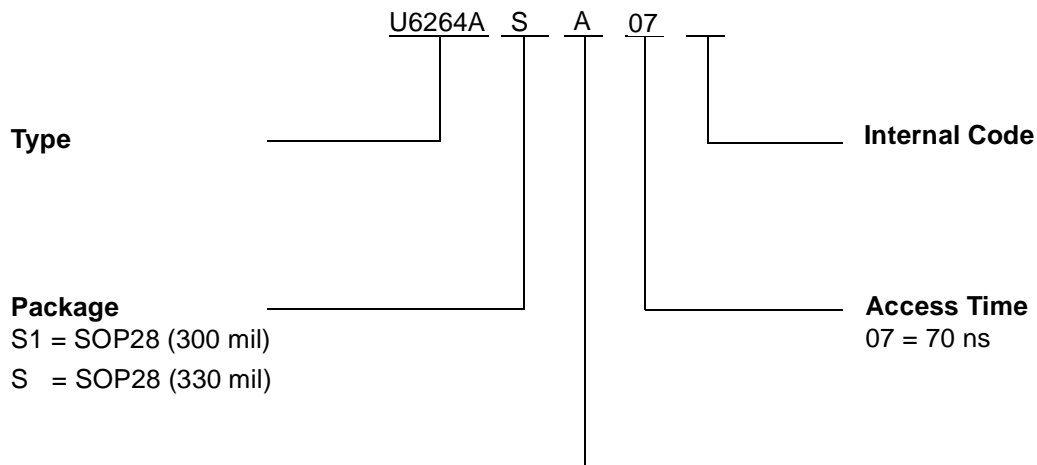**Test Configuration for Functional Check
(for TTL output levels)**

[1] In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 5.0$ V $V_I = V_{SS}$	C_I		8	pF
Output Capacitance	f = 1 MHz $T_a = 25\,°C$	C_O		10	pF

IC Code Numbers

Example   U6264A   S   A   07

Type

Package
S1 = SOP28 (300 mil)
S = SOP28 (330 mil)

Internal Code

Access Time
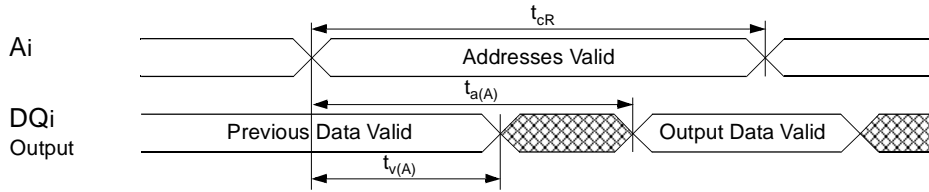07 = 70 ns
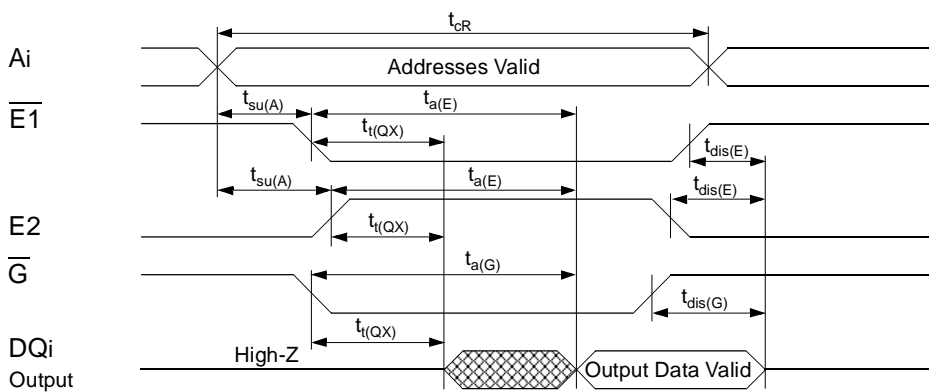
Operating Temperature Range
A = -40 to 125 °C

The date of manufacture is given by the last 4 digits of the third line of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.
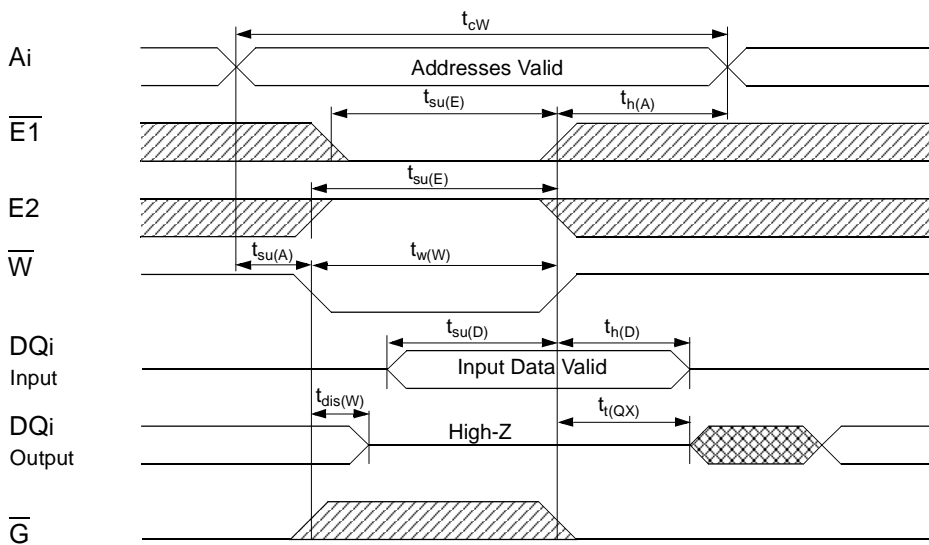Assembly location and trace code are shown in line 4.

U6264ASA07

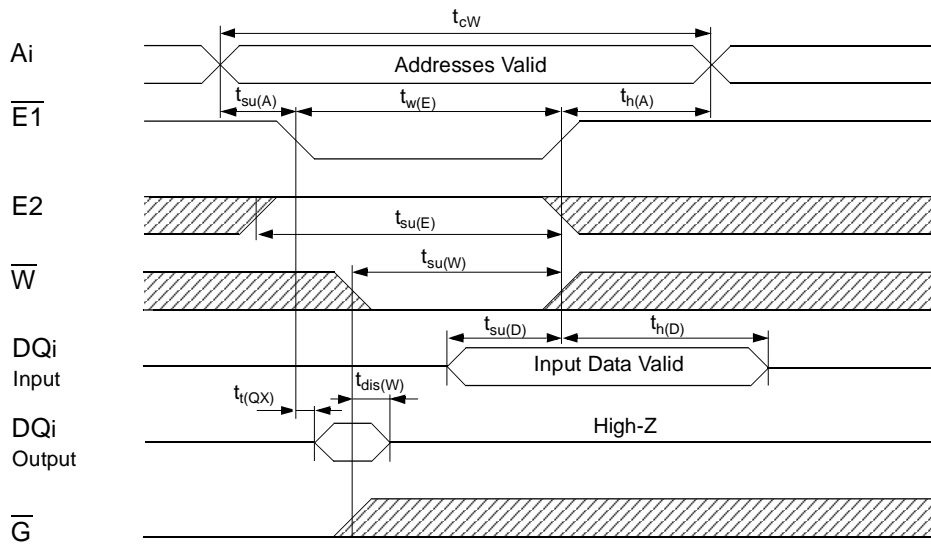**Read Cycle 1 (during Read cycle: $\overline{E1} = \overline{G} = V_{IL}$, $E2 = \overline{W} = V_{IH}$)**

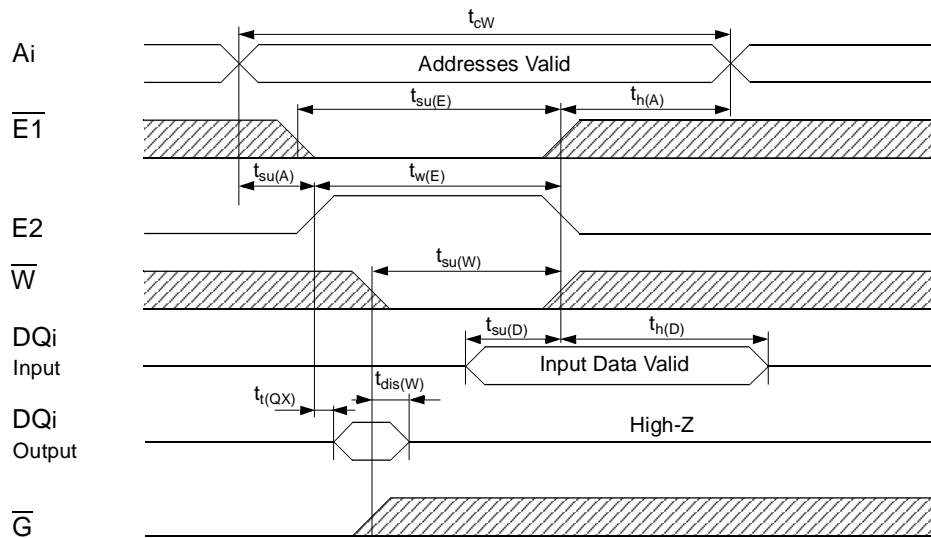**Read Cycle 2 (during Read cycle: $\overline{W} = V_{IH}$)**

Write Cycle 1 ($\overline{W}$-controlled)

Write Cycle 2 ($\overline{E1}$-controlled)

Ai — Addresses Valid — t_{cW} — $t_{su(A)}$ — $t_{w(E)}$ — $t_{h(A)}$

$\overline{E1}$

E2 — $t_{su(E)}$

$\overline{W}$ — $t_{su(W)}$

DQi Input — Input Data Valid — $t_{su(D)}$ — $t_{h(D)}$

DQi Output — High-Z — $t_{t(QX)}$ — $t_{dis(W)}$

$\overline{G}$

Write Cycle 3 (E2-controlled)

Ai — Addresses Valid — t_{cW}

$\overline{E1}$ — $t_{su(E)}$ — $t_{h(A)}$

E2 — $t_{su(A)}$ — $t_{w(E)}$

$\overline{W}$ — $t_{su(W)}$

DQi Input — Input Data Valid — $t_{su(D)}$ — $t_{h(D)}$

DQi Output — High-Z — $t_{t(QX)}$ — $t_{dis(W)}$

$\overline{G}$

undefined   L- or H-level

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