



NDS9953A Dual P-Channel Enhancement Mode Field Effect Transistor

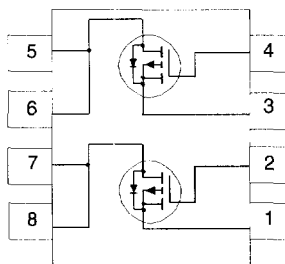
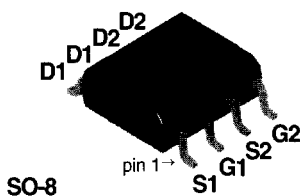
General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.9A, -30V. $R_{DS(ON)} = 0.13\Omega @ V_{GS} = -10V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.

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Absolute Maximum Ratings $T_A = 25\text{ C}$ unless otherwise noted

Symbol	Parameter		NDS9953A	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 2.9	A
	- Pulsed		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	C/W

Electrical Characteristics (T _A = 25°C unless otherwise noted)							
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _b = -250 μA	-30			V	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-2	μA	
			T _J = 55°C			-25	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA	
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA	
ON CHARACTERISTICS (Note 2)							
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _b = -250 μA		-1	-1.6	-2.8	V
			T _J = 125°C	-0.85	-1.25	-2.5	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _b = -1.0 A			0.11	0.13	Ω
			T _J = 125°C		0.15	0.21	
			V _{GS} = -4.5 V, I _b = -0.5 A		0.17	0.2	
			T _J = 125°C		0.24	0.32	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -5 V				A	
			T _J = 125°C	-10			
		V _{GS} = -4.5 V, V _{DS} = -5 V			-1.5		
G _{FS}	Forward Transconductance	V _{GS} = -15 V, I _b = -2.9 A		4		S	
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz		350		pF	
C _{oss}	Output Capacitance			260		pF	
C _{rss}	Reverse Transfer Capacitance			100		pF	
SWITCHING CHARACTERISTICS (Note 2)							
t _{D(on)}	Turn - On Delay Time	V _{DD} = -10 V, I _b = -1 A, V _{GEN} = -10 V, R _{GEN} = 6 Ω		9	40	ns	
t _r	Turn - On Rise Time			21	40	ns	
t _{D(off)}	Turn - Off Delay Time			21	90	ns	
t _f	Turn - Off Fall Time			8	50	ns	
Q _g	Total Gate Charge	V _{DS} = -10 V, I _b = -2.9 A, V _{GS} = -10 V		10	25	nC	
Q _{gs}	Gate-Source Charge			1.6		nC	
Q _{gd}	Gate-Drain Charge			3.4		nC	

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Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.2	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -1.25\text{ A}$ (Note 2)		-0.8	-1.3	V
t_r	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_F = -1.25\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$			100	ns

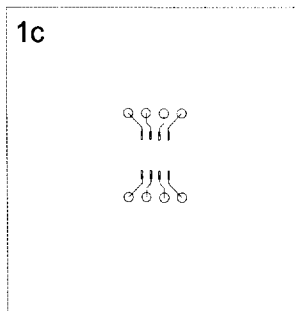
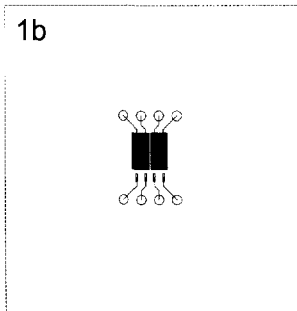
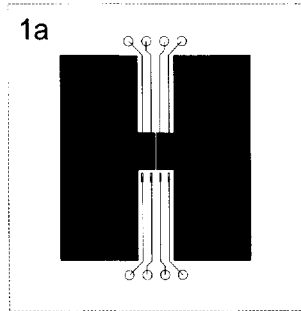
Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

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Typical Electrical Characteristics

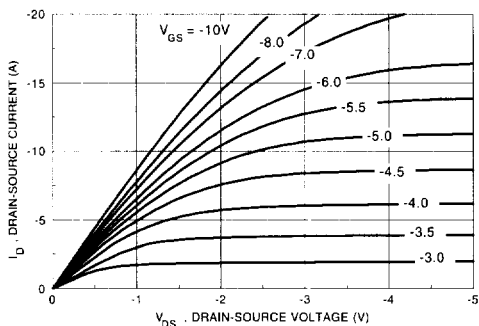


Figure 1. On-Region Characteristics.

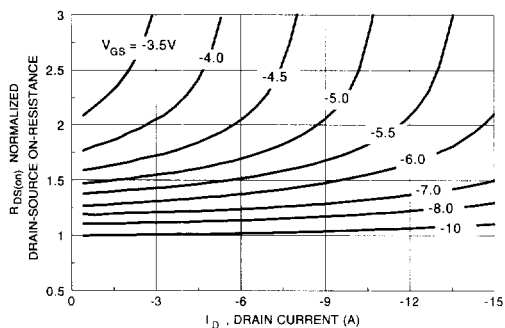


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

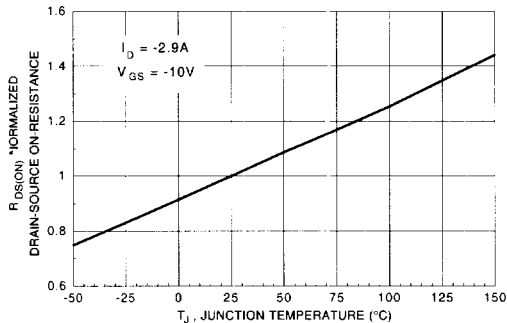


Figure 3. On-Resistance Variation with Temperature.

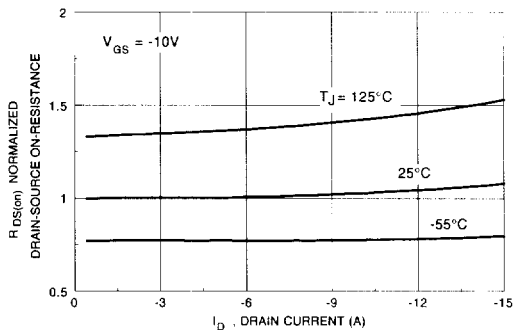


Figure 4. On-Resistance Variation with Drain Current and Temperature.

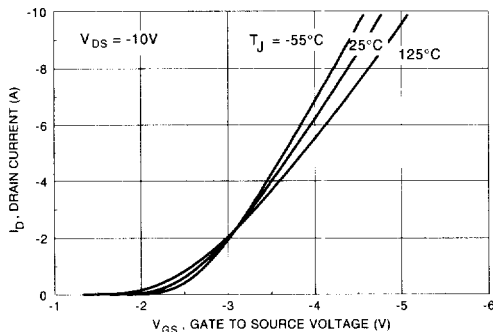


Figure 5. Transfer Characteristics.

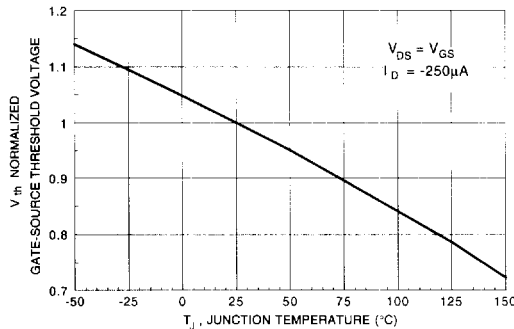


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

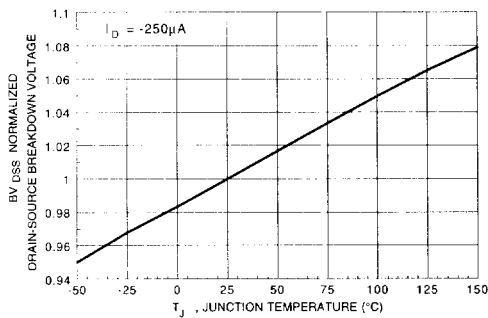


Figure 7. Breakdown Voltage Variation with Temperature.

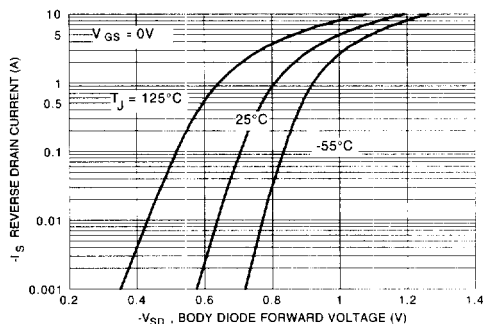


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

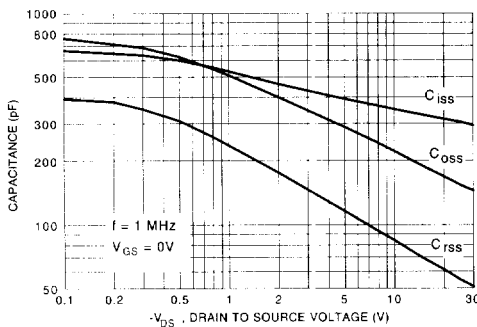


Figure 9. Capacitance Characteristics.

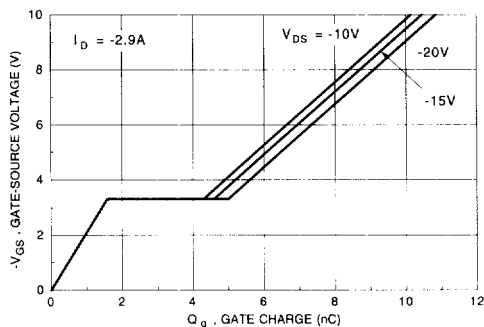


Figure 10. Gate Charge Characteristic.

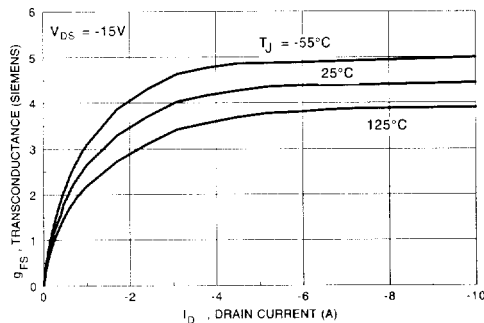


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

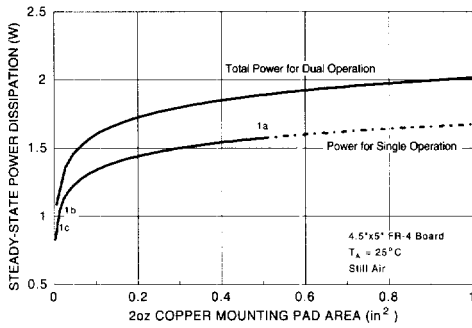


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

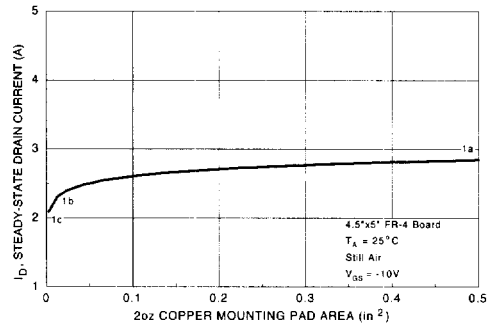


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

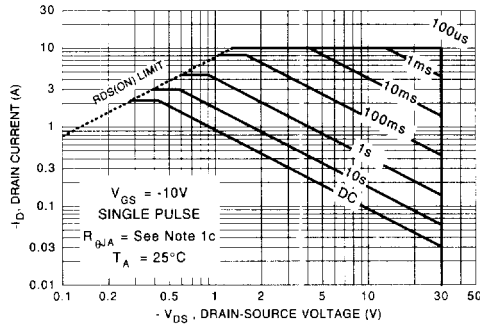


Figure 14. Maximum Safe Operating Area.

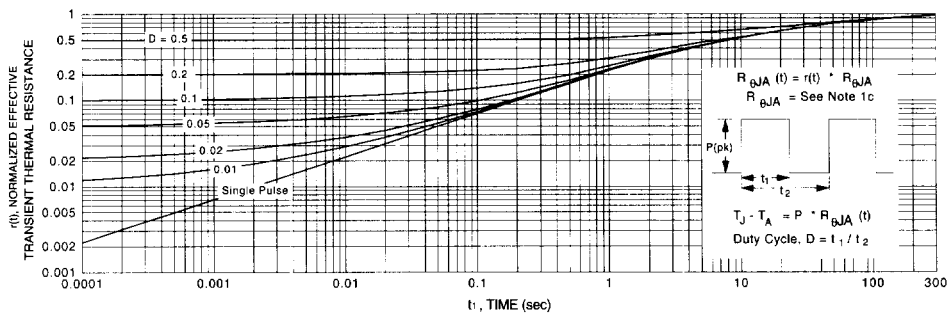


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.