National Semiconductor

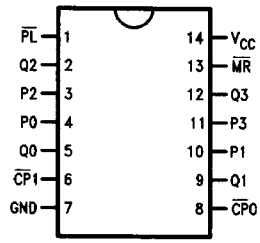
DM74197
Presettable Binary Counters

General Description

The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The '197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH.

Connection Diagram

Dual-In-Line Package



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Order Number DM74197N
See NS Package Number N14A

Pin Names	Description
$\overline{CP}0$	÷2 Section Clock Input (Active Falling Edge)
$\overline{CP}1$	÷8 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0	÷2 Section Output*
Q1–Q3	÷8 Section Outputs

*Q0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}1$ input.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74197			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.25	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$	10 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$	0 0			ns
t_w (H)	$\overline{CP0}$ Pulse Width HIGH	20			ns
t_w (H)	$\overline{CP1}$ Pulse Width HIGH	30			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	15			ns
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP_n}$	20			ns
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP_n}$	20			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 5.5V, $\overline{CP_1}$			1	mA
		V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−18		−57	mA
I_{CC}	Supply Current	V_{CC} = Max, All Inputs = GND			59	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

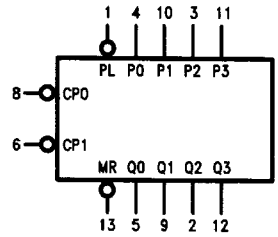
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	C_L = 15 pF, R_L = 400Ω		Units
		Min	Max	
f_{max}	Maximum Count Frequency at $\overline{CP0}$	50		MHz
f_{max}	Maximum Count Frequency at $\overline{CP1}$	25		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP0}$ to Q0		12 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q1		18 21	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q2		36 42	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q3		54 63	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		24 38	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		33 36	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		37	ns

Logic Symbol



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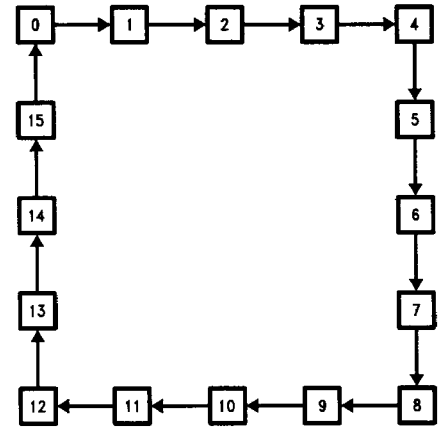
V_{CC} = Pin 14
GND = Pin 7

Mode Selection Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n Forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

÷ 16 State Diagram



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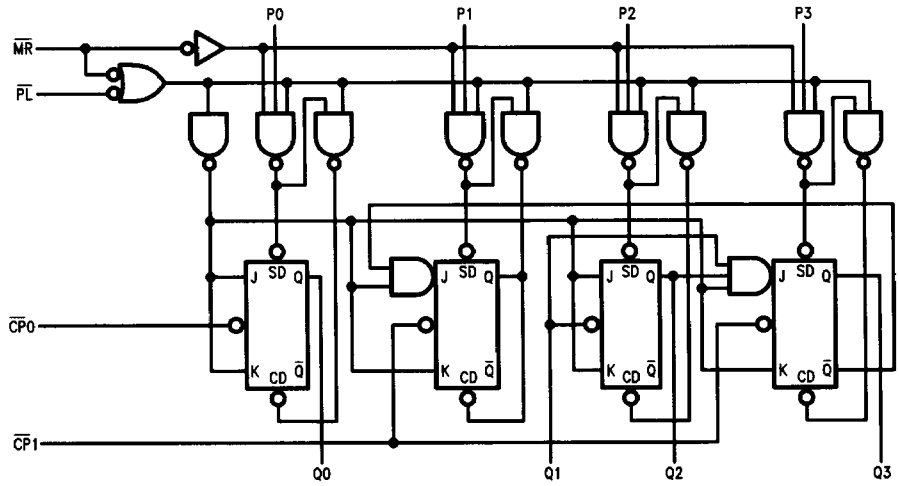
Logic Diagram



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