Custom Clock Synthesizer

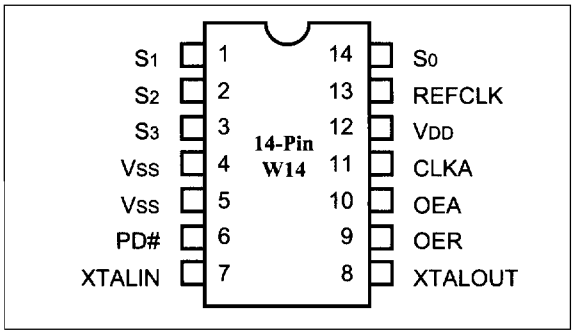
Features

- Single PLL clock synthesizer provides clocking requirements at a very low jitter rate competitive with crystal can oscillators
- Excellent signal quality:
  - Minimal undershoot, ringback, and overshoot
  - Nearly perfect 50% duty cycle
- 1-32 MHz input reference frequency
- Uses a low-cost crystal
- Up to 16 user-selectable output frequencies
- Output frequencies from 2 MHz to 100 MHz at 3.3V
- Output Enable and Power Down function
- ±250ps jitter
- 3.3V operation
- Available in 8,14,16-pin SOIC packages (W14)

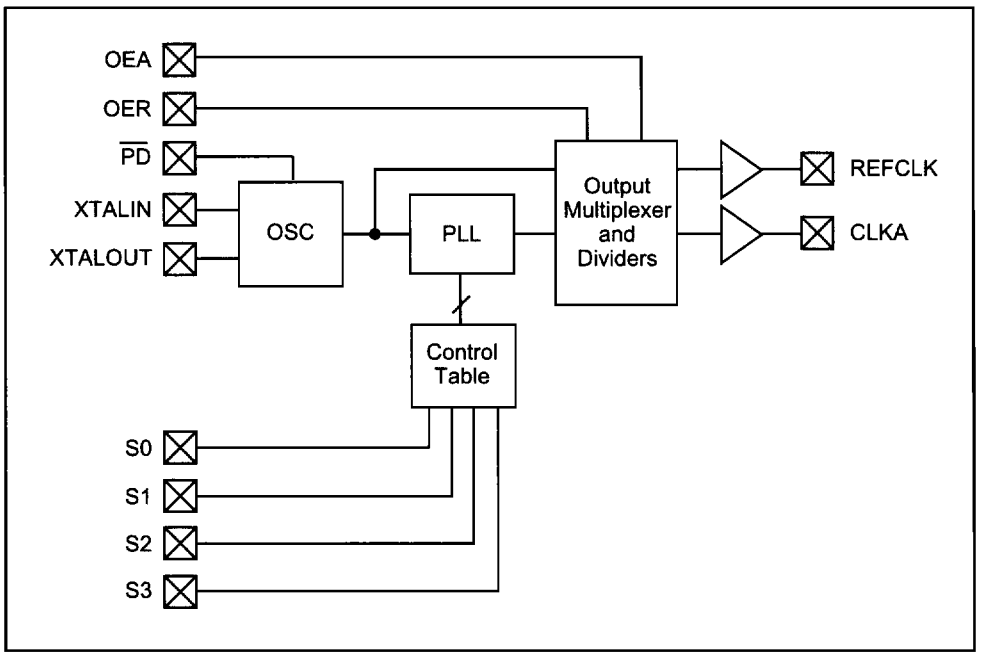
Description

The PI6C2907 is a very low jitter Custom Clock Synthesizer chip that generates multiple system clocks at different frequencies from a single reference frequency input. The PI6C2907 can be used in a wide variety of applications - from graphics to PC motherboards to disk drives. Any application that requires more than one clock frequency can benefit from using this clock synthesizer. The PI6C2907 is compatible with all industry standard 9107 and 9108 clock synthesizers.

Pin Configuration



Block Diagram



Pin Description

Name	Option 14-Pin SOIC Pin Number	Description
S1	1	Frequency select (CLKA) (Internal pull-up resistor to VDD)
S2	2	Frequency select (CLKA) (Internal pull-up resistor to VDD)
S3	3	Frequency select (CLKA) (Internal pull-up resistor to VDD)
Vss	4	Ground
Vss	5	Ground
PD#	6	Power down (active LOW) (Internal pull-up resistor to VDD)
XTALIN[2]	7	Reference crystal input
XTALOUT[2,3]	8	Reference crystal feedback
OEB	9	CLKB output enable (active HIGH) (Internal pull-up resistor to VDD)
OEA	10	CLKA output enable (active HIGH) (Internal pull-up resistor to VDD)
CLKA	6	Clock output
VDD	12	Voltage Supply
REFCLK	13	Reference clock output
S0	14	Frequency select (CLKA) (Internal pull-up resistor to VDD)

Frequency Table

Input Frequency (MHz)				25	Input Frequency (MHz)				25
Select Pins				Output Frequency (MHz)	Select Pins				Output Frequency (MHz)
S3	S2	S1	S0	CLKA	S3	S2	S1	S0	CLKA
0	0	0	0	80.0	1	0	0	0	64.0
0	0	0	1	78.0	1	0	0	1	62.0
0	0	1	0	76.0	1	0	1	0	60.0
0	0	1	1	74.0	1	0	1	1	N/A
0	1	0	0	72.0	1	1	0	0	N/A
0	1	0	1	70.0	1	1	0	1	20.0
0	1	1	0	68.0	1	1	1	0	40.0
0	1	1	1	66.0	1	1	1	1	N/A

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature (Non-condensing)	–65°C to +150°C
Junction Temperature	+150°C
Maximum Soldering Temperature (10 seconds)	+260°C
Supply Voltage	–0.5V to +7.0V
Input Voltage	–0.5V to V_{DD} +0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Conditions (5)

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage, 3.3V Operation	3.0	3.7	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Maximum Capacitive Load		15	pF

Electrical Characteristics (V_{DD} = 3.0V to 3.7V, T_A = 0° to 70°C)

Symbol	Description	Test Condition	Min.	Max.	Units
V_{IH}	High-Level Input Voltage	Except Crystal Inputs	0.7*V_{DD}		V
V_{IL}	Low-Level Input Voltage	Except Crystal Inputs		0.2*V_{DD}	
V_{OH}(6)	High-Level Output Voltage	CLKA, I_{OH} = -5mA	0.85*V_{DD}		
V_{OL}(6)	Low-Level Output Voltage	CLKA, I_{OH} = 6mA		0.1*V_{DD}	
I_{OH}(6)	Output High Voltage	V_{OH} = 0.7*V_{DD}		-10	mA
I_{OL}(6)	Output Low Current	V_{OH} = 0.2*V_{DD}	15		
I_{IH}	Input Low Current	V_{IH} = V_{DD}	-2	2	µA
I_{IL}	Input Leakage Current	V_{IL} = 0V		10	
I_{DD}	Power Supply Current	PD HIGH, CLKA = 50 MHz		13	mA
I_{DD}	Power Supply Current	PD LOW, Logic Inputs LOW		40	µA
I_{DD}	Power Supply Current	PD LOW, Logic Inputs HIGH		12	
R_{PU}(6)	Pull-up Resistor	V_{IN} = V_{DD} -1.0V		1.3	MΩ

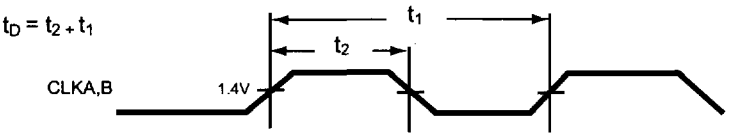
Notes:
5. Electrical parameters are guaranteed with these operating conditions.
6. Guaranteed by design, not 100% tested in production.

Switching Characteristics at 3.3V

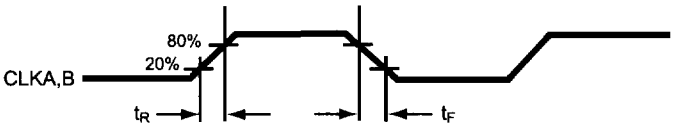
Parameter	Output	Description	Test Conditions	Min.	Max.	Units
t_R	CLKA	Output Rise Time 20% to 80%	15pF Load		3.5	ns
t_F	CLKA	Output Fall Time 80% to 20%V	15pF Load		2.5	
t_D	CLKA	Duty Cycle	15pF Load at 1.4V	45	55	%
F_I	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F_I	XTALIN	Input Frequency	External Input Clock	1	32	
F_O	CLKA	Output Frequency	15pF Load	2.0	100.0	
t_{JIS}	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t_{JIS}	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	
t_{JIS}	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t_{JAB}	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	-250	+250	ps
t_{JAB}	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	-500	+500	
t_{JAB}	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t_{PU}		Power-up Time			18	ms

Switching Waveforms

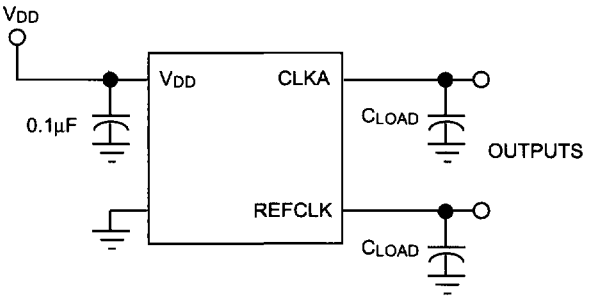
Duty Cycle Timing



All Outputs Rise/Fall Time

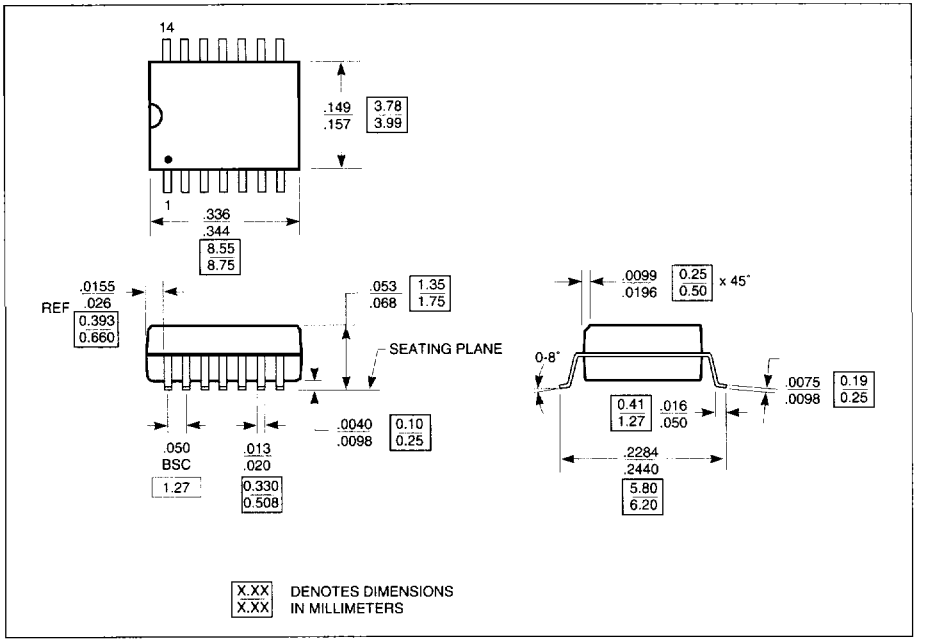


Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

Package Drawing



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2907W	W14	14-Pin SOIC	Commercial