

# 54ACT11853, 74ACT11853 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3474, MARCH 1990—REVISED OCTOBER 1990

- High-Speed Bus Transceivers With Parity Generator/Checker
- Parity-Error-Flag Open-Drain Output
- Register for Storage of the Parity-Error Flag
- Inputs are TTL-Voltage Compatible
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

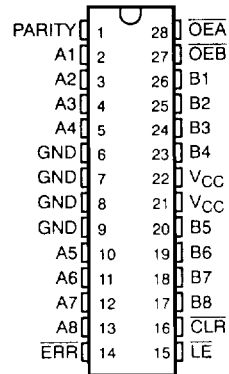
## description

The 'ACT11853 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the  $\overline{ERR}$  output will indicate whether or not an error in the B data has occurred. The output-enable inputs  $\overline{OEA}$  and  $\overline{OEB}$  can be used to disable the device so that the buses are effectively isolated.

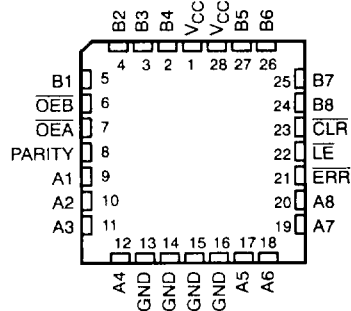
A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity-error flag ( $\overline{ERR}$ ).  $\overline{ERR}$  can be either passed, sampled, stored, or cleared from the latch using the  $\overline{LE}$  and  $\overline{CLR}$  control inputs. The error flag register is cleared with a low pulse on the  $\overline{CLR}$  input. When both  $\overline{OEA}$  and  $\overline{OEB}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54ACT11853 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74ACT11853 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

54ACT11853 . . . JT PACKAGE  
74ACT11853 . . . DW OR NT PACKAGE  
(TOP VIEW)



54ACT11853 . . . FK PACKAGE  
(TOP VIEW)



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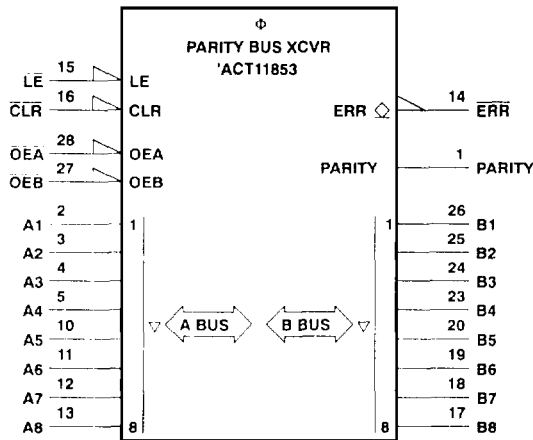
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984.  
Pin numbers shown are for DW, JT, and NT packages.

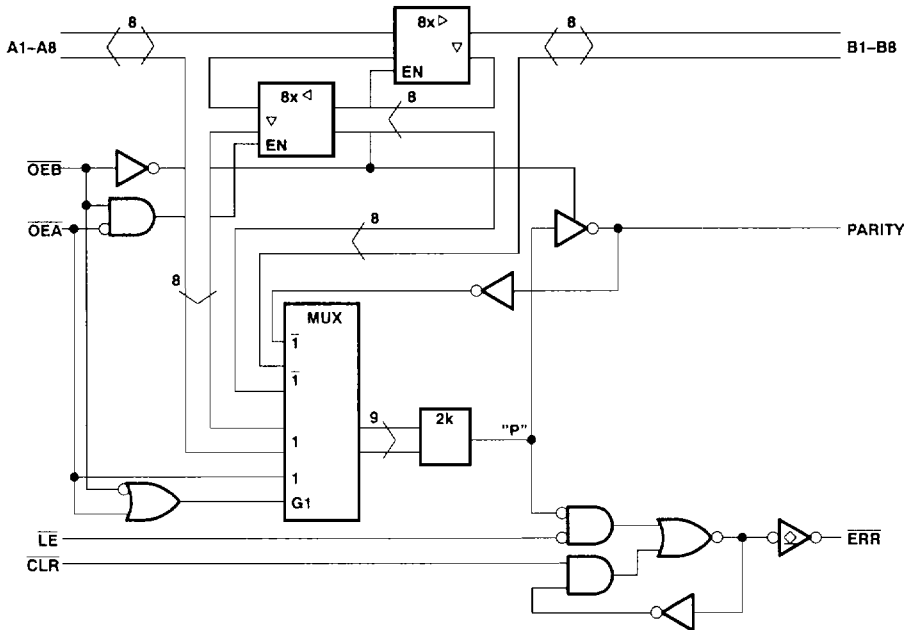
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logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
OE̅B	OE̅A	CLR	LE	A <sub>i</sub> Σ of H's	B <sub>i</sub> <sup>†</sup> Σ of H's	A	B	PARITY	ERR <sup>‡</sup>	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	NC	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation <sup>§</sup> (Parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care

<sup>†</sup> Summation of high-level inputs includes PARITY along with B<sub>i</sub> inputs.

<sup>‡</sup> Output states shown assume the ERR output was previously high.

<sup>§</sup> In this mode, the ERR output, when enabled, shows inverted parity of the A bus.

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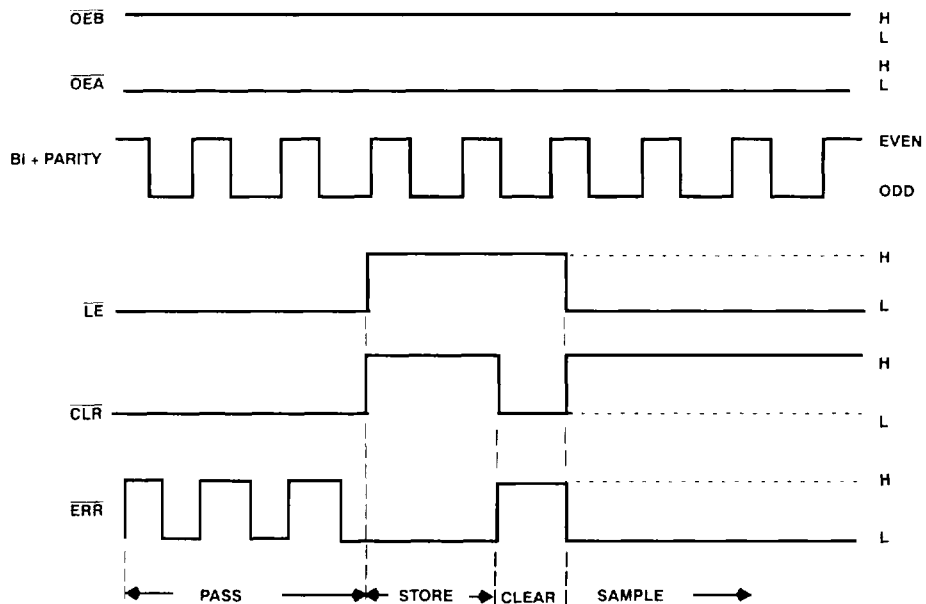
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## error-flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE POINT "P"	OUTPUT PRE-STATE $ERR_{n-1}$ †	OUTPUT $ERR$	FUNCTION
$\overline{LE}$	$\overline{CLR}$				
L	L	L H	X	L H	PASS
L	H	L X H	X L H	L L H	SAMPLE
H	L	X	X	H	CLEAR
H	H	X	L H	L H	STORE

†  $ERR_{n-1}$  represents the state of the  $ERR$  output before any changes at  $\overline{CLR}$ ,  $\overline{LE}$ , or point P.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	– 0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	– 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	± 20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	± 50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	± 50 mA
Continuous current through $V_{CC}$ or GND pins	± 200 mA
Storage temperature range	– 65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

		54ACT11853			74ACT11853			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$I_{OH}$	High-level output current			– 24			– 24	mA
$I_{OL}$	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$	Operating free-air temperature	– 55		125	– 40		85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			54ACT11853		74ACT11853		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	All outputs except ERR	I <sub>OH</sub> = – 50 μA	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		I <sub>OH</sub> = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I <sub>OH</sub> = – 50 mA <sup>†</sup>	5.5 V				3.85				
	I <sub>OH</sub> = – 75 mA <sup>†</sup>	5.5 V						3.85			
V <sub>OL</sub>		I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V				1.65				
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V						1.65			
I <sub>I</sub>	OE <sub>A</sub> , OE <sub>B</sub> , LE, and CLR	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	A or B ports, PARITY <sup>‡</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.5		± 10		± 5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8		160		80	μA
ΔI <sub>CC</sub> <sup>§</sup>		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			0.9		1		1	mA
C <sub>i</sub>	OE <sub>A</sub> , OE <sub>B</sub> , LE, and CLR	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5						pF
C <sub>io</sub>	A or B ports, PARITY	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		12						

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

<sup>§</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

			T <sub>A</sub> = 25°C		54ACT11853		74ACT11853		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	LE high	5		5		5		ns
		LE low	5		5		5		
		CLR low	5		5		5		
t <sub>su</sub>	Setup time, before LE <sub>↓</sub>	Bi and PARITY	14		14		14		ns
		CLR inactive	2		2		2		
t <sub>h</sub>	Hold time, Bi and PARITY after LE <sub>↓</sub>		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS				TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	A to B	C <sub>L</sub> = 50 pF, f = 1 MHz		87	pF
			B to A			60	
		Outputs disabled	A to B			28	
			B to A			8	

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