P54/74FCT161/A (P54/74PCT161/A)
P54/74FCT163/A (P54/74PCT163/A)
SYNCHRONOUS PRESETTABLE BINARY COUNTERS

FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic

- FCT-C speed at 7.2ns max. (Com'l)
  FCT-A speed at 11.0ns max. (Com'l)

- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic

- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics

- ESD protection exceeds 2000V

- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices

- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode

- 64 mA Sink Current (Com'l), 48 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
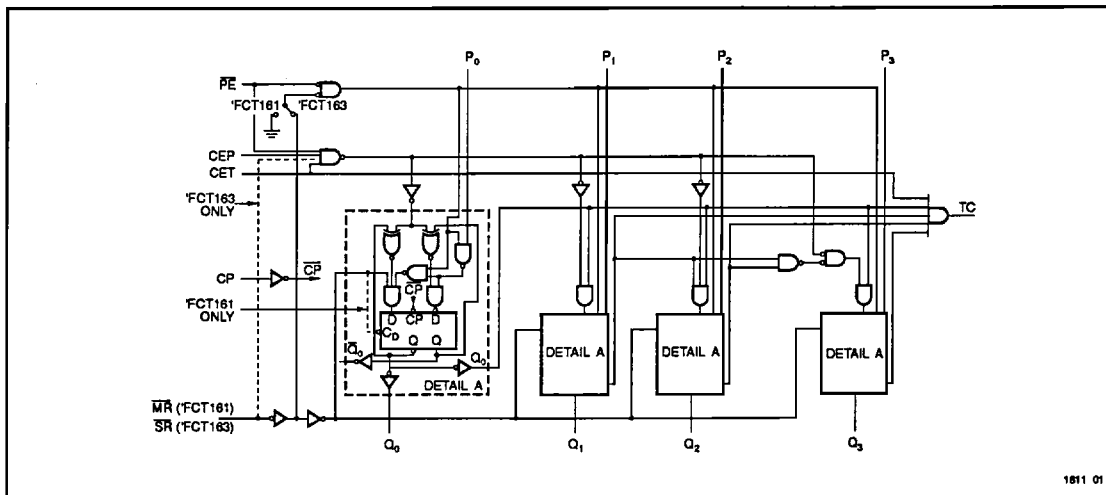
- Manufactured In 0.8 micron PACE Technology™

DESCRIPTION

The 'FCT161 and 'FCT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The 'FCT161 have a asynchronous Master Reset input that override all other inputs and force the outputs LOW. The 'FCT163 have a Synchronous Reset input that override counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

The 'FCT161 and 'FCT163 are manufactured using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths giving 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

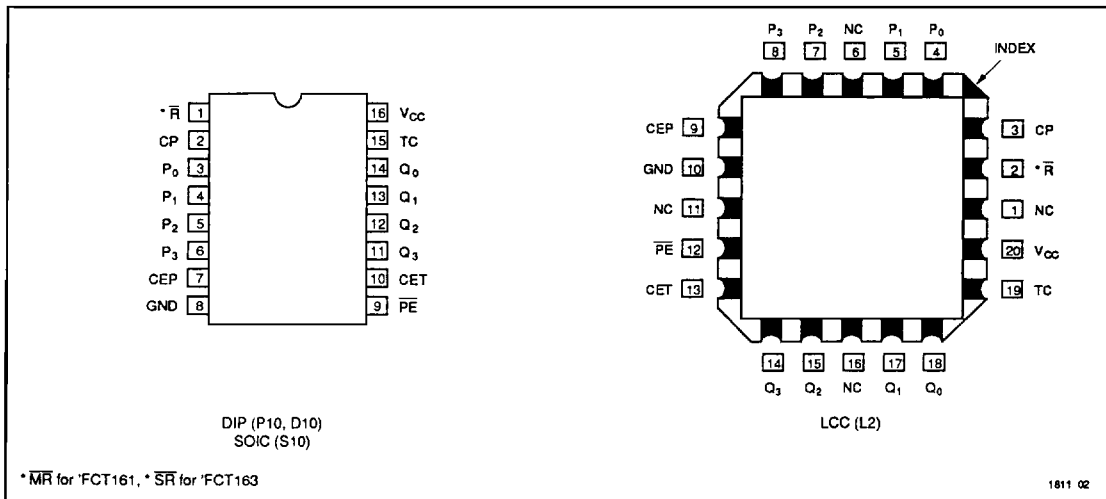*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM

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PIN CONFIGURATIONS

DIP (P10, D10)
SOIC (S10)

LCC (L2)

* $\overline{MR}$ for 'FCT161, * $\overline{SR}$ for 'FCT163

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DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
CEP	Count Enable Parallel Unit
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

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TRUTH TABLE

$\overline{SR}^{(1)}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Incremental)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

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Notes:
1. For 'FCT163 only.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Ambient Temperature Under Bias	−65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	−0.5 to +7.0	V
I_{IN}	Input Current	−30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	−0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	−0.5 to V_{CC} + 0.5	V

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Notes:
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	−55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	Military	2.4			V		
		Commercial	2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			−0.7	−1.2	V	MIN	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V	V_{CC} − 0.2	V_{CC}		V		I_{OH} = −32μA
		Military/Commercial (CMOS)	V_{CC} − 0.2	V_{CC}		V	MIN	I_{OH} = −300μA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = −12mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = −15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} − 0.2V	GND	0.2		V		I_{OL} = 300μA
		Military/Commercial (CMOS)	GND	0.2		V	MIN	I_{OL} = 300μA
		Military (TTL)	0.3	0.5		V	MIN	I_{OL} = 32mA
		Commercial (TTL)	0.3	0.5		V	MIN	I_{OL} = 48mA
		Commercial (TTL)	0.3	0.5		V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				5	μA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				−5	μA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	μA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current[3]				−5	μA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		−60	−120		mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

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Notes:
1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

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DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions[6]
I_{CC}	Quiescent Power Supply Current (CMOS inputs HIGH)	0.003	0.5	mA	V_{CC} = MAX, f_i = 0, Outputs Open, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_i = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, CEP = CET = $\overline{PE}$ = GND, $\overline{MR}$ = V_{CC} = $\overline{SR}$, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_i = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR}$ = V_{CC} = $\overline{SR}$ $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_i = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR}$ = V_{CC} = $\overline{SR}$ V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_i = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR}$ = V_{CC} = $\overline{SR}$ $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_i = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{MR}$ = V_{CC} = $\overline{SR}$ V_{IN} = 3.4V or V_{IN} = GND

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Notes:
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + $\Delta I_{CC}D_HN_T$ + $I_{CCD}(f_o/2 + f_iN_i)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_o = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.
6. $\overline{MR}$ for 'FCT161T, $\overline{SR}$ for 'FCT163T

AC CHARACTERISTICS

Symbol	Parameter	'FCT161 'FCT163 MIL		'FCT161 'FCT163 COM'L		'FCT161A 'FCT163A MIL		'FCT161A 'FCT163A COM'L		Units	Fig. No.
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP TO Q_n ($\overline{PE}$ Input High)	2.0	11.5	2.0	11.0	2.0	7.5	2.0	7.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP TO Q_N ($\overline{PE}$ Input Low)	2.0	10.0	2.0	9.5	2.0	6.5	2.0	6.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP TO TC	2.0	16.5	2.0	15.0	2.0	10.8	2.0	9.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET TO TC	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ TO Q_n ('FCT161T)	2.0	14.0	2.0	13.0	2.0	9.1	2.0	8.5	ns	1, 6
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ TO TC ('FCT161T)	2.0	12.5	2.0	11.5	2.0	8.2	2.0	7.5	ns	1, 6
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW P_n to CP	5.5	—	5.0	—	4.5	—	4.0	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW P_n to CP	2.0	—	1.5	—	2.0	—	1.5	—	ns	4
$t_{su}(H)$ $t_{su}(L)$	Setup Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	13.5	—	11.5	—	11.5	—	9.5	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_{su}(H)$ $t_{su}(L)$	Setup Time HIGH or LOW CEP or CET to CP	13.0	—	11.5	—	11.0	—	9.5	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW CEP or CET to CP	0	—	0	—	0	—	0	—	ns	4
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0	—	5.0	—	4.0[2]	—	4.0[2]	—	ns	5
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	8.0	—	7.0	—	7.0	—	6.0	—	ns	5
$t_w(L)$	$\overline{MR}$ Pulse Width Low ('FCT161T)	5.0	—	5.0	—	4.0[2]	—	4.0[2]	—	ns	6
t_{REM}	Recovery Time $\overline{MR}$ to CP ('FCT161T)	6.0	—	6.0	—	5.0	—	5.0	—	ns	6

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Note:
1. Minimum limits are guaranteed but not tested on Propagation Delays.

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ORDERING INFORMATION

$$\underset{\text{Temp. Class}}{\underline{\text{PxxFCT}}} \quad \underset{\text{Device type}}{\underline{\text{xxxx}}} \quad \underset{\text{Package}}{\underline{\text{xx}}} \quad \underset{\text{Processing}}{\underline{\text{x}}}$$

Blank	Commercial
M	Military Temperature
MB	MIL-STD-883, Class B

P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier

161	Synchronous Binary Counter with Asynchronous Master Reset
163	Synchronous Binary Counter with Synchronous Reset
161A	Fast Synchronous Binary Counter with Asynchronous Master Reset
163A	Fast Synchronous Binary Counter with Synchronous Reset

74	Commercial
54	Military

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