LOW POWER SCHOTTKY INTEGRATED CIRCUITS

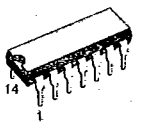
T54LS107A
T74LS107A

PRELIMINARY DATA

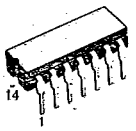
DUAL JK FLIP-FLOP

DESCRIPTION

The T54LS107A/T74LS107A is a Dual JK flip-flop with individual J, K, clock pulse and direct Reset inputs. The HIGH-to-LOW transition of the clock initiates output changes. A LOW signal on CD input overrides the other inputs and makes the Q output LOW. The T54LS/T74LS107A is the same as the T54LS/T54LS73A but has corner power pins.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

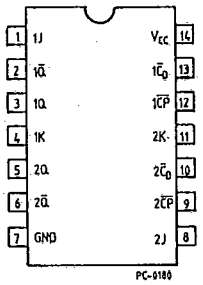
C1
Plastic Chip Carrier

ORDERING NUMBERS:

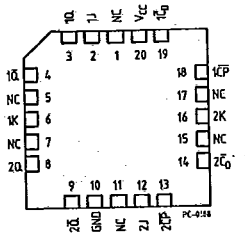
T54LS107A D2	T74LS107A C1
T74LS107A D1	T74LS107A M1
T74LS107A B1	

PIN CONNECTION (top view)

DUAL IN LINE

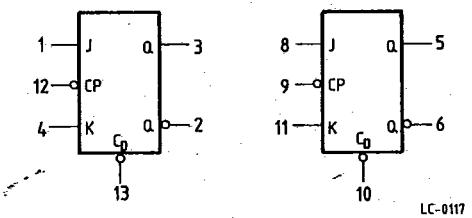


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL



T54LS107A
T74LS107A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS107AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS107AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed Input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed Input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.5				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current	J, K Clear Clock			20 60 80	V_{CC} = MAX, V_{IN} = 2.7V		μA
		J, K Clear Clock			0.1 0.3 0.4	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current	J, K Clear,Clock			−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				6.0	V_{CC} = MAX		mA

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

T54LS107A
T74LS107A

AC CHARACTERISTICS: $T_A = 25°C$

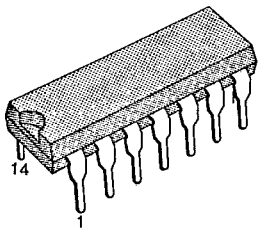
Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
f_{MAX}	Maximum Clock Frequency	30	45		$V_{CC} = 5.0V$ $C_L = 15pF$	MHz
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output		15 15	20 20		ns

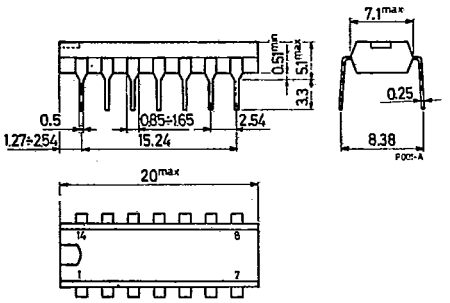
AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
t_W	Clock Pulse Width	20			$V_{CC} = 5.0V$	ns
t_W	Set Pulse Width	25				ns
t_s	Set-Up Time	20				ns
t_h	Hold Time	0				ns

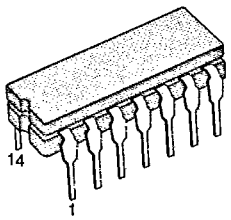
Packages

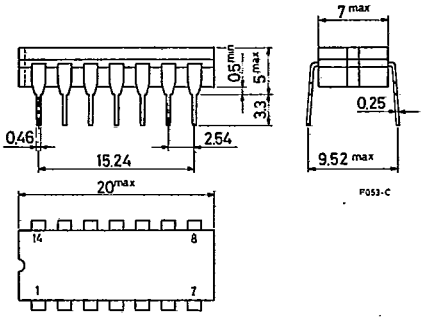
14-LEAD PLASTIC DIP



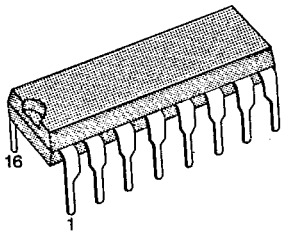


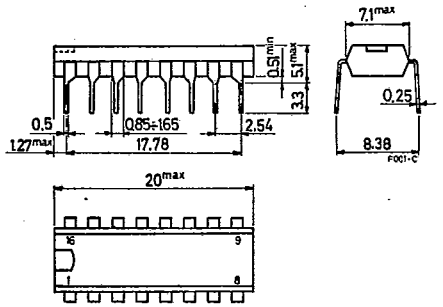
14-LEAD CERAMIC DIP





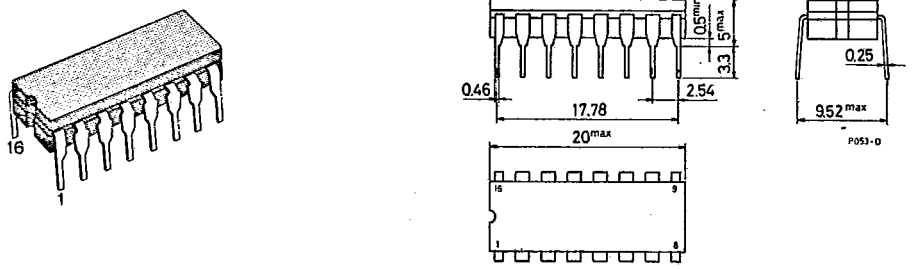
16-LEAD PLASTIC DIP





Packages

16-LEAD CERAMIC DIP



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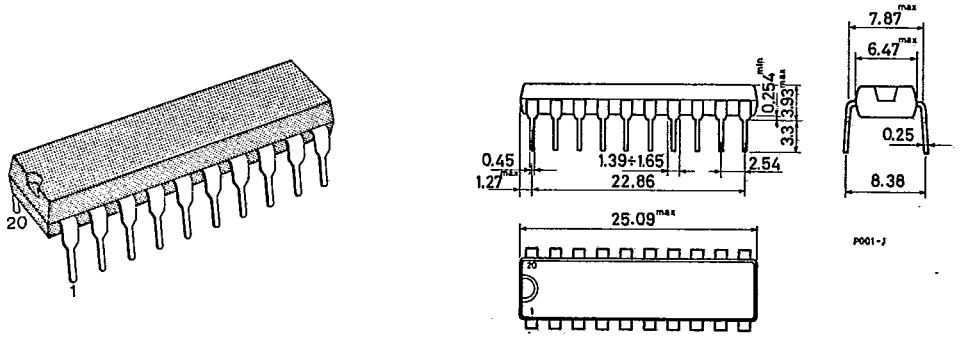

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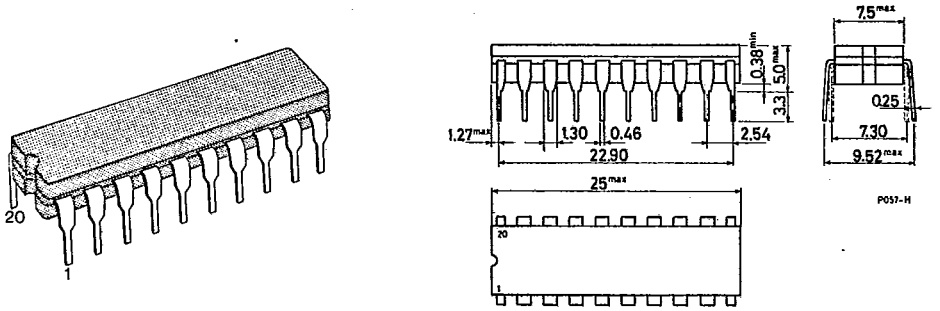
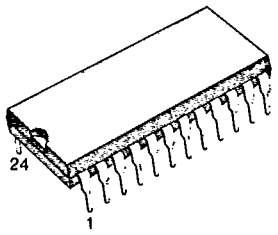
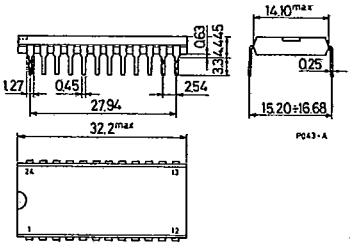


Packages

24-LEAD PLASTIC DIP





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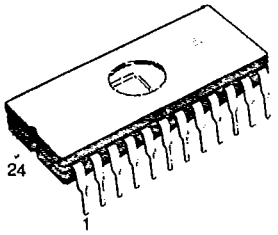
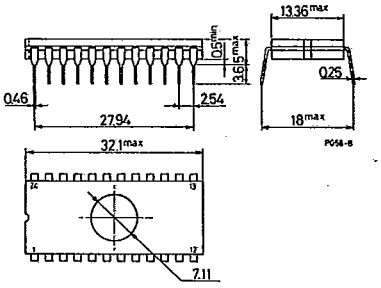
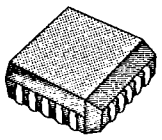
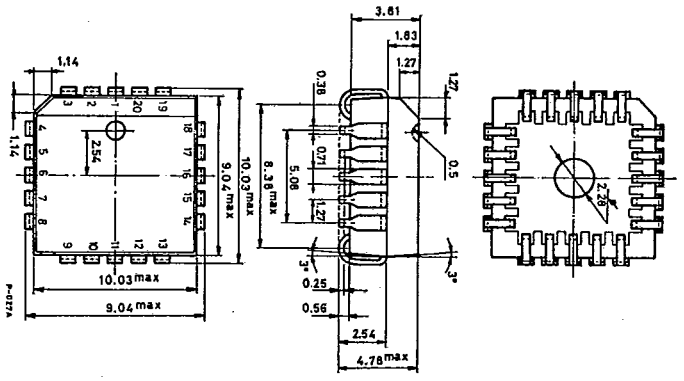




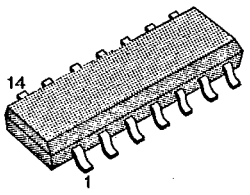
CHIP CARRIER 20 LEAD PLASTIC

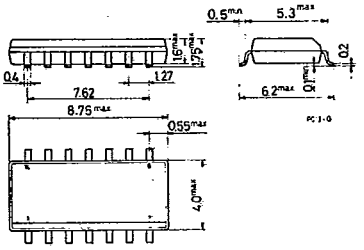




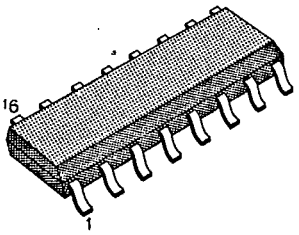
Packages

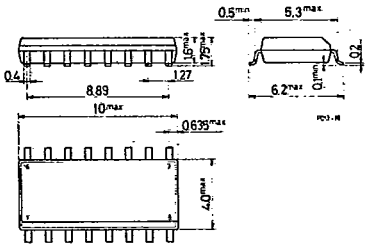
14-LEAD PLASTIC DIP MICROPACKAGE





16-LEAD PLASTIC DIP MICROPACKAGE





NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages.
The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propogation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.