



**MT5C1601**  
**16K x 1 SRAM**

# SRAM

# 16K x 1 SRAM

**5 VOLT SRAM**

## FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with  $\overline{CE}$  option
- All inputs and outputs are TTL-compatible

## OPTIONS

- Timing
  - 9ns access
  - 10ns access
  - 12ns access
  - 15ns access
  - 20ns access
  - 25ns access

## MARKING

- |             |     |
|-------------|-----|
| 9ns access  | - 9 |
| 10ns access | -10 |
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
- 
- |                       |      |
|-----------------------|------|
| • Packages            |      |
| Plastic DIP (300 mil) | None |
| Plastic SOJ (300 mil) | DJ   |
- 
- |                     |   |
|---------------------|---|
| • 2V data retention | L |
|---------------------|---|
- 
- |                              |      |
|------------------------------|------|
| • Temperature                |      |
| Commercial (0°C to +70°C)    | None |
| Industrial (-40°C to +85°C)  | IT   |
| Automotive (-40°C to +125°C) | AT   |
| Extended (-55°C to +125°C)   | XT   |
- 
- Part Number Example: MT5C1601DJ-12 L

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

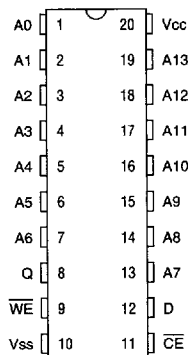
## GENERAL DESCRIPTION

The MT5C1601 is organized as a 16384 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

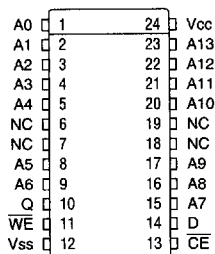
For flexibility in high-speed memory applications, Micron offers chip enable ( $\overline{CE}$ ) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

## PIN ASSIGNMENT (Top View)

### 20-Pin DIP (SA-1)



### 24-Pin SOJ (SD-1)

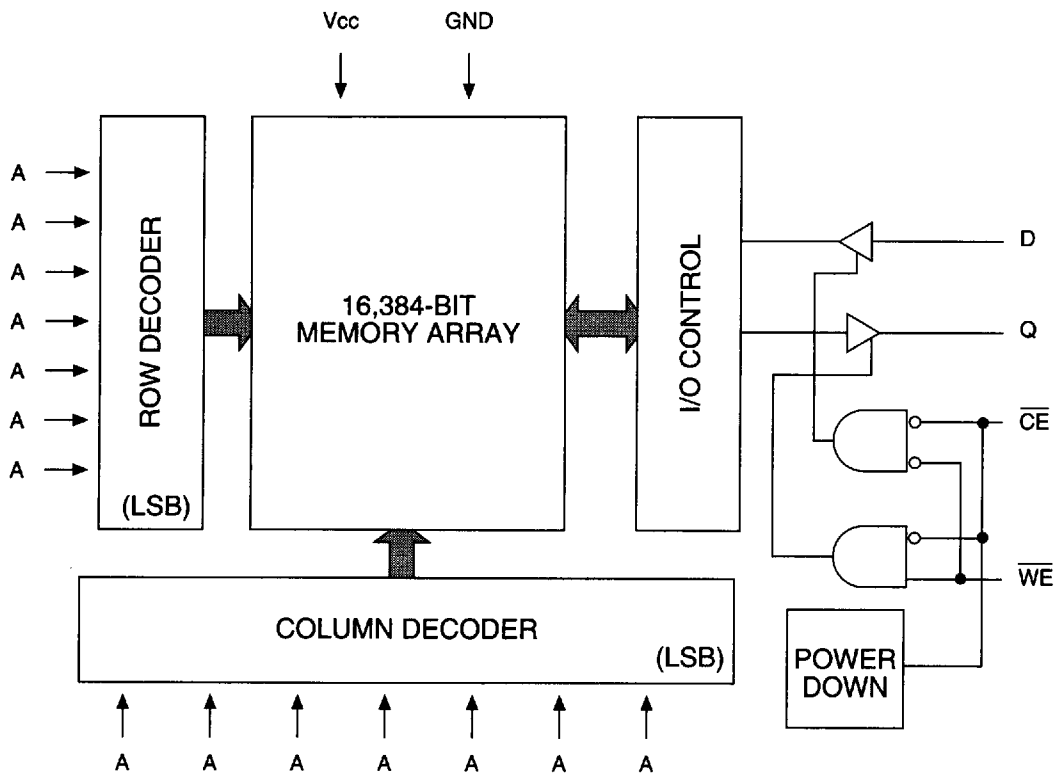


Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

**FUNCTIONAL BLOCK DIAGRAM**

**5 VOLT SRAM**



**TRUTH TABLE**

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'TCARE	HIGH-Z	STANDBY
READ	L	H	DON'TCARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE



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**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss .....-1V to +7V  
 Storage Temperature (plastic) .....-55°C to +150°C  
 Power Dissipation .....1W  
 Short Circuit Output Current .....50mA  
 Voltage on Any Pin Relative to Vss .....-1V to Vcc +1V

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**5 VOLT SRAM**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤ T<sub>A</sub> ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.2	Vcc +1	V	1
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ Vcc	I <sub>LI</sub>	-5	5	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V <sub>OUT</sub> ≤ Vcc	I <sub>LO</sub>	-5	5	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-9	-10	-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/ 'RC outputs open	I <sub>CC</sub>	125	190	185	175	165	140	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/ 'RC outputs open	I <sub>SB1</sub>	22	60	50	45	40	35	35	mA	13
	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V; f = 0	I <sub>SB2</sub>	0.5	3	3	3	3	3	5	mA	13

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C; f = 1 MHz Vcc = 5V	C <sub>I</sub>	7	pF	4
Output Capacitance		C <sub>O</sub>	7	pF	4

**MICRON****MT5C1601**  
**16K x 1 SRAM****ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Note 5) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 5\text{V} \pm 10\%$ )**5 VOLT SRAM**

DESCRIPTION	SYM	-9		-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>															
READ cycle time	<sup>t</sup> RC	9		10		12		15		20		25		ns	
Address access time	<sup>t</sup> AA		9		10		12		15		20		25	ns	
Chip Enable access time	<sup>t</sup> ACE		9		9		10		12		15		20	ns	
Output hold from address change	<sup>t</sup> OH	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	<sup>t</sup> LZCE	2		2		2		2		2		2		ns	7, 14
Chip disable to output in High-Z	<sup>t</sup> HZCE		5		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	<sup>t</sup> PU	0		0		0		0		0		0		ns	
Chip disable to power-down time	<sup>t</sup> PD		9		10		12		15		20		25	ns	
<b>WRITE Cycle</b>															
WRITE cycle time	<sup>t</sup> WC	9		10		12		15		20		25		ns	
Chip Enable to end of write	<sup>t</sup> CW	7		8		10		12		15		20		ns	
Address valid to end of write	<sup>t</sup> AW	7		8		10		12		15		20		ns	
Address setup time	<sup>t</sup> AS	0		0		0		0		0		0		ns	
Address hold from end of write	<sup>t</sup> AH	0		0		0		0		0		0		ns	
WRITE pulse width	<sup>t</sup> WP	6		7		8		10		12		15		ns	
Data setup time	<sup>t</sup> DS	5		6		7		8		9		10		ns	
Data hold time	<sup>t</sup> DH	1		1		1		1		1		1		ns	
Write disable to output in Low-Z	<sup>t</sup> LZWE	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	<sup>t</sup> HZWE		4		5		5		6		8		8	ns	6, 7


**MT5C1601**  
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**INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)**

The following specifications are to be used for Industrial Temperature (IT) MT5C1601 SRAMs.

 $(-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C})$ 
**5 VOLT SRAM**

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-10	-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{\text{CE}} \leq V_{IL}$ ; $V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/\text{tRC}$ outputs open	I <sub>CC</sub>	195	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{\text{CE}} \geq V_{IH}$ ; $V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/\text{tRC}$ outputs open	I <sub>SB1</sub>	60	50	45	40	40	mA	13
	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$ ; $V_{CC} = \text{MAX}$ $V_{IN} \leq V_{SS} + 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$ ; $f = 0$	I <sub>SB2</sub>	5	5	5	5	5	mA	13

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Data Retention Current	$\overline{\text{CE}} \geq (V_{CC} - 0.2\text{V})$ $V_{IN} \geq (V_{CC} - 0.2\text{V})$ or $\leq 0.2\text{V}$	$V_{CC} = 2\text{V}$	I <sub>CCDR</sub>	130	300	$\mu\text{A}$ 14
		$V_{CC} = 3\text{V}$	I <sub>CCDR</sub>	210	550	$\mu\text{A}$ 14

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.

 $(\text{Notes } 5, 14) (-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C})$ 

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>											
Output hold from address change	t <sub>OH</sub>	2		2		2		2		ns	
Chip Enable to output in Low-Z	t <sub>LZCE</sub>	1		1		1		1		ns	7
<b>WRITE Cycle</b>											
Write disable to output in Low-Z	t <sub>LZWE</sub>	1		1		1		1		ns	7



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**AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)**

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1601 SRAMs. (-40°C ≤ T<sub>A</sub> ≤ 125°C - AT) (-55°C ≤ T<sub>A</sub> ≤ 125°C - XT)

DESCRIPTION	CONDITIONS	SYMBOL	MAX				UNITS	NOTES
			-12	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/{}^1\text{RC}$ outputs open	I <sub>CC</sub>	185	175	150	140	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ $f = \text{MAX} = 1/{}^1\text{RC}$ outputs open	I <sub>SB1</sub>	50	45	40	40	mA	13
	$\overline{CE} \geq V_{CC} - 0.2\text{V}; V_{CC} = \text{MAX}$ $V_{IN} \leq V_{SS} + 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}; f = 0$	I <sub>SB2</sub>	5	5	5	5	mA	13

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2\text{V})$ $V_{IN} \geq (V_{CC} - 0.2\text{V})$ or $\leq 0.2\text{V}$	$V_{CC} = 2\text{V}$	I <sub>CCDR</sub>	130	300	μA	14
		$V_{CC} = 3\text{V}$	I <sub>CCDR</sub>	210	550	μA	14

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

Refer to commercial temperature timing parameters for specifications not listed here.

(Notes 5, 14) (-40°C ≤ T<sub>A</sub> ≤ 125°C; -55°C ≤ T<sub>A</sub> ≤ 125°C; V<sub>CC</sub> = 5V ±10%)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>											
Output hold from address change	<sup>t</sup> OH	2		2		2		2		ns	
Chip Enable to output in Low-Z	<sup>t</sup> LZCE	1		1		1		1		ns	7
<b>WRITE Cycle</b>											
Write disable to output in Low-Z	<sup>t</sup> LZWE	1		1		1		1		ns	7



MT5C1601  
16K x 1 SRAM

**AC TEST CONDITIONS**

Input pulse levels .....	V <sub>SS</sub> to 3.0V
Input rise and fall times .....	3ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2

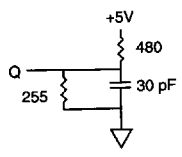


Fig. 1 OUTPUT LOAD EQUIVALENT

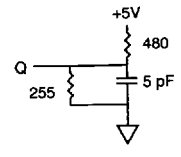


Fig. 2 OUTPUT LOAD EQUIVALENT

**5 VOLT SRAM**

**NOTES**

- All voltages referenced to V<sub>SS</sub> (GND).
- 3V for pulse width < t<sub>RC</sub>/2ns.
- I<sub>CC</sub> is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t<sub>HZCE</sub> and t<sub>HZWE</sub> are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZWE</sub> is less than t<sub>LZWE</sub>.
- $\overline{WE}$  is HIGH for READ cycle.
- Device is continuously selected. All chip enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t<sub>RC</sub> = Read Cycle Time.
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 5V, 25°C and 15ns cycle time.
- Typical currents are measured at 25°C.

**DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)**

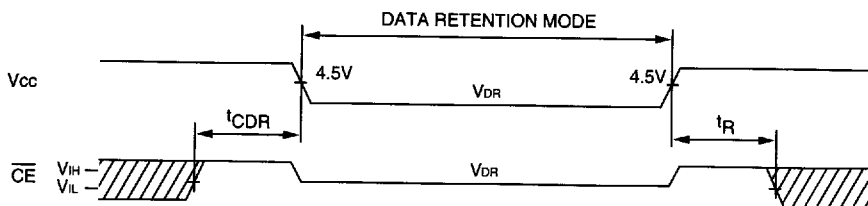
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V <sub>CC</sub> for Retention Data			V <sub>DR</sub>	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V <sub>CC</sub> = 2V	I <sub>CCDR</sub>		130	300	μA	14
		V <sub>CC</sub> = 3V	I <sub>CCDR</sub>		210	400	μA	14
Chip Deselect to Data Retention Time			t <sub>CDR</sub>	0			ns	4
Operation Recovery Time			t <sub>R</sub>	t <sub>RC</sub>			ns	4, 11



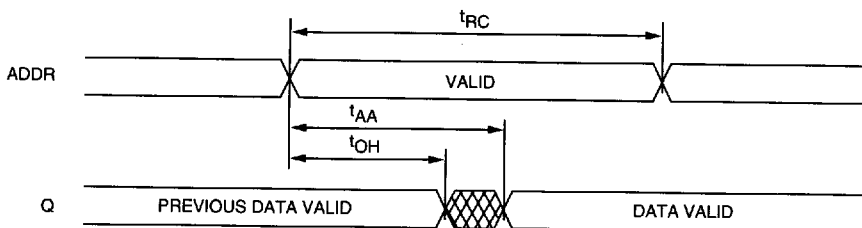
MT5C1601  
16K x 1 SRAM

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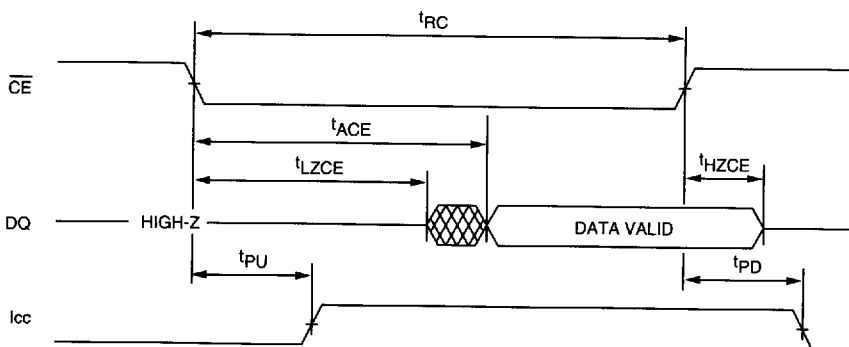
LOW V<sub>CC</sub> DATA RETENTION WAVEFORM



READ CYCLE NO. 1 8, 9



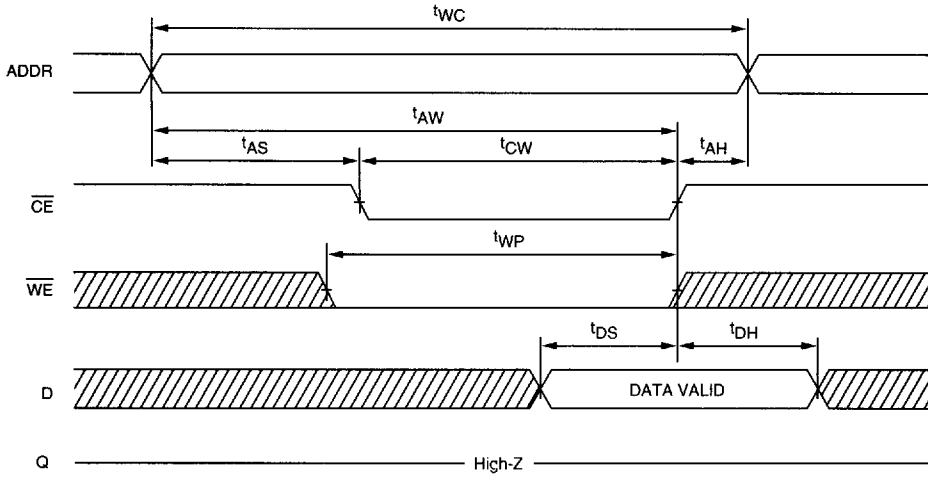
READ CYCLE NO. 2 7, 8, 10



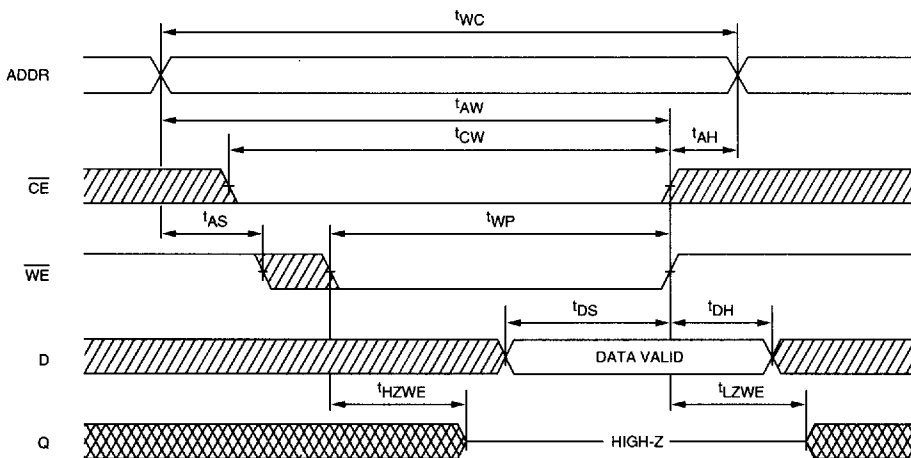
DON'T CARE  
 UNDEFINED





**WRITE CYCLE NO. 1**<sup>12</sup>  
(Chip Enable Controlled)



**WRITE CYCLE NO. 2**<sup>7, 12</sup>  
(Write Enable Controlled)



 DON'T CARE  
 UNDEFINED