NEC

MOS INTEGRATED CIRCUIT
μPD431000A

1M-BIT CMOS STATIC RAM
128K-WORD BY 8-BIT

Description

The μPD431000A is a high speed, low power, and 1,048,576 bits (131,072 words × 8 bits) CMOS static RAM.

The μPD431000A has two chip enable pins ($\overline{CE1}$, CE2) to extend the capacity. And battery backup is available. In addition to this, B version is a wide voltage version.

The μPD431000A is packed in 32-pin plastic DIP, 32-pin plastic SOP, and 32-pin plastic TSOP(I).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 150 ns (MAX.)
- Wide voltage range: B version
- 2 V (MIN.) data retention
- Output Enable input for easy application
- Two Chip Enable inputs: $\overline{CE1}$, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Standby supply current μA (MAX.)	Data retention supply current[Note1] μA (MAX.)
μPD431000A-L	70, 85, 100	4.5 to 5.5	0 to 70	100	15
μPD431000A-LL				50	3
μPD431000A-B15	100[Note2], 150	2.7 to 5.5			

Notes 1. $T_A \leq 40$ °C

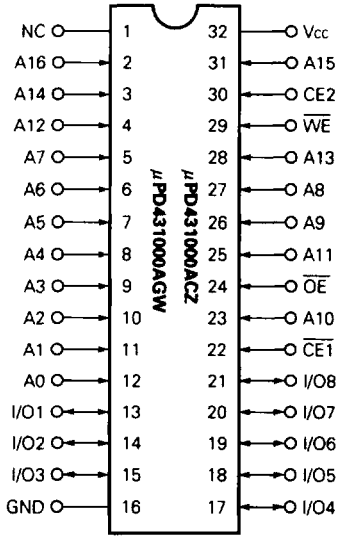
2. V_{CC} = 4.5 to 5.5 V

Ordering Information

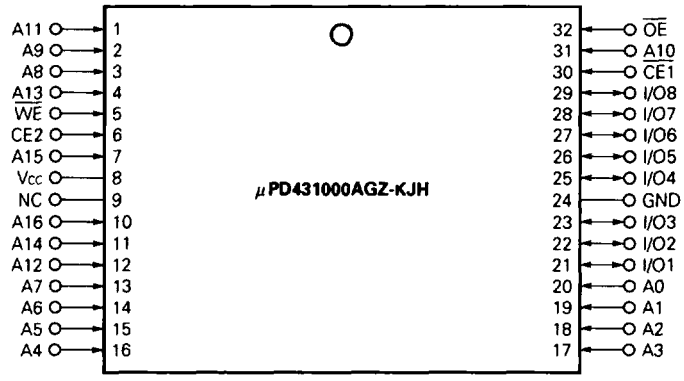
Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD431000ACZ-70L	32-pin Plastic DIP (600 mil)	70	4.5 to 5.5	0 to 70	L Version
μPD431000ACZ-85L		85			
μPD431000ACZ-10L		100			
μPD431000ACZ-70LL		70			LL Version
μPD431000ACZ-85LL		85			
μPD431000ACZ-10LL		100			
μPD431000AGW-70L	32-pin Plastic SOP (525 mil)	70			L Version
μPD431000AGW-85L		85			
μPD431000AGW-10L		100			
μPD431000AGW-70LL		70			LL Version
μPD431000AGW-85LL		85			
μPD431000AGW-10LL		100			
μPD431000AGW-B15		150	2.7 to 5.5		B Version
μPD431000AGZ-70LL-KJH	32-pin Plastic TSOP (I) (8 × 20 mm) (Normal bent)	70	4.5 to 5.5		LL Version
μPD431000AGZ-B15-KJH		150	2.7 to 5.5		B Version
μPD431000AGZ-70LL-KKH	32-pin Plastic TSOP (I) (8 × 20 mm) (Reverse bent)	70	4.5 to 5.5		LL Version
μPD431000AGZ-B15-KKH		150	2.7 to 5.5		B Version

Pin Configuration (Marking side)

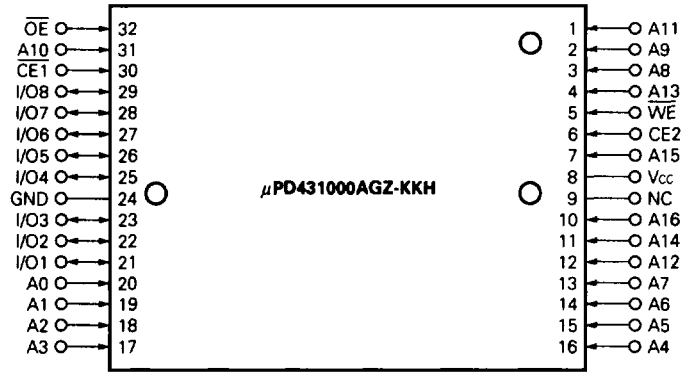
32-pin Plastic DIP (600 mil)
32-pin Plastic SOP (525 mil)



32-pin Plastic TSOP (I) (8 × 20mm)
(Normal bent)

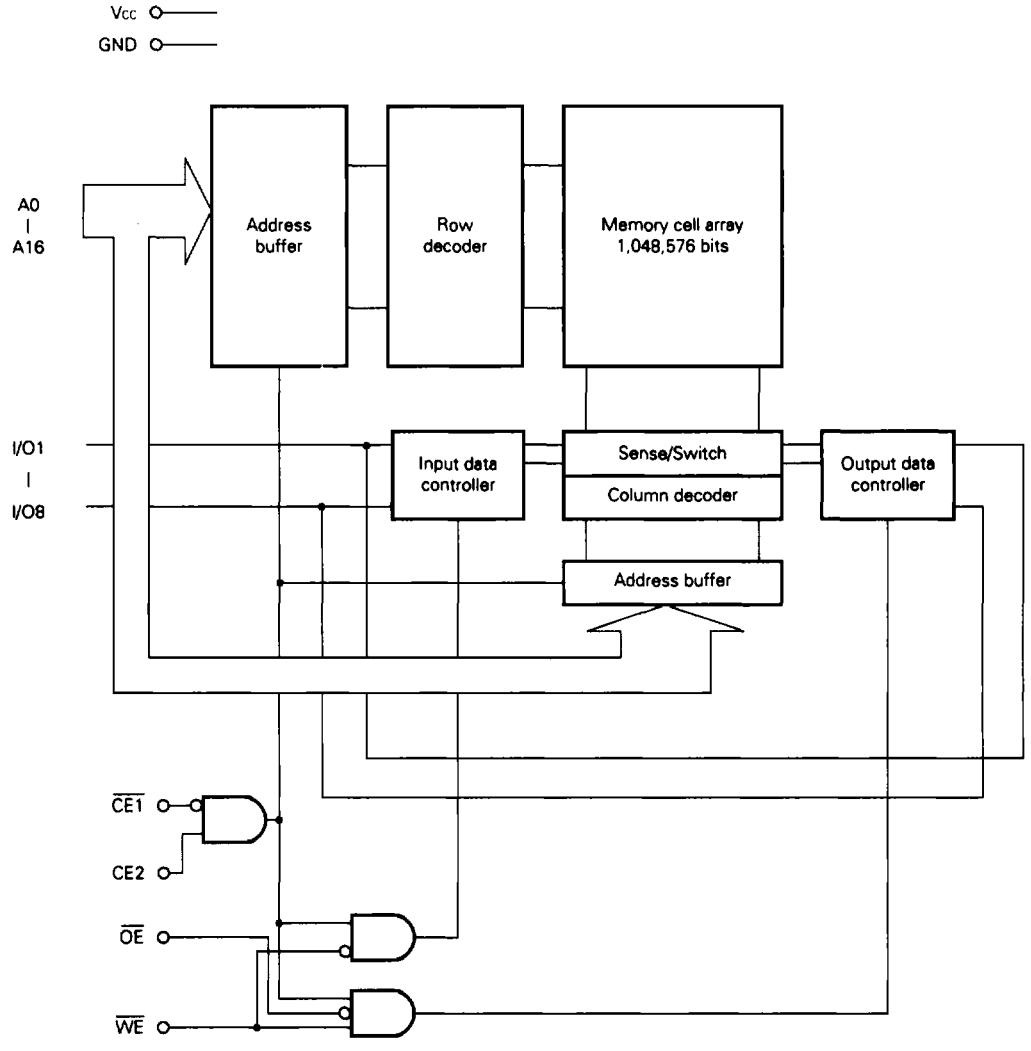


32-pin Plastic TSOP (I) (8 × 20mm)
(Reverse bent)



A0 to A16	: Address inputs
I/O1 to I/O8	: Data inputs/outputs
$\overline{CE1}$, CE2	: Chip Enable 1, 2
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power supply
GND	: Ground
NC	: No connection

Block Diagram



Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×			I_{CCA}
L	H	H	H	Output disable		
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : Don't care

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5[Note] to +7.0	V
Input/Output voltage	V_T	−0.5[Note] to V_{CC} + 0.5	V
Operating ambient temperature	T_A	0 to 70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note −3.0 V (MIN.) (Pulse width 30 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	μPD431000A-L μPD431000A-LL		μPD431000A-B15		Unit
		MIN.	MAX.	MIN.	MAX	
Supply voltage	V_{CC}	4.5	5.5	2.7	5.5	V
High level input voltage	V_{IH}	2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
Low level input voltage	V_{IL}	−0.3[Note]	+0.8	−0.3[Note]	+0.5	V
Operating ambient temperature	T_A	0	70	0	70	°C

Note −3.0 V (MIN.) (Pulse width 30 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	μPD431000A-L			μPD431000A-LL			μPD431000A-B15			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}	−1.0		+1.0	−1.0		+1.0	−1.0		+1.0	μA
Operating supply current	I_{CCA1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} Minimum cycle time $I_{I/O}$ = 0 mA		40	70		40	70			70	mA
		$V_{CC} \leqq 3.3$ V			—			—			20	
	I_{CCA2}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA			15			15			15	
		$V_{CC} \leqq 3.3$ V			—			—			5	
	I_{CCA3}	$\overline{CE1} \leqq 0.2$ V, CE2 ≧ V_{CC} − 0.2 V, Cycle = 1 MHz, $I_{I/O}$ = 0 mA, $V_{IL} \leqq 0.2$ V, $V_{IH} \geqq V_{CC}$ − 0.2 V			10			10			10	
		$V_{CC} \leqq 3.3$ V			—			—			5	
Standby supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}			3			3			3	mA
		$V_{CC} \leqq 3.3$ V			—			—			2	
	I_{SB1}	$\overline{CE1} \geqq V_{CC}$ − 0.2 V, CE2 ≧ V_{CC} − 0.2 V		2	100		1	50		1	50	μA
		$V_{CC} \leqq 3.3$ V			—			—		0.5	25	
	I_{SB2}	CE2 ≦ 0.2 V		2	100		1	50		1	50	
		$V_{CC} \leqq 3.3$ V		—	—		—	—		0.5	25	
High level output voltage	V_{OH1}	I_{OH} = −1.0 mA, $V_{CC} \geqq 4.5$ V	2.4			2.4			2.4			V
		I_{OH} = −0.5 mA	—			—			2.4			
	V_{OH2}	I_{OH} = −0.02 mA	—			—			V_{CC} −0.1			
Low level output voltage	V_{OL1}	I_{OL} = 2.1 mA, $V_{CC} \geqq 4.5$ V			0.4			0.4			0.4	V
		I_{OL} = 1.0 mA			—			—			0.4	
	V_{OL2}	I_{OL} = 0.02 mA			—			—			0.1	

Remark These DC characteristics are in common regardless of package types and access time.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remark 1. V_{IN}: Input voltage

2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

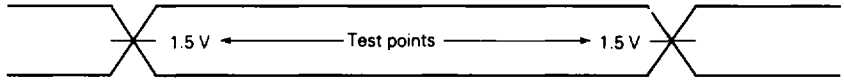
AC Test Conditions

Input waveform (Rise/fall time ≦ 5 ns)

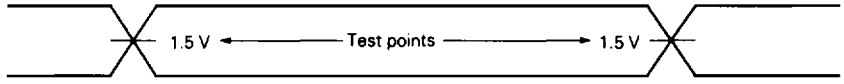
Input pulse levels

0.8 V to 2.2 V : μPD431000A-L, μPD431000A-LL

0.5 V to 2.2 V : μPD431000A-B15



Output waveform



Output load

μPD431000A-B15 : 1TTL + 100 pF

μPD431000A-L, 431000A-LL:

AC characteristics with notes should be measured with the output load shown in **Figure 1** and **Figure 2**.

Figure 1

(For t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH})

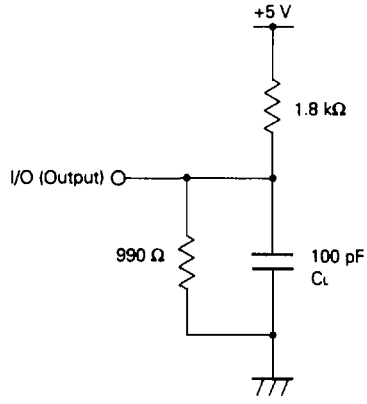
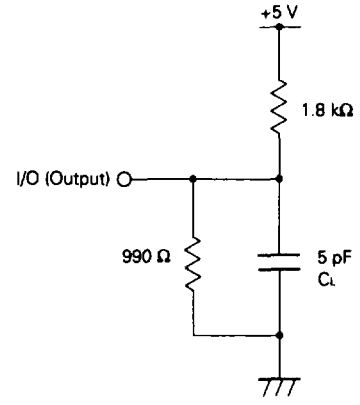


Figure 2

(For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

Read Cycle

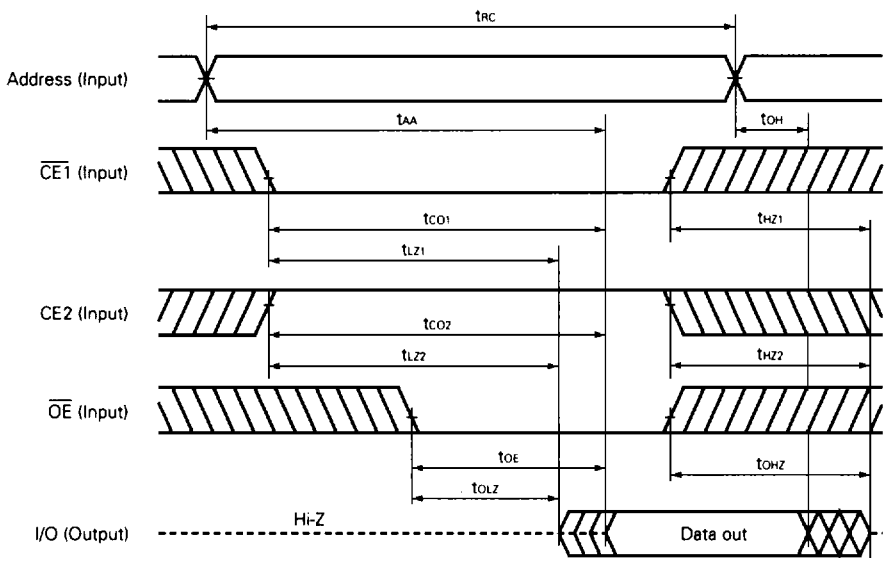
Parameter	Symbol	$V_{CC} \geq 4.5$ V						$V_{CC} \geq 2.7$ V		Unit	Condition
		μPD431000A-70		μPD431000A-85		μPD431000A-10 μPD431000A-B15		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		150		ns	
Address access time	t_{AA}		70		85		100		150	ns	
$\overline{CE1}$ access time	t_{CO1}		70		85		100		150	ns	
CE2 access time	t_{CO2}		70		85		100		150	ns	**Note 1**
$\overline{OE}$ to output valid	t_{OE}		35		45		50		70	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
$\overline{CE1}$ to output in low impedance	t_{LZ1}	10		10		10		10		ns	
CE2 to output in low impedance	t_{LZ2}	10		10		10		10		ns	
$\overline{OE}$ to output in low impedance	t_{OLZ}	5		5		5		5		ns	**Note 2**
$\overline{CE1}$ to output in high impedance	t_{HZ1}		25		30		35		50	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35		50	ns	
$\overline{OE}$ to output in high impedance	t_{OHZ}		25		30		35		50	ns	

Notes 1. See the output load shown in **Figure 1** except for μPD431000A-B15.

2. See the output load shown in **Figure 2** except for μPD431000A-B15.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart



Remark In read cycle, $\overline{WE}$ should be fixed to high level.

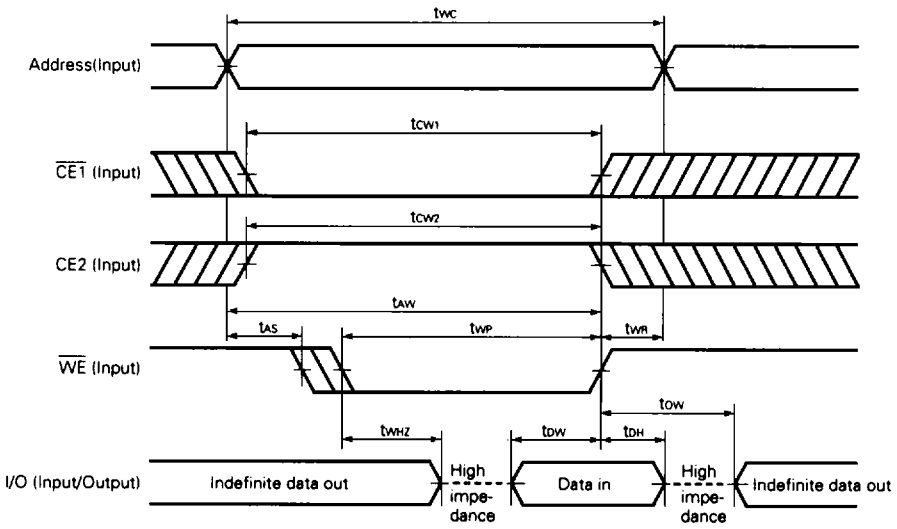
Write Cycle

Parameter	Symbol	$V_{CC} \geq 4.5$ V						$V_{CC} \geq 2.7$ V		Unit	Condition
		μPD431000A-70		μPD431000A-85		μPD431000A-10 μPD431000A-B15		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		150		ns	
$\overline{CE1}$ to end of write	t_{CW1}	55		70		85		120		ns	
CE2 to end of write	t_{CW2}	55		70		85		120		ns	
Address valid to end of write	t_{AW}	55		70		85		120		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	50		60		70		100		ns	
Write recovery time	t_{WR}	5		5		5		10		ns	
Data valid to end of write	t_{DW}	35		35		40		80		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
$\overline{WE}$ to output in high impedance	t_{WHZ}		25		30		35		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		5		ns	

Note See the output load shown in **Figure 2** except for μPD431000A-B15.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Write Cycle Timing Chart 1 ($\overline{WE}$ Controlled)



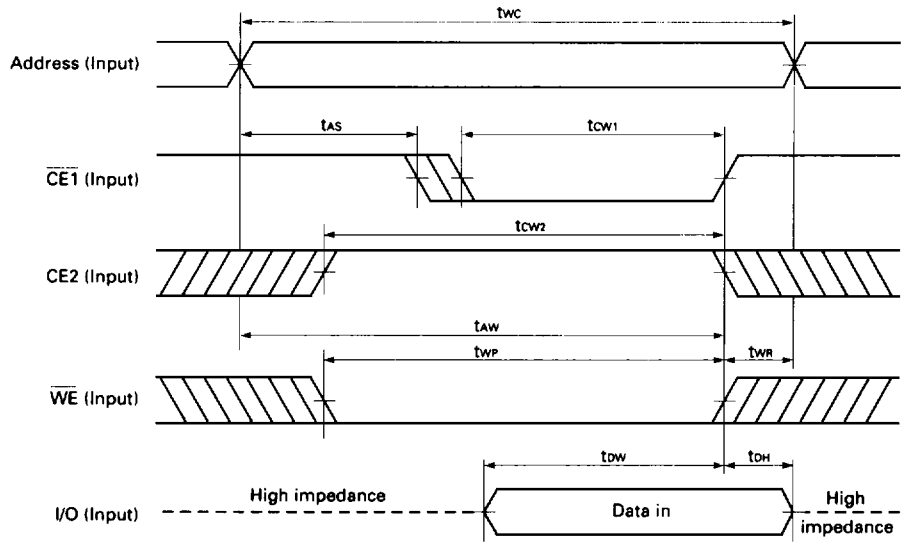
Caution During address transition, $\overline{CE1}$ should be fixed to high level, or CE2 to low level, or $\overline{WE}$ to high level.

Remarks 1. Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

2. If $\overline{CE1}$ changes to low level at the same time or after the change of $\overline{WE}$ to low level, or if CE2 changes to high level at the same time or after the change of $\overline{WE}$ to low level, the I/O pins will remain high impedance state.

3. When $\overline{WE}$ is at low level, the I/O pins are always high impedance. When $\overline{WE}$ is at high level, read operation is executed. Therefore $\overline{OE}$ should be at high level to make the I/O pins high impedance.

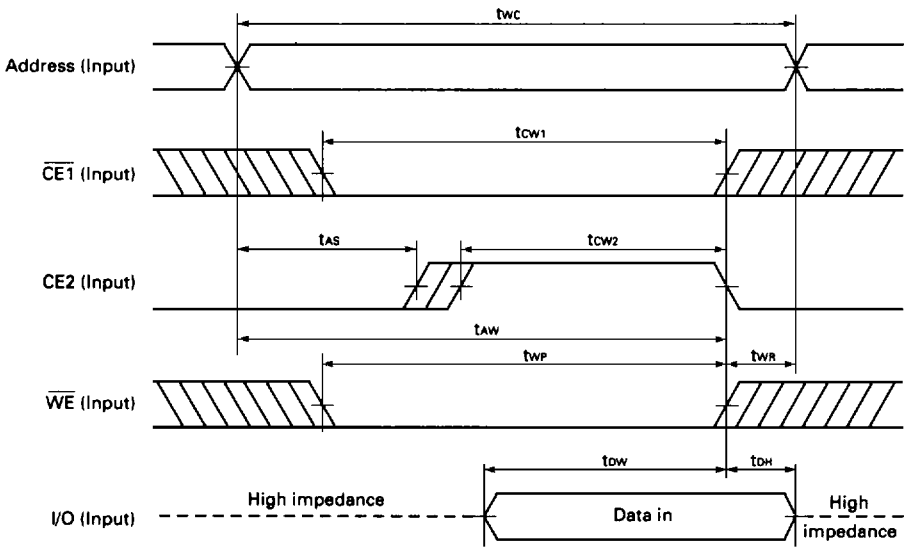
Write Cycle Timing Chart 2 ($\overline{CE1}$ Controlled)



Caution **During address transition, $\overline{CE1}$ should be fixed to high level, or CE2 to low level, or $\overline{WE}$ to high level.**

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Caution **During address transition, $\overline{CE1}$ should be fixed to high level, or CE2 to low level, or $\overline{WE}$ to high level.**

Remark Write operation is done during the overlap time of a low level $\overline{CE1}$, $\overline{WE}$, and a high level CE2.

Low Vcc Data Retention Characteristics

L Version (μPD431000A-L: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} − 0.2 V	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, $\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} − 0.2 V or CE2 ≤ 0.2 V		1	50 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		1	50 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 15 μA ($T_A \leq 40$ °C)

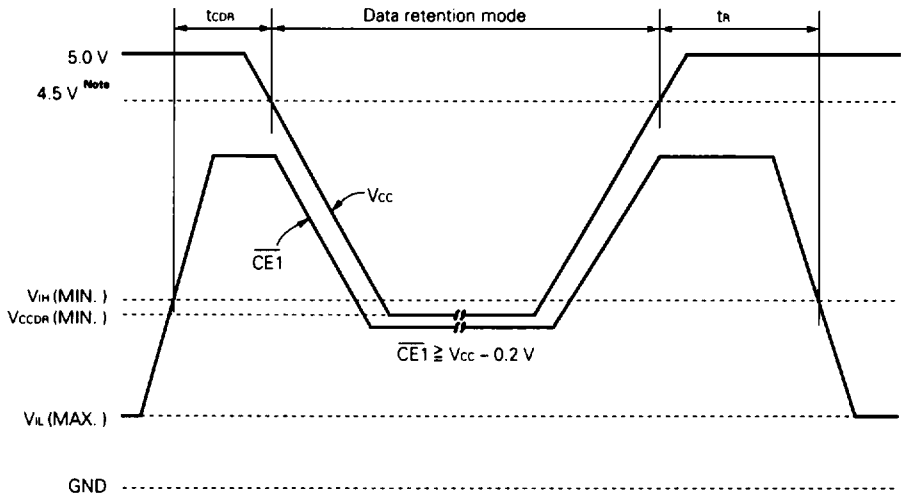
LL Version and B Version (μPD431000A-LL, 431000A-B: T_A = 0 to 70 °C)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	$\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} − 0.2 V	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, $\overline{CE1} \geq V_{CC} - 0.2$ V, CE2 ≥ V_{CC} − 0.2 V or CE2 ≤ 0.2 V		0.5	20 Note	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		0.5	20 Note	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		5			ms

Note 3 μA ($T_A \leq 40$ °C)

Data Retention Timing Chart

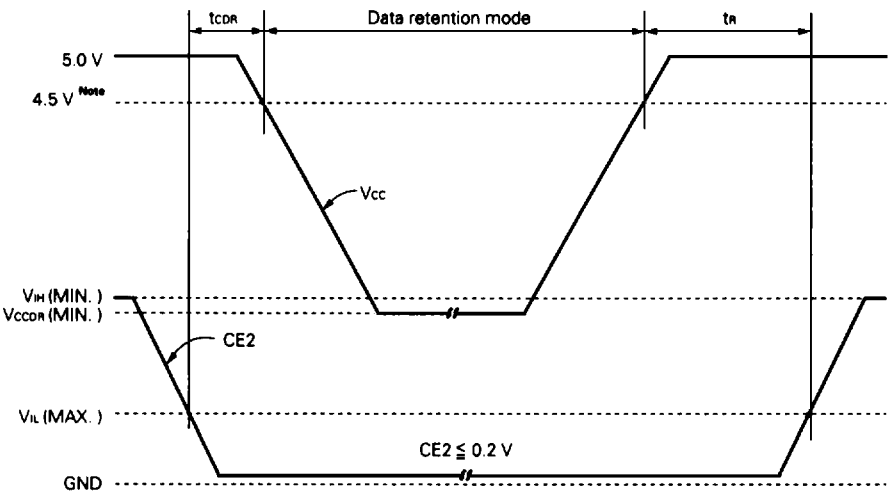
(1) $\overline{CE1}$ Controlled



Note B version : 2.7 V

Remark On the data retention mode by controlling $\overline{CE1}$, the input level of CE2 must be CE2 ≧ VCC – 0.2 V or CE2 ≦ 0.2 V. The other pins (Address, I/O, $\overline{WE}$, $\overline{OE}$) can be in high impedance state.

(2) CE2 Controlled

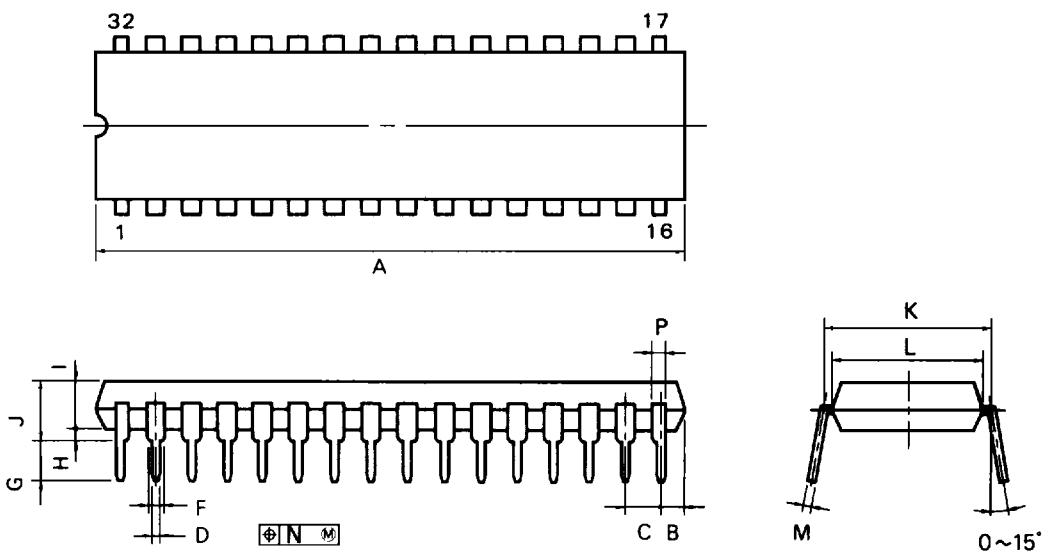


Note B version : 2.7 V

Remark The other pins ($\overline{CE1}$, Address, I/O, $\overline{WE}$, $\overline{OE}$) can be in high impedance state.

Package Drawings

32PIN PLASTIC DIP (600 mil)



P32C-100-600A

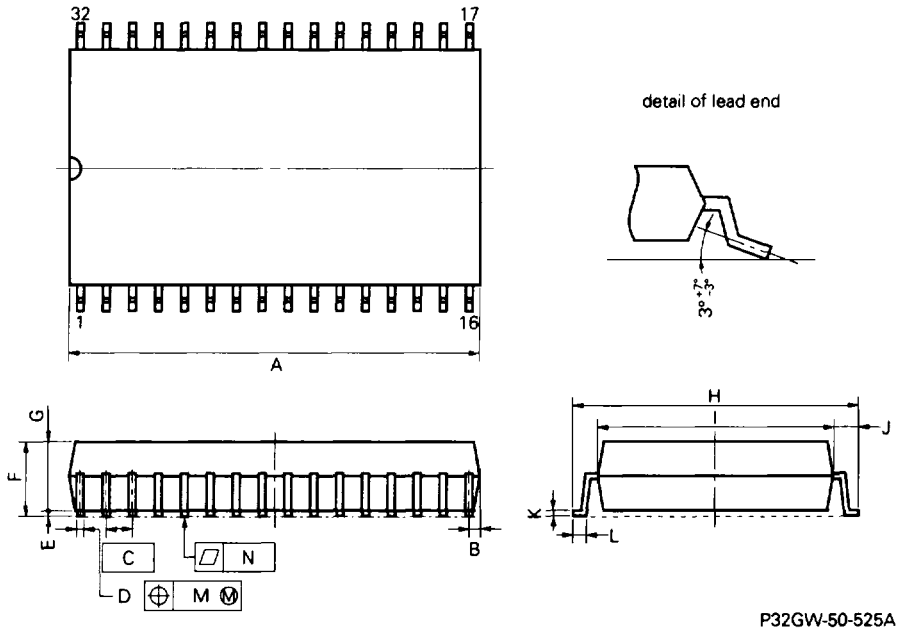
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	40.64 MAX.	1.600 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.1 MIN.	0.043 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.08}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.

32 PIN PLASTIC SOP (525 mil)



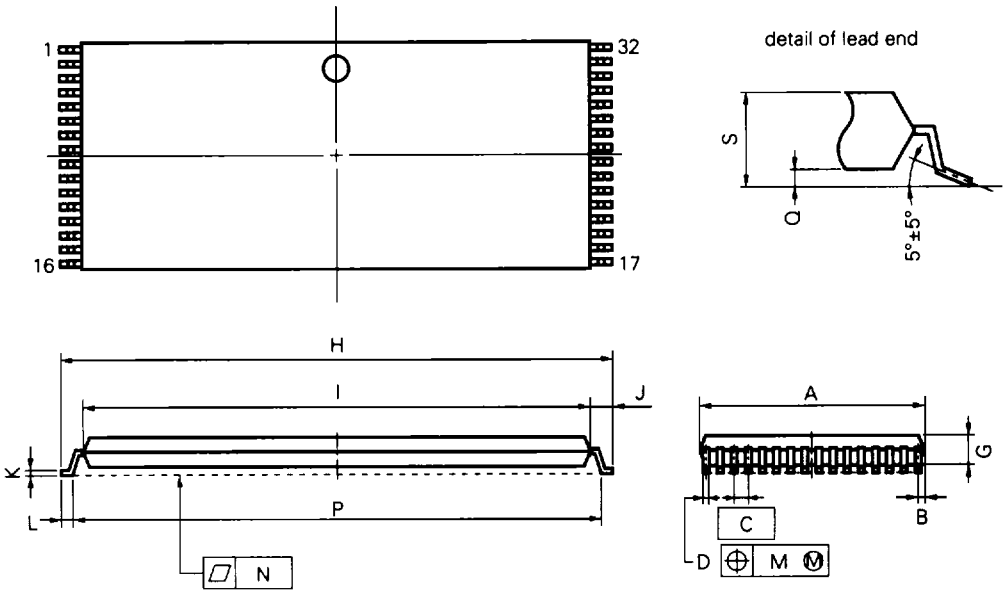
P32GW-50-525A

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.61 MAX.	0.812 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.15±0.05	0.006
F	2.95 MAX.	0.117 MAX.
G	2.7	0.106
H	14.1±0.3	0.555±0.012
I	11.3	0.445
J	1.4±0.2	0.055±0.008
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.10	0.004

32 PIN PLASTIC TSOP(I) (8 × 20)



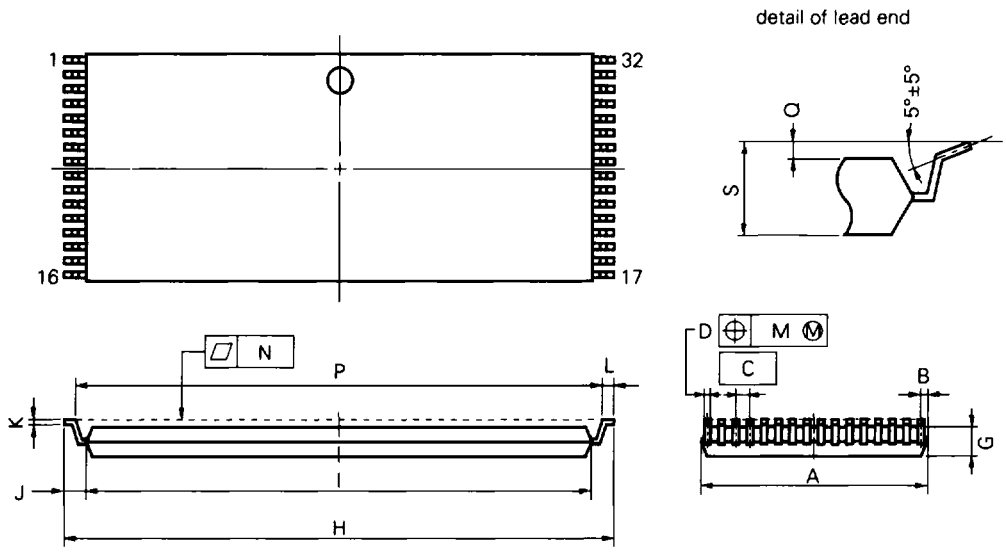
S32GZ-50-KJH-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	8.0±0.2	0.315±0.008
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	20.0±0.2	$0.787^{+0.009}_{-0.008}$
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	19.0±0.2	0.748±0.008
Q	0.05±0.05	0.002±0.002
S	1.1 MAX.	0.044 MAX.

32 PIN PLASTIC TSOP(I) (8 × 20)



S32GZ-50-KKH-1

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	8.0±0.2	0.315±0.008
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.20±0.10	0.008±0.004
G	1.02 MAX.	0.041 MAX.
H	20.0±0.2	$0.787^{+0.009}_{-0.008}$
I	18.4±0.2	$0.724^{+0.009}_{-0.008}$
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.08	0.003
N	0.10	0.004
P	19.0±0.2	0.748±0.008
Q	0.05±0.05	0.002±0.002
S	1.1 MAX.	0.044 MAX.

Recommended Soldering Conditions

The following conditions must be met when soldering conditions of the μPD431000A.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD431000AGW: 32-pin Plastic SOP (525 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number or reflow process: 1 Exposure limit[Note]: 2 days (16 hours pre-baking is required at 125 °C afterwards)	IR30-162-1
	Peak temperature of package surface: 230°C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 2 days (20 hours pre-baking is required at 125°C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR30-202-2
VPS	Peak temperature of package: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1 Exposure limit[Note]: 1 day (16 hours pre-baking is required at 125 °C afterwards)	VP15-161-1
	Peak temperature of package: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 1 day (20 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-201-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Temperature of pre-heat: 120 °C or below (Plastic surface temperature) Number of flow process: 1 Exposure limit[Note]: 2 days (16 hours pre-baking is required at 125 °C afterwards)	WS60-162-1
Partial heating method	Pin temperature: 300 °C or below, Time: 3 seconds or below (Per one side of device).	——

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method."

μPD431000AGZ-KJH: 32-pin Plastic TSOP(I) (8 × 20 mm) (Normal bent)
μPD431000AGZ-KKH: 32-pin Plastic TSOP(I) (8 × 20 mm) (Reverse bent)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1 Exposure limit[Note]: 12 hours (10 hours pre-baking is required at 125 °C afterwards)	IR30-10C-1
	Peak temperature of package surface: 230°C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 8 hours (10 hours pre-baking is required at 125°C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR30-10B-2
VPS	Peak temperature of package: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1 Exposure limit[Note]: 12 hours (10 hours pre-baking is required at 125 °C afterwards)	VP15-10C-1
	Peak temperature of package: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 8 hours (10 hours pre-baking is required at 125 °C afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-10B-2
Partial heating method	Pin temperature: 300 °C or below, Time: 3 seconds or below (Per one side of device).	——

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method."

Type of Through Hole Mount Device

μPD431000ACZ: 32-pin Plastic DIP (600 mil)

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature: 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.