

**SN54HC377, SN54HC378, SN54HC379
SN74HC377, SN74HC378, SN74HC379**
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

D2884, DECEMBER 1982—REVISED JUNE 1989

- 'HC377 and 'HC378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'HC379 Contains Four Flip-Flops with Double-Rail Outputs
- Clock Enable Latched to Avoid False Clocking
- Applications Include:
Buffer/Storage Registers
Shift Registers
Pattern Generators
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

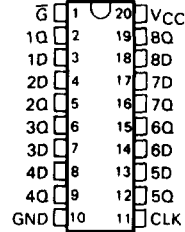
description

These circuits are positive-edge-triggered D-type flip-flops with an enable input. The 'HC377, 'HC378, and 'HC379 devices are similar to 'HC273, 'HC174, and 'HC175 respectively, but feature a latched clock enable (\bar{G}) instead of a common clear.

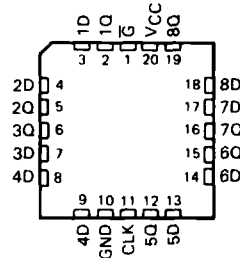
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if \bar{G} is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the \bar{G} input.

The SN54HC377, SN54HC378, and SN54HC379 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC377, SN74HC378, and SN74HC379 are characterized for operation from -40°C to 85°C .

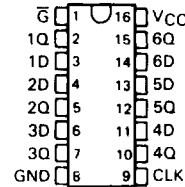
SN54HC377 . . . J PACKAGE
SN74HC377 . . . DW OR N PACKAGE
(TOP VIEW)



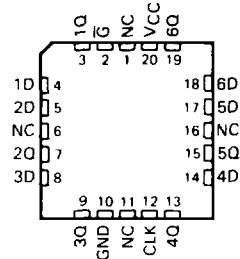
SN54HC377 . . . FK PACKAGE
(TOP VIEW)



SN54HC378 . . . J PACKAGE
SN74HC378 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC378 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

2
HCMOS Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



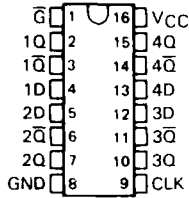
POST OFFICE BOX 855012 • DALLAS, TEXAS 75265

Copyright © 1989, Texas Instruments Incorporated

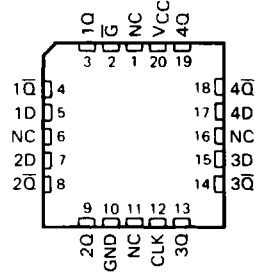
2-431

SN54HC377, SN54HC379, SN74HC377, SN74HC379 OCTAL AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

SN54HC379 ... J PACKAGE
SN74HC379 ... D, J, OR N PACKAGE
(TOP VIEW)

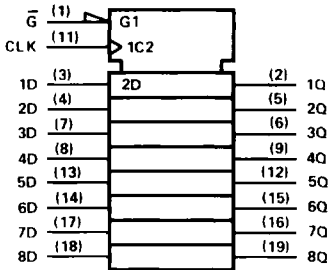


SN54HC379 ... FK PACKAGE
(TOP VIEW)



2

HC377 logic symbol †
HCMOS Devices



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

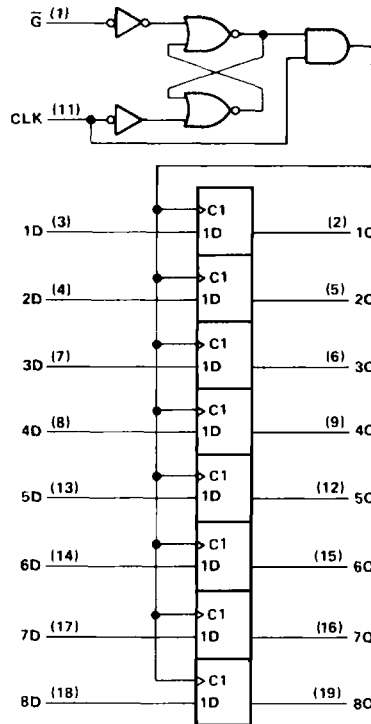
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
Ḡ	CLOCK	DATA	Q
H	X	X	Q ₀
L	↑	H	H
L	↑	L	L
X	L	X	Q ₀

H = high level, L = low level, X = irrelevant

NC - No internal connection

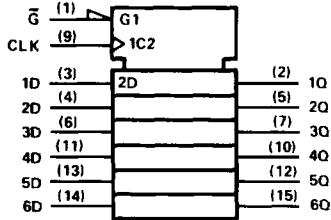
HC377 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

SN54HC378, SN54HC379, SN74HC378, SN74HC379 HEX AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

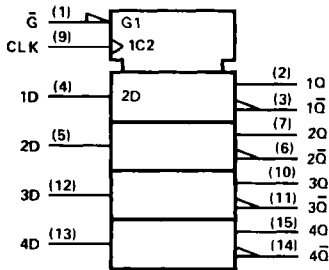
'HC378 logic symbol†



**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUT
\bar{G}	CLOCK	DATA	Q
H	X	X	Q_0
L	↑	H	H
L	↑	L	L
X	L	X	Q_0

'HC379 logic symbol†



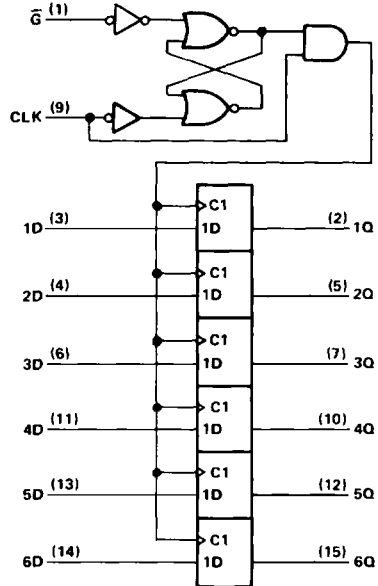
**FUNCTION TABLE
(EACH FLIP-FLOP)**

INPUTS			OUTPUTS	
\bar{G}	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q_0	\bar{Q}_0
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	\bar{Q}_0

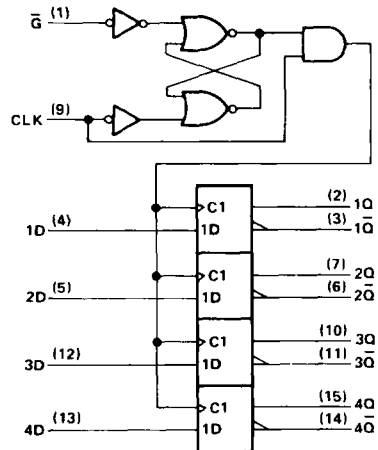
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers are for D, J, and N packages.

'HC378 logic diagram (positive logic)



'HC379 logic diagram (positive logic)



SN54HC377, SN54HC378, SN54HC379
SN74HC377, SN74HC378, SN74HC379
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE

absolute maximum ratings over operating free-air temperature†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D, DW, or N package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2
HCMOS Devices

recommended operating conditions

		SN54HC377 SN54HC378 SN54HC379			SN74HC377 SN74HC378 SN74HC379			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5			V
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	0.3	0	0.3	V
		$V_{CC} = 4.5$ V		0	0.9	0	0.9	
		$V_{CC} = 6$ V		0	1.2	0	1.2	
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
T_A	Operating free-air temperature	-55		125	-40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20$ μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -5.2$ mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20$ μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	4.5 V		0.17	0.26		0.4		0.33		
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		± 0.1	± 100		± 1000		± 1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

**SN54HC377, SN54HC378, SN74HC379
SN74HC377, SN74HC378, SN74HC379
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH CLOCK ENABLE**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25 °C			SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
			f _{clock}	Clock frequency	2 V	0	5	0	3	
		4.5 V	0	25	0	16	0	20		
		6 V	0	29	0	19	0	23		
t _w	Pulse duration, CLK high or low	2 V	100		150		125		ns	
		4.5 V	20		30		25			
		6 V	17		25		21			
t _{su}	Set up time before CLK↓	D	2 V	100		150		125		ns
			4.5 V	20		30		25		
		6 V	17		25		21			
	\bar{C} high or low	2 V	100		150		125		ns	
	4.5 V	20		30		25				
	6 V	17		25		21				
t _h	Hold time after CLK↑	\bar{C} inactive or active, data	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25 °C			SN54HC377 SN54HC378 SN54HC379		SN74HC377 SN74HC378 SN74HC379		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}			2 V	5	11		3		4	MHz	
			4.5 V	25	54		16		20		
			6 V	29	64		19		23		
t _{pd}	CLK	Any	2 V	56	160		240		200	ns	
			4.5 V	15	32		48		40		
			6 V	12	27		41		34		
t _t	Any	Any	2 V	38	75		110		95	ns	
			4.5 V	8	15		22		19		
			6 V	6	13		19		16		

C _{pd}	Power dissipation capacitance	No load, T _A = 25 °C	30 pF typ
-----------------	-------------------------------	---------------------------------	-----------

Note 1: Load circuits and voltage waveforms are shown in Section 1.

2
HCMOS Devices

