DESCRIPTION

The HY62V8100A-(I)/HY62U8100A-(I) is a high speed, low power and 1M bit CMOS SRAM organized as 131,072 words by 8bit. The HY62V8100A-(I) / HY62U8100A-(I) uses high performance CMOS process technology and designed for high speed low power circuit technology. It is particulary well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0V.

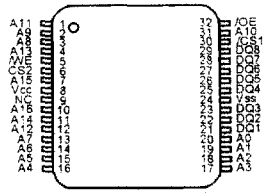
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(L/LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 32pin 8x20mm/ 8x13.4mm Small TSOP-I (Standard and Reversed)

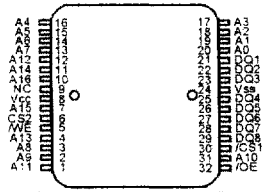
Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (℃)
				L	LL	
HY62V8100A	3.3	85/100/120	5	50	10	0~70(Normal)
HY62V8100A-I	3.3	85/100/120	5	50	20	-40~85(E.T.)
HY62U8100A	3.0	100/120/150	5	50	10	0~70(Normal)
HY62U8100A-I	3.0	100/120/150	5	50	15	-40~85(E.T.)

Note 1. E.T. : Extended Temperature. Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION



TSOP-I/Small TSOP-I
(Standard)

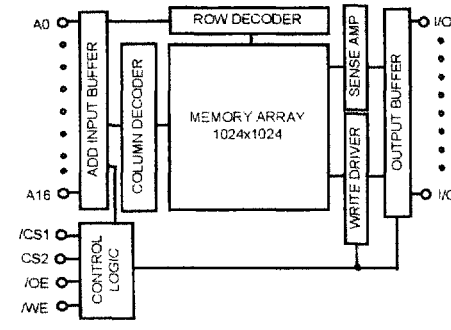


TSOP-I/Small TSOP-I
(Reversed)

PIN DESCRIPTION

Pin Name	Pin Function
/CS1	Chip Select 1
CS2	Chip Select 2
/WE	Write Enable
/OE	Output Enable
A0 ~ A16	Address Input
I/O1 ~ I/O8	Data Input/Output
Vcc	Power(3.3V or 3.0V)
Vss	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62V8100ALT1	85/100/120	L-part		TSOP-I(Standard)
HY62V8100ALLT1	85/100/120	LL-part		TSOP-I(Standard)
HY62V8100ALR1	85/100/120	L-part		TSOP-I(Reversed)
HY62V8100ALLR1	85/100/120	LL-part		TSOP-I(Reversed)
HY62V8100ALST	85/100/120	L-part		Small TSOP-I(Standard)
HY62V8100ALLST	85/100/120	LL-part		Small TSOP-I(Standard)
HY62V8100ALSR	85/100/120	L-part		Small TSOP-I(Reversed)
HY62V8100ALLSR	85/100/120	LL-part		Small TSOP-I(Reversed)
HY62V8100ALT1-I	85/100/120	L-part	E.T.	TSOP-I(Standard)
HY62V8100ALLT1-I	85/100/120	LL-part	E.T.	TSOP-I(Standard)
HY62V8100ALR1-I	85/100/120	L-part	E.T.	TSOP-I(Reversed)
HY62V8100ALLR1-I	85/100/120	LL-part	E.T.	TSOP-I(Reversed)
HY62V8100ALST-I	85/100/120	L-part	E.T.	Small TSOP-I(Standard)
HY62V8100ALLST-I	85/100/120	LL-part	E.T.	Small TSOP-I(Standard)
HY62V8100ALSR-I	85/100/120	L-part	E.T.	Small TSOP-I(Reversed)
HY62V8100ALLSR-I	85/100/120	LL-part	E.T.	Small TSOP-I(Reversed)
HY62U8100ALT1	100/120/150	L-part		TSOP-I(Standard)
HY62U8100ALLT1	100/120/150	LL-part		TSOP-I(Standard)
HY62U8100ALR1	100/120/150	L-part		TSOP-I(Reversed)
HY62U8100ALLR1	100/120/150	LL-part		TSOP-I(Reversed)
HY62U8100ALST	100/120/150	L-part		Small TSOP-I(Standard)
HY62U8100ALLST	100/120/150	LL-part		Small TSOP-I(Standard)
HY62U8100ALSR	100/120/150	L-part		Small TSOP-I(Reversed)
HY62U8100ALLSR	100/120/150	LL-part		Small TSOP-I(Reversed)
HY62U8100ALT1-I	100/120/150	L-part	E.T.	TSOP-I(Standard)
HY62U8100ALLT1-I	100/120/150	LL-part	E.T.	TSOP-I(Standard)
HY62U8100ALR1-I	100/120/150	L-part	E.T.	TSOP-I(Reversed)
HY62U8100ALLR1-I	100/120/150	LL-part	E.T.	TSOP-I(Reversed)
HY62U8100ALST-I	100/120/150	L-part	E.T.	Small TSOP-I(Standard)
HY62U8100ALLST-I	100/120/150	LL-part	E.T.	Small TSOP-I(Standard)
HY62U8100ALSR-I	100/120/150	L-part	E.T.	Small TSOP-I(Reversed)
HY62U8100ALLSR-I	100/120/150	LL-part	E.T.	Small TSOP-I(Reversed)

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.3 to 4.6	V	
T_A	Operating Temperature	0 to 70	℃	HY62V8100A
				HY62U8100A
		-40 to 85	℃	HY62V8100A-I
				HY62U8100A-I
T_{STG}	Storage Temperature	-65 to 125	℃	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	℃•sec	

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Product	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	HY62V8100A-(I)	3.0	3.3	3.6	V
		HY62U8100A-(I)	2.7	3.0	3.3	V
Vss	Ground	HY62V8100A-(I) HY62U8100A-(I)	0	0	0	V
VIH	Input High Voltage	HY62V8100A-(I) HY62U8100A-(I)	2.2	-	Vcc+0.3	V
VIL	Input Low Voltage	HY62V8100A-(I) HY62U8100A-(I)	-0.3(1)	-	0.6	V

Note :
1. VIL = -1.5V for pulse width less than 30ns

TRUTH TABLE

/CS1	CS2	/WE	/OE	MODE	I/O OPERATION
H	X	X	X	Standby	High-Z
X	L	X	X		High-Z
L	H	H	H	Output Disabled	High-Z
L	H	H	L	Read	Data Out
L	H	L	X	Write	Data In

Note :
1. H=VIH, L=VIL, X=don't care

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.3V±10%/3.0V±10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

Symbol	Parameter		Test Condition		Min.	Typ.	Max.	Unit
ILI	Input Leakage Current		Vss ≤ VIN ≤ Vcc		-1	-	1	uA
ILO	Output Leakage Current		Vss ≤ VOUT ≤ Vcc, /CS1 = VIH or CS2 = VIL or /OE = VIH or /WE = VIL		-1	-	1	uA
Icc	Operating Power Supply Current		/CS1 = VIL, CS2 = VIH, VIN = VIH or VIL, II/O = 0mA		-	3	5	mA
ICC1	Average Operating Current	HY62V8100A-(I)	/CS1 = VIL CS2 = VIH, Min Duty Cycle = 100%, II/O = 0mA		-	25	35	mA
		HY62U8100A-(I)			-	20	30	mA
ISB	TTL Standby Current (TTL Input)		/CS1 = VIH or CS2 = VIL		-	-	0.5	mA
ISB1	Standby Current (CMOS Input)	HY62V8100A	/CS1 ≥ Vcc - 0.2V CS2 ≤ 0.2V or CS2 ≥ Vcc - 0.2V	L	-	1	50	uA
				LL	-	0.5	10	uA
		HY62V8100A-I		L	-	1	50	uA
				LL	-	0.5	20	uA
		HY62U8100A		L	-	1	50	uA
				LL	-	0.5	10	uA
		HY62U8100A-I		L	-	1	50	uA
				LL	-	0.5	15	uA
VOL	Output Low Voltage		IOL = 2.1mA		-	-	0.4	V
VOH	Output High Voltage		IOH = -1mA		2.2	-	-	V

Note : Typical values are at Vcc = 3.3V/3.0V, TA = 25℃

AC CHARACTERISTICS(I)

Vcc = 3.3V±10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
9	tOH	Output Hold from Address Change	10	-	10	-	20	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	85	-	100	-	120	-	ns
11	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
12	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	55	-	60	-	85	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	30	0	30	0	50	ns
17	tDW	Data to Write Time Overlap	40	-	45	-	50	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

AC CHARACTERISTICS(II)

Vcc = 3.0V±10%, TA = 0℃ to 70℃(Normal)/ -40℃ to 85℃(E.T.), unless otherwise specified

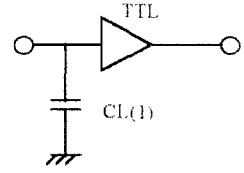
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
6	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
8	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
9	tOH	Output Hold from Address Change	20	-	20	-	20	-	ns
	WRITE CYCLE								
10	tWC	Write Cycle Time	100	-	120	-	150	-	ns
11	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
12	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	75	-	85	-	100	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
17	tDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0℃ to 70℃(Normal) / -40℃ to 85℃(E.T.), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : 1 Including jig and scope capacitance

CAPACITANCE

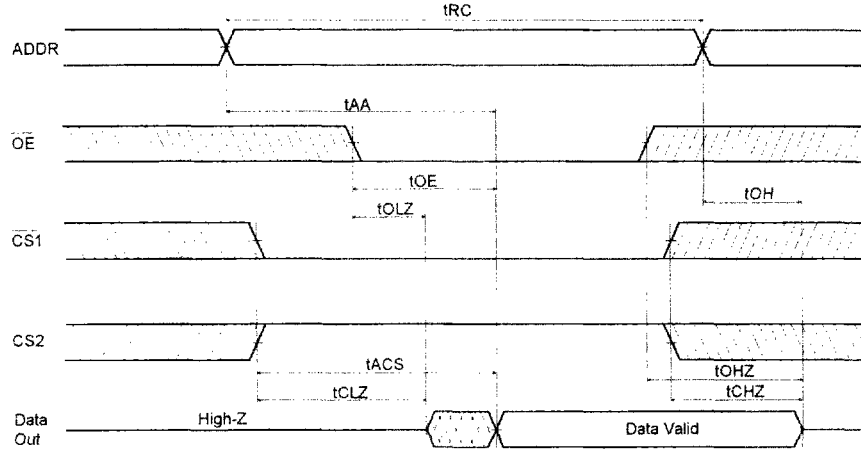
(Temp = 25℃, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	8	pF

Note : These parameters are sampled and not 100% tested

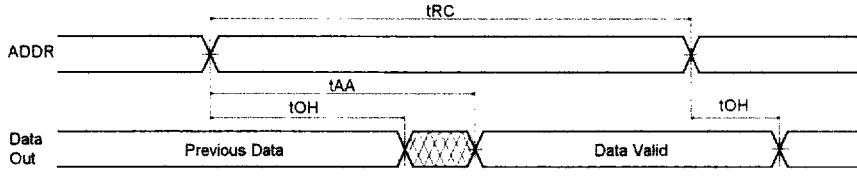
TIMING DIAGRAM

READ CYCLE 1



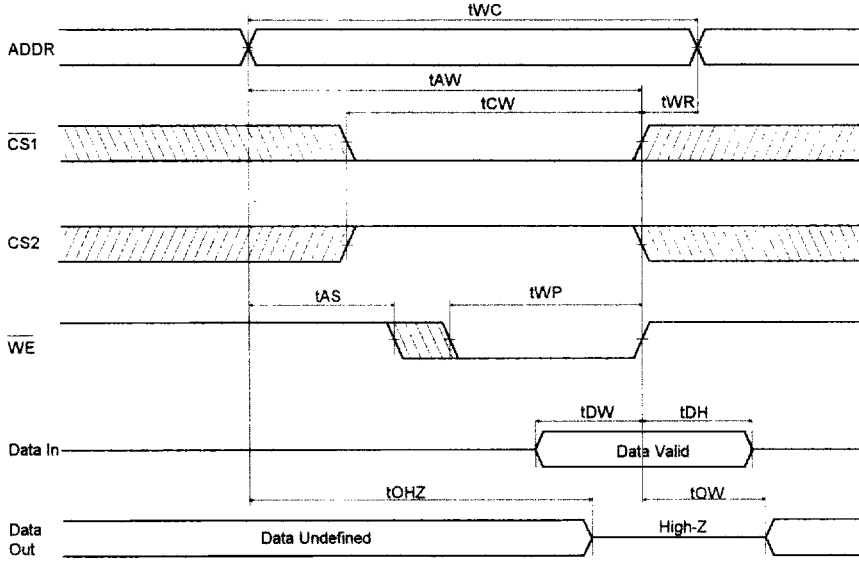
Note(READ CYCLE):
1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for the read cycle.

READ CYCLE 2

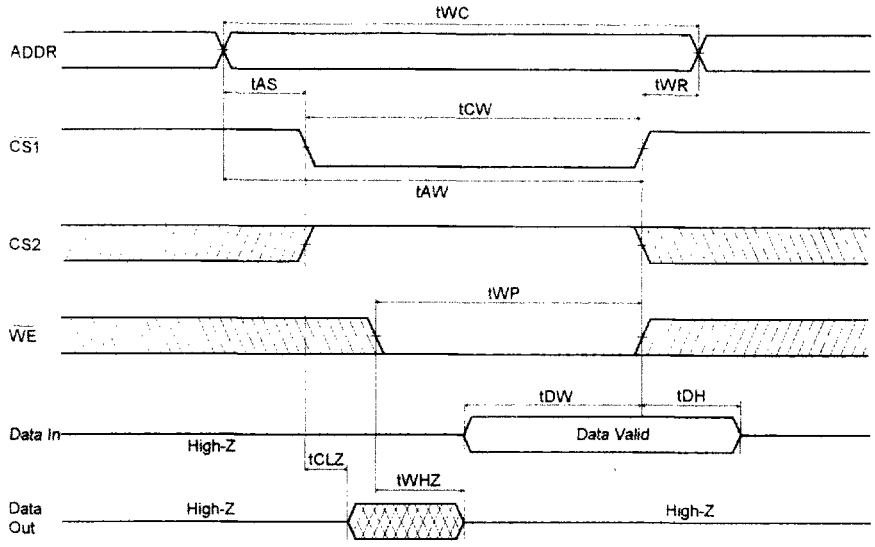


Note(READ CYCLE):
1. /WE is high for the read cycle.
2. Device is continuously selected /CS1 = V_{IL}, CS2 = V_{IH}.
3. /OE =V_{IL}.

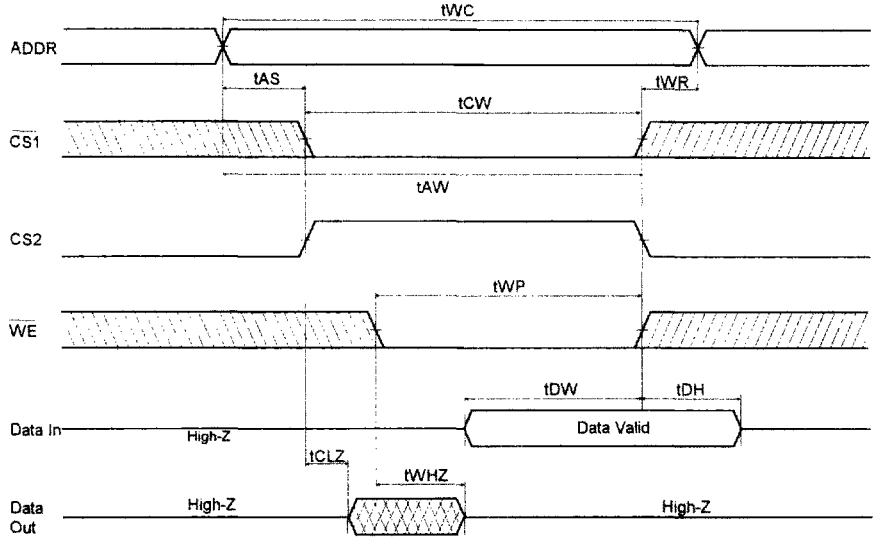
WRITE CYCLE 1(/WE Controlled)



WRITE CYCLE 2 (/CS1 Controlled)



WRITE CYCLE 3 (CS2 Controlled)



Notes(WRITE CYCLE):

1. A write occurs during the overlap of a low /CS1, CS2 and low /WE. A write begines at the latest transition among /CS1 going low, CS2 going high and /WE going low: A write ends at the earliest transition among /CS1 going high, CS2 low and /WE going high. tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS1 going low or CS2 going high to the end of write .
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR is applied in case a write ends as /CS1, or /WE going high, and tWR is applied in case a write ends at CS2 going low.
5. If /OE, CS2 and /WE are in the read mode during this period, the I/O pins are in the output low-Z state, input of opposite phase of the output must not be applied because bus contention can occur.
6. If /CS1 goes low simultaneously with /WE going low, the outputs remain in high impedance state.
7. Dout is the read data of the new address.
8. When /CS1 is low and CS2 is high, I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.

DATA RETENTION ELECTRIC CHARACTERISTIC

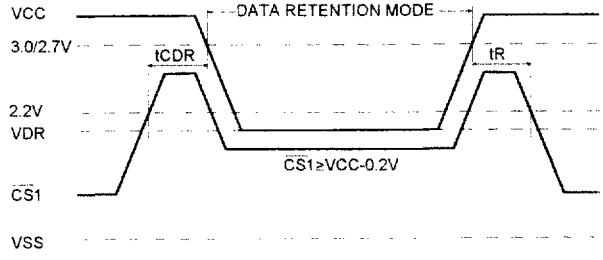
T_A=0℃ to 70℃(Normal)/-40℃ to 85℃(E.T.)

Symbol	Parameter		Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention		/CS1 ≥ Vcc-0.2V, CS2 ≤ 0.2V or ≥ Vcc - 0.2V, Vss ≤ V_{IN} ≤ Vcc		2.0	-	-	V
I_{CCDR}	Data Retention Current	HY62V8100A	Vcc=3.0V, /CS1 ≥ Vcc - 0.2V, CS2 ≤ 0.2V or ≥ Vcc - 0.2V, Vss ≤ V_{IN} ≤ Vcc	L	-	1	50	uA
				LL	-	0.5	10	uA
		HY62V8100A-I		L	-	1	50	uA
				LL	-	0.5	15	uA
		HY62U8100A		L	-	1	50	uA
				LL	-	0.5	10	uA
		HY62U8100A-I		L	-	1	50	uA
				LL	-	0.5	15	uA
tCDR	Chip Deselect to Data Retention Time		See Data Retention		0	-	-	ns
tR	Operating Recovery Time		Timing Diagram		tRC(2)	-	-	ns

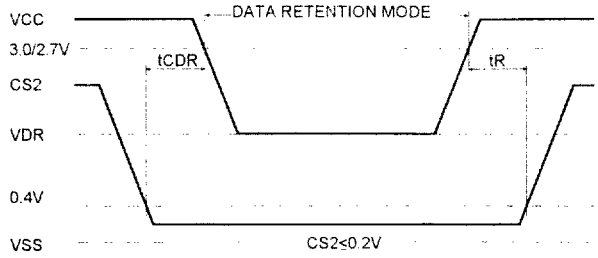
Notes:

1. Typical values are under the condition of T_A = 25℃.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM 1



DATA RETENTION TIMING DIAGRAM 2



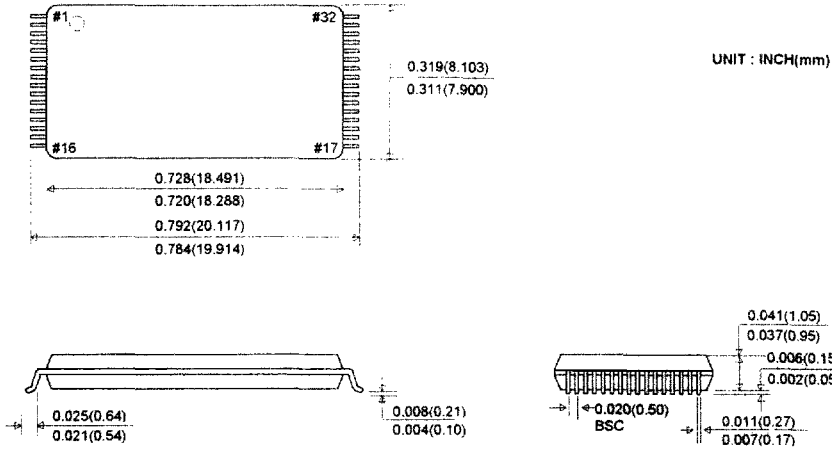
Note :
1. 3.0V : HY62V8100A and HY62V8100A-I
   2.7V : HY62U8100A and HY62U8100A-I

RELIABILITY SPEC.

TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

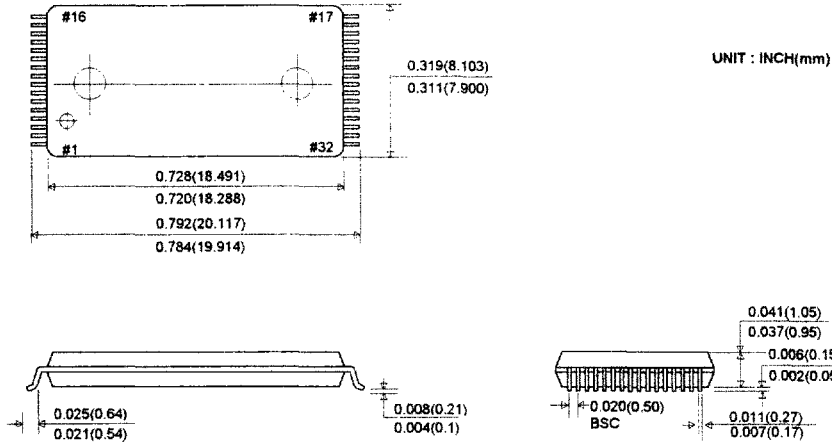
PACKAGE INFORMATION

32pin 8x20mm Thin Small Outline Package Standard(T1)



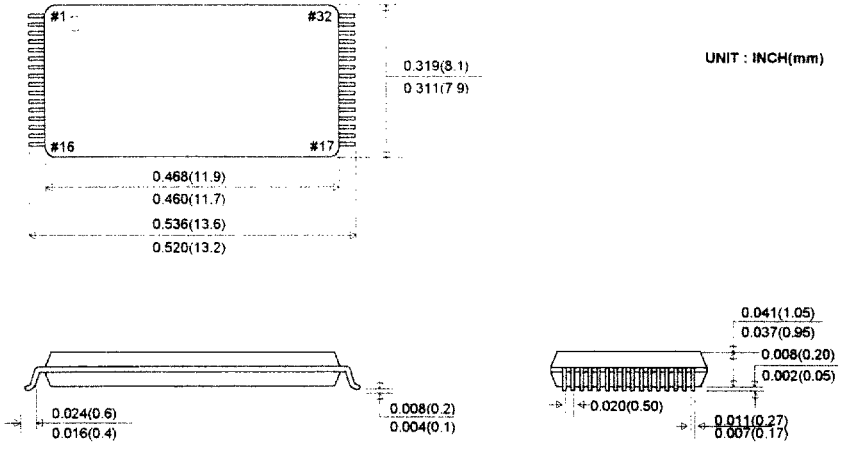
UNIT : INCH(mm)

32pin 8x20mm Thin Small Outline Package Reversed(R1)



UNIT : INCH(mm)

32pin 8x13.4mm Thin Small Outline Package Standard(ST)



32pin 8x13.4mm Thin Small Outline Package Reversed(SR)