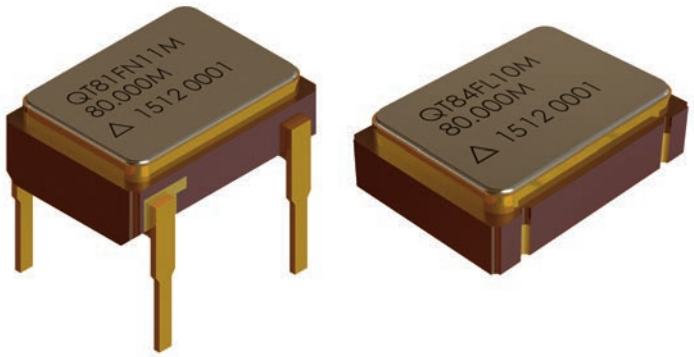
Description

Q-Tech's 5x7mm low profile extreme high shock hybrid oscillators consist of an IC operating at various supply voltages from 1.8V, 2.5V, 3.3V, and 5.0Vdc and a miniature strip quartz crystal. The series is offered in various ceramic package configurations from true Surface-Mount SMT to straight leads and formed leads. This is the smallest package offered with a four-point crystal mount for high shock and high reliability military applications.



Features

- Made in the USA
- ECCN: EAR99
- Innovative Four Point Mount Strip Crystal Resonator
- Broad Frequency Range, 500kHz to 156.25MHz
- Small Footprint
- CMOS, LVHCMOS, TTL Logic
- Various Supply Voltages, 1.8Vdc to 5.0Vdc
- Wide Operating Temperature Range, -55°C to 125°C
- Tri-State Output (Option D)
- Hermetically sealed package
- Fundamental and 3rd Overtone Designs
- Full or Partial Screening per MIL-PRF-55310, Level B
- High Shock Resistant Tested Up to 20,000g Mechanical Shock, Half-Sine, 0.3ms, All Axes
- Tape and Reel Packaging
- Optional Hot Solder Dip, Sn60Pb40 or SAC305
- RoHS Compliant

(Sample part number)

Q T 81F L D 10 M - 50.000MHz

Q	T	81	F	L	D	10	M	-	100.000MHz

Solder Dip Options
T = Standard (*)
S = Sn60Pb40
G = SAC305

Materials Level
81, 86=Leaded
82, 87=Formed Leads
83, 80=Formed Leads
84, 85=SMT

Logic & Supply Voltage:
HC = HCMOS +5V
T = TTL +5Vdc
L = CMOS +3.3V
N = CMOS +2.5V
R = CMOS +1.8V

Frequency vs. Temperature Code (***):
7 = ± 75ppm at -55ºC to +125°C
9 = ± 50ppm at -55ºC to +125°C
10 = ± 100ppm at -55ºC to +125°C
11 = ± 50ppm at -40ºC to +85°C
12 = ± 100ppm at -40ºC to +85°C
17 = ± 75ppm at -60ºC to +125°C
18 = ± 100ppm at -60ºC to +125°C

Screening Option:
Blank = No Screening
M = Screening per MIL-PRF-55310, Level B

Output Frequency

Tristate Option:
Blank = No Tristate
D = Tristate

1/ Please contact Q-Tech for higher frequencies

Applications

- Designed to Meet High Shock Requirements
- Missile Launch
- Gun-Launched Munitions and Systems
- Avionics
- Navigation On-Board System
- Oil-Drilling and Exploration Equipment

Packaging Options

- Standard ESD packaging

TABLE I - ELECTRICAL CHARACTERISTICS (+5Vdc ± 10%)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	500kHz – 70MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+5Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	+7Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	20mA Max. 500kHz – <16MHz 25mA Max. 16MHz – <32MHz 35mA Max. 32MHz – 70MHz	No Load
Load	15pF//10kΩ or 6TTL to 10TTL	Note 1/
Duty Cycle (Sym)	45/55% Max. 500kHz – <16MHz 40/60% Max. 16MHz – 70MHz	Measured at ½ Vdd (CMOS) or 1.4V (TTL)
Rise and Fall Times (Tr/Tf)	6ns Max. for Fo < 40MHz 3ns Max. for Fo ≥ 40MHz	Measured Between 10% and 90% or 0.8V to 2.0V (TTL)
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	0.9*Vdd Min. (CMOS) 2.4Vdc Min. (TTL)	
Output Voltage Low (VOL)	0.1*Vdd Max. (CMOS) 0.4Vdc Max. (TTL)	
Enable/Disable (Tristate Option – D)	VIH ≥ 2.2Vdc Oscillation VIL ≤ 0.8Vdc High Impedance	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm Max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -78dBc/Hz 100Hz Offset -109dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -145dBc/Hz 100kHz Offset -150dBc/Hz	QS83HC -40MHz at +5Vdc Typical by Design Not Tested Unless Specified
g-Sensitivity	3ppb/g Typ.	By Design; Not Tested
1/ Consult factory for different load. Capable to drive up to 50pF.		

TABLE II - ELECTRICAL CHARACTERISTICS (+3.3VDC ± 10%)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	500kHz – 156.25MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+3.3Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	+5Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	6mA Max. 500kHz – <16MHz 10mA Max. 16MHz – <32MHz 20mA Max. 32MHz – <70MHz 30mA Max. 70MHz – <100MHz 40mA Max. 100MHz – 156.25MHz	No Load
Load	15pF//10kΩ	Note 1/
Duty Cycle (Sym)	45/55% Max. 500kHz – <16MHz 40/60% Max. 16MHz – 156.25MHz	Measured at ½ Vdd (CMOS) or 1.4V (TTL)
Rise and Fall Times (Tr/Tf)	6ns Max. for Fo < 40MHz 3ns Max. for Fo ≥ 40MHz	Measured Between 10% and 90%
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	0.9*Vdd Min. (CMOS)	
Output Voltage Low (VOL)	0.1*Vdd Max. (CMOS)	
Enable/Disable (Tristate Option – D)	VIH ≥ 2.2Vdc Oscillation VIL ≤ 0.8Vdc High Impedance	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm Max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -78dBc/Hz 100Hz Offset -109dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -145dBc/Hz 100kHz Offset -150dBc/Hz	QS83L-32MHz at +3.3Vdc Typical by Design Not Tested Unless Specified
g-Sensitivity	3ppb/g Typ.	By Design; Not Tested
1/ Consult factory for different load. Capable to drive up to 30pF.		

TABLE III - ELECTRICAL CHARACTERISTICS (+2.5VDC ± 10%)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	500kHz – 133MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+2.5Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	+5Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	6mA Max. 500kHz – <40MHz 15mA Max. 40MHz – <60MHz 25mA Max. 60MHz – <85MHz 35mA Max. 85MHz – 133MHz	No Load
Load	15pF//10kΩ	Note 1/
Duty Cycle (Sym)	45/55% Max. 500kHz – <16MHz 40/60% Max. 16MHz – 133MHz	Measured at ½ Vdd (CMOS)
Rise and Fall Times (Tr/Tf)	6ns Max. for Fo < 40MHz 3ns Max. for Fo ≥ 40MHz	Measured Between 10% and 90%
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	0.9*Vdd Min. (CMOS)	
Output Voltage Low (VOL)	0.1*Vdd Max. (CMOS)	
Enable/Disable (Tristate Option – D)	VIH ≥ 0.7*Vdd Oscillation VIL ≤ 0.3*Vdd High Impedance	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm Max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -74dBc/Hz 100Hz Offset -107dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz Offset -145dBc/Hz 100kHz Offset -150dBc/Hz	QS81N-80MHz at +2.5Vdc Typical by Design Not Tested Unless Specified
g-Sensitivity	3ppb/g Typ.	By Design; Not Tested
1/ Consult factory for different load. Capable to drive up to 30pF.		

TABLE IV - ELECTRICAL CHARACTERISTICS (+1.8VDC±10%)

PARAMETERS	LIMITS	COMMENTS
Output Frequency Range (Fo)	500kHz – 100MHz	Consult Factory for Lower and Higher Frequencies
Supply Voltage (Vdd)	+1.8Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	+5Vdc	
Operating Temperature (Top)	See Ordering Information	
Storage temperature (Tsto)	-62°C to +125°C	
Supply current (Idd)	4mA Max. 500kHz – <40MHz 10mA Max. 40MHz – <50MHz 20mA Max. 50MHz – <85MHz 25mA Max. 85MHz – 100MHz	No Load
Load	15pF//10kΩ	Note 1/
Duty Cycle (Sym)	445/55% Max. 500kHz – <16MHz 40/60% Max. 16MHz – 133MHz	Measured at ½ Vdd (CMOS)
Rise and Fall Times (Tr/Tf)	6ns Max. for Fo < 40MHz 3ns Max. for Fo ≥ 40MHz	Measured Between 10% and 90%
Start-Up Time (Tstup)	10ms Max.	
Output Voltage High (VOH)	0.9*Vdd Min. (CMOS)	
Output Voltage Low (VOL)	0.1*Vdd Max. (CMOS)	
Enable/Disable (Tristate Option – D)	VIH ≥ 0.7*Vdd Oscillation VIL ≤ 0.3*Vdd High Impedance	
Aging at +70°C ± 3°C	±5ppm First Year Max. ±2ppm max. Each Year Thereafter	
Period Jitter 1σ (RMS) Integrated Phase Jitter	5ps Typ. 1ps Max.	By Design; Not Tested 12kHz to 20MHz
Phase Noise (Typical)	10Hz Offset -74dBc/Hz 100Hz Offset -107dBc/Hz 1kHz Offset -130dBc/Hz 10kHz Offset -135dBc/Hz 100kHz offset -145dBc/Hz 100kHz Offset -150dBc/Hz	QS81R-80MHz at +1.8V Typical by Design Not Tested Unless Specified
g-Sensitivity	3ppb/g Typ.	By Design; Not Tested
1/ Consult factory for different load. Capable to drive up to 30pF.		

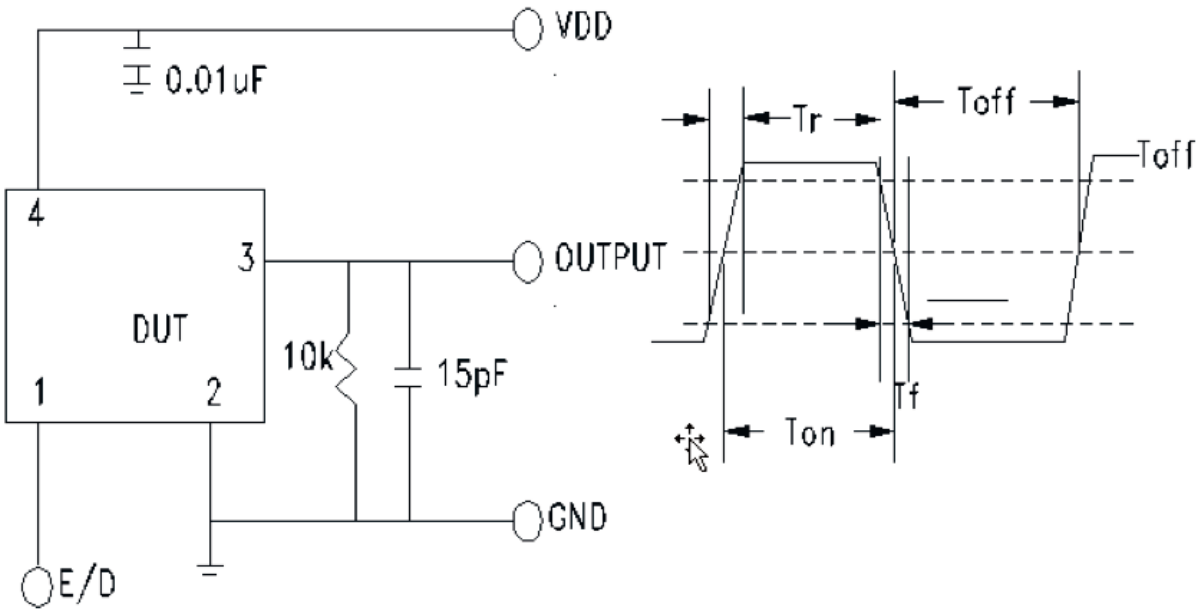
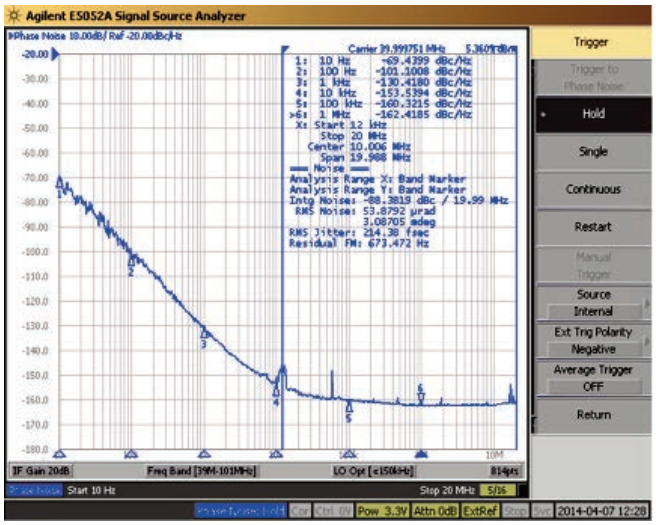


FIGURE 1 – CIRCUIT DIAGRAM AND OUTPUT WAVEFORM



OFFSET FREQUENCY (Hz)	40MHz	80MHz
10	-70	-70
100	-101	-100
1E3	-131	-130
1E4	-153	-150
1E5	-160	-160
1E6	-160	-160

FIGURE 2 – TYPICAL PHASE NOISE OF A 40MHz QT81FL-32.000MHz

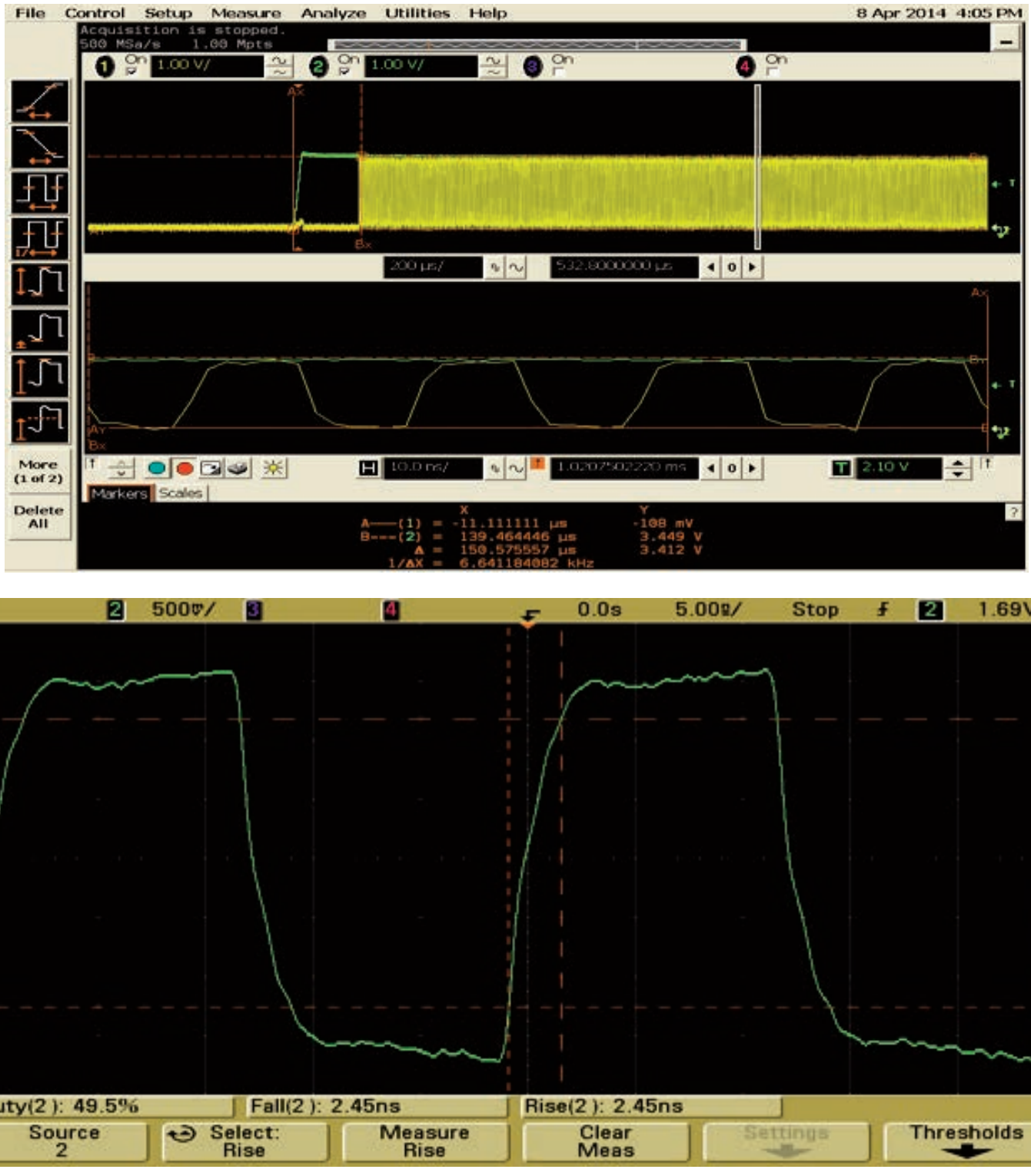


Figure 3 – Typical Start-Up Time and Output Waveform of a QT82L-40MHz 3.3Vdc

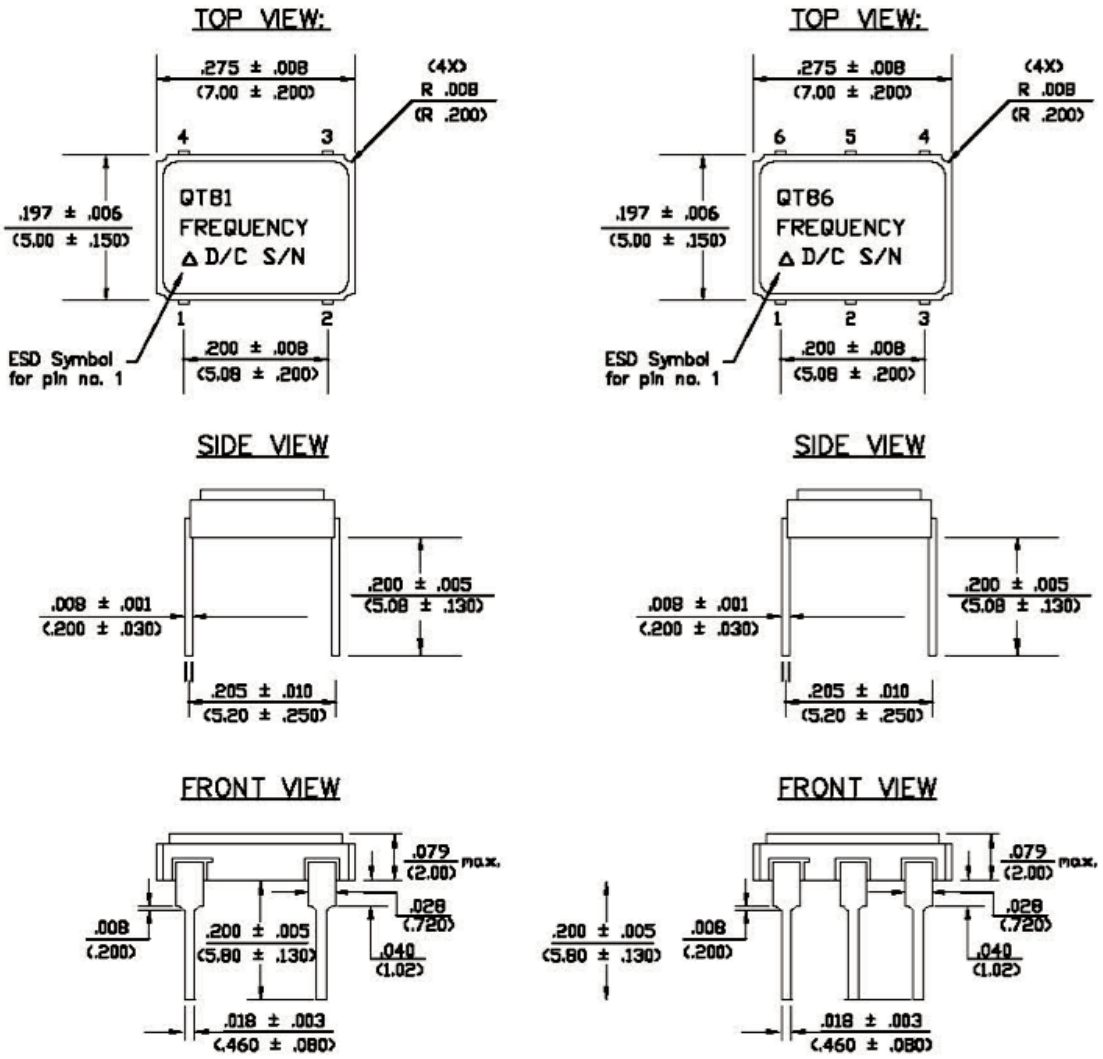


Figure 4 – QT81 and QT86 Form Drawing and Pin Outputs

QT81 (4 Leads)	
Pin No.	**Function**
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT86 (6 Leads)	
Pin No.	**Function**
1	NC or ED
2	NC
3	GND/CASE
4	OUTPUT
5	NC
6	VDD

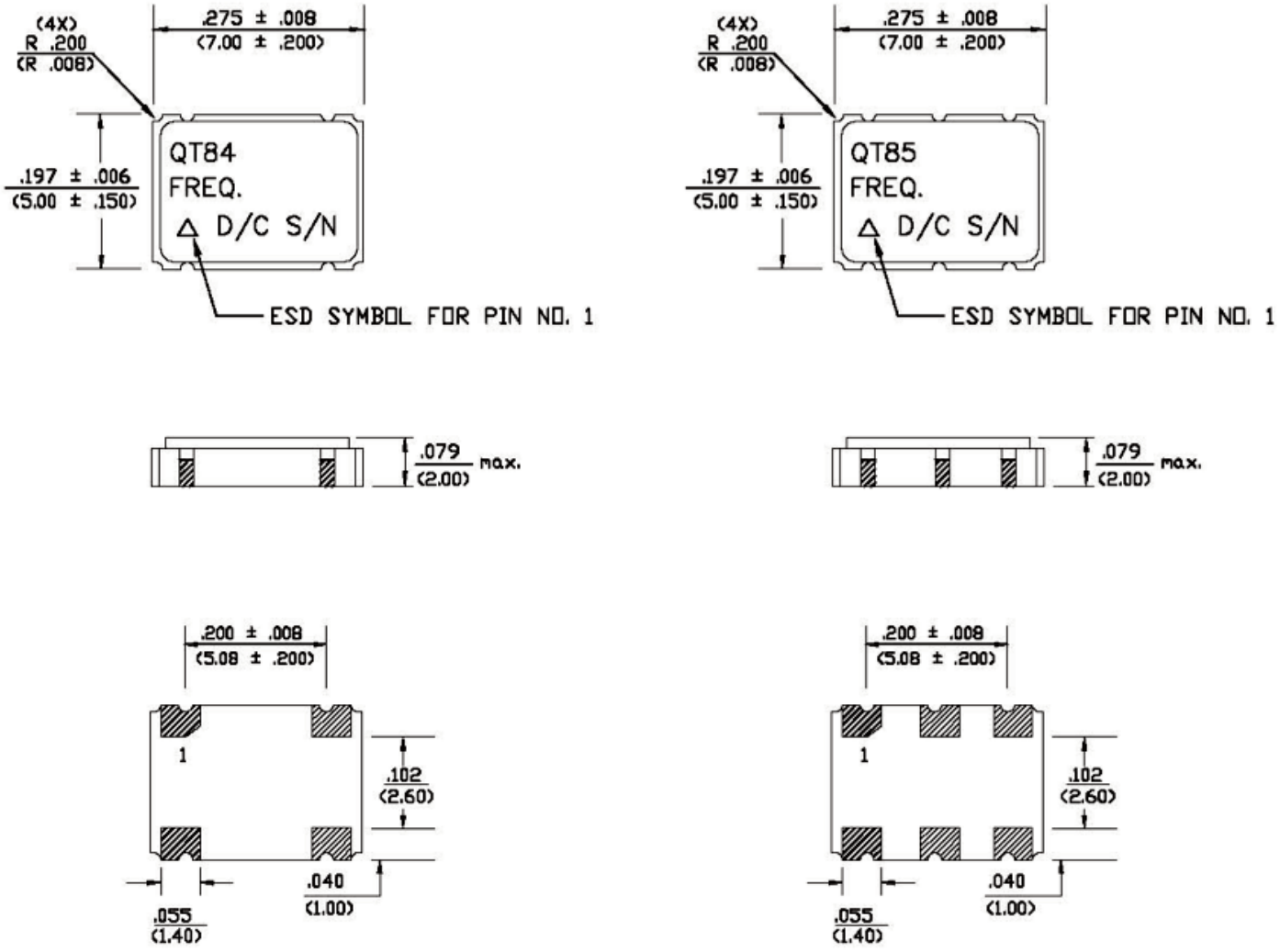


Figure 5 – QT84 and QT85 Form Drawing and Pin Outputs

QT84 (SMT 4 Pads)	
Pin No.	**Function**
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT85 (SMT 6 Pads)	
Pin No.	**Function**
1	NC or ED
2	NC
3	GND/CASE
4	OUTPUT
5	NC
6	VDD

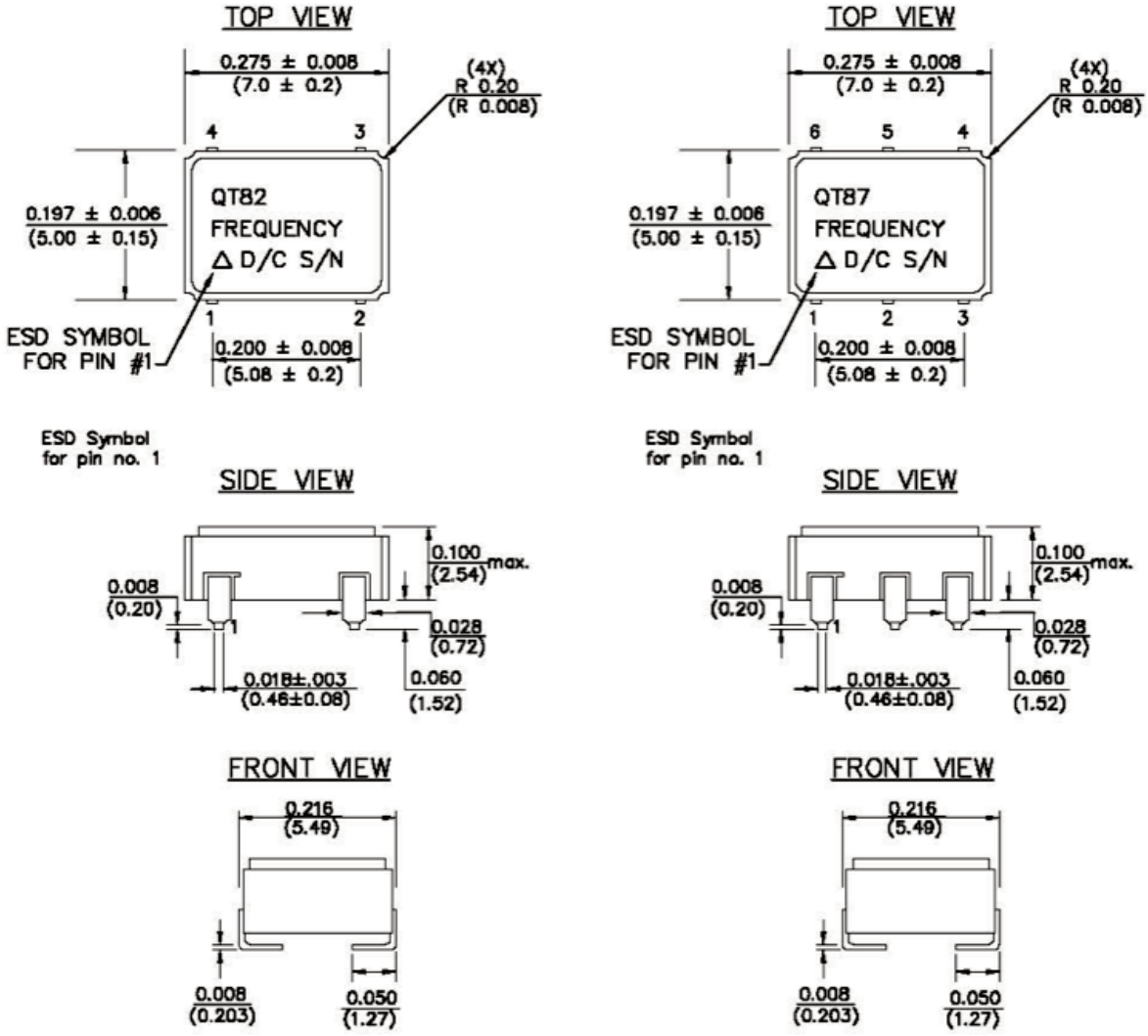


Figure 6 – QT82 and QT87 Form Drawing and Pin Outputs

QT82 (Lead Formed, 4 Leads)	
Pin No.	**Function**
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT87 (Lead Formed, 6 Leads)	
Pin No.	**Function**
1	NC or ED
2	NC
3	GND/CASE
4	OUTPUT
5	NC
6	VDD

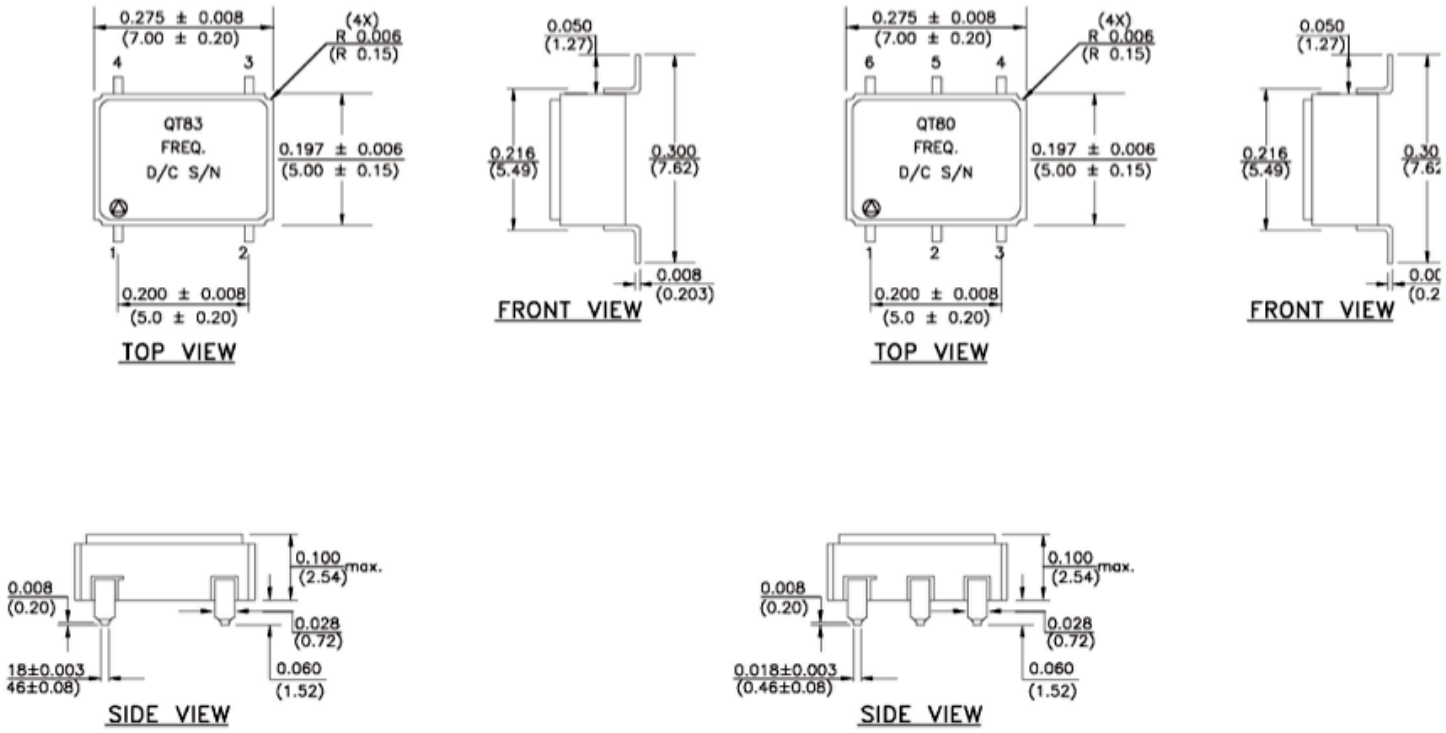


Figure 7 – QT83 and QT80 Form Drawing and Pin Outputs

QT83 (Lead Formed, 4 Leads)	
Pin No.	**Function**
1	NC or ED
2	GND/CASE
3	OUTPUT
4	VDD

QT80 (Lead Formed, 6 Leads)	
Pin No.	**Function**
1	NC or ED
2	NC
3	GND/CASE
4	OUTPUT
5	NC
6	VDD

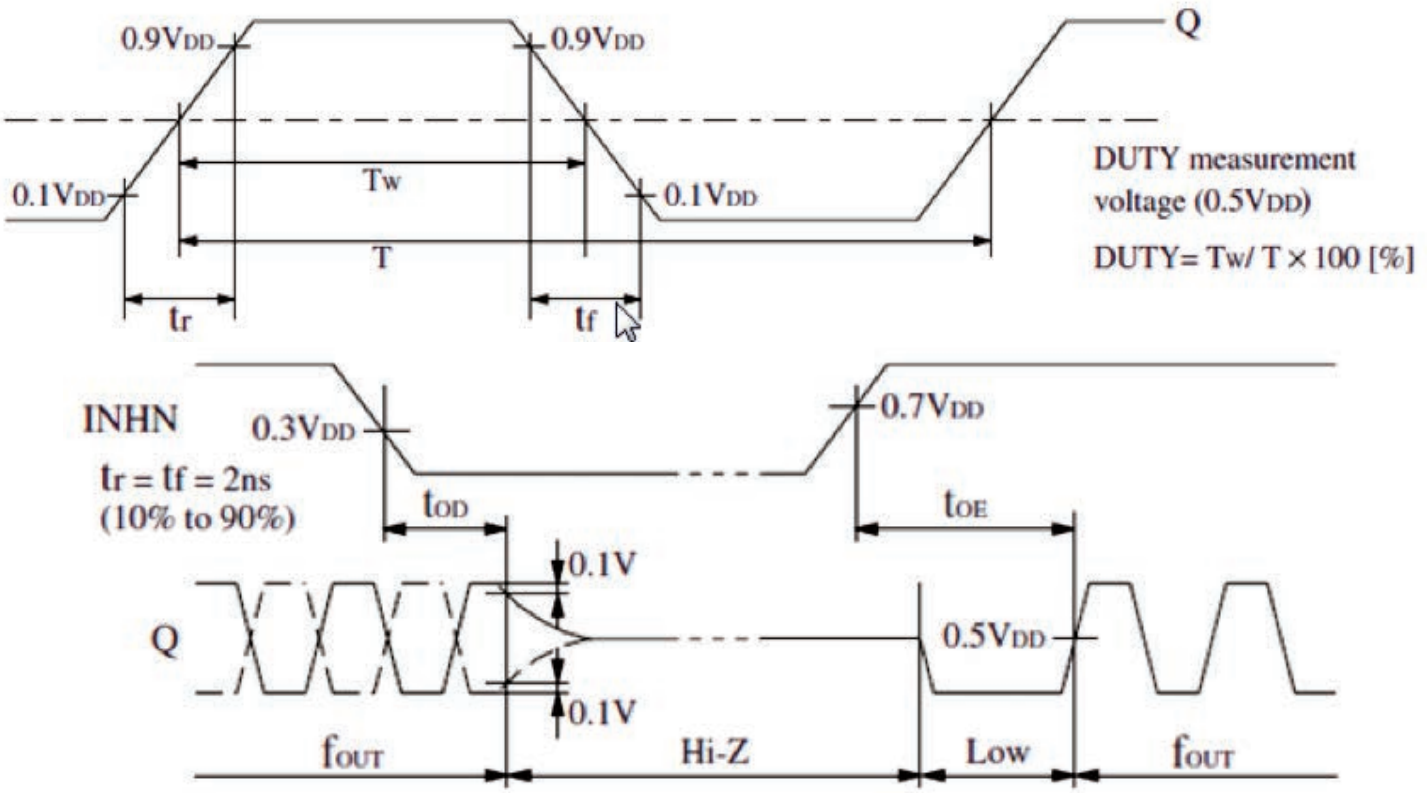


Figure 8 – Output Switching Waveform (Top) and Output Disable Timing Chart (Bottom)

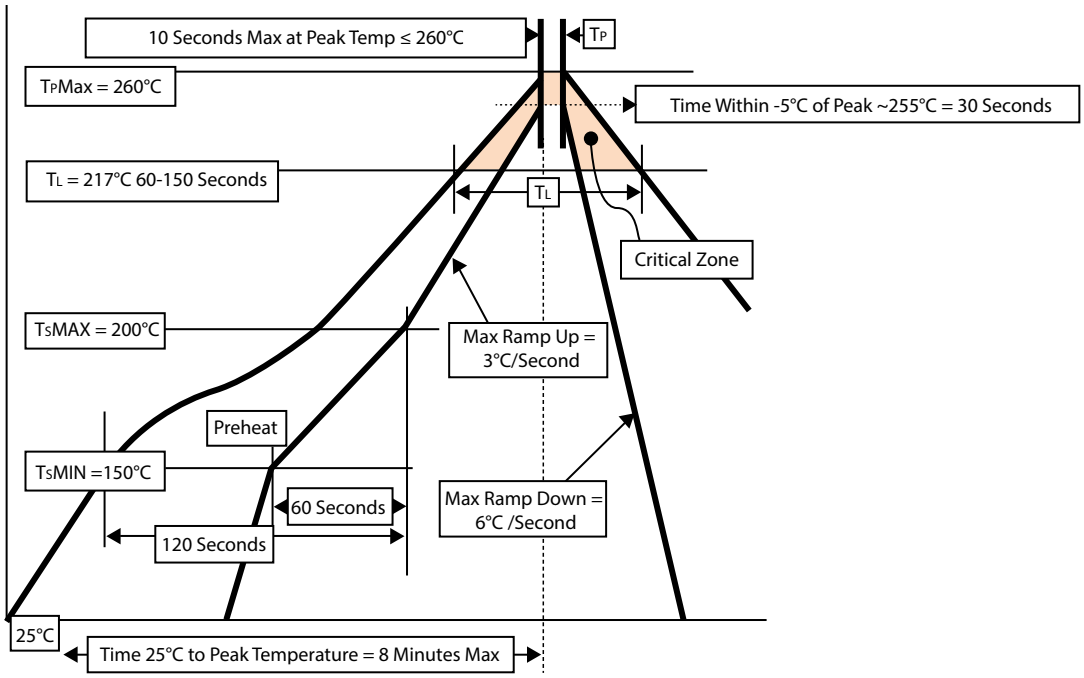


Figure 9 – Solder Reflow Profile Reflow Profile per IPC/JEDEC J-STD-020D.1, 240°C Reflow Profile Also Acceptable

ENVIRONMENTAL AND MECHANICAL TEST SPECIFICATIONS

TEST	SPECIFICATION
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Solderability	MIL-STD-883, Method 2003
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition B
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A1
Solvent Resistance	MIL-STD-202, Method 215
Moisture Sensitivity Level	MSL = 1
Contact Pads	Gold (Au 60µin) Over Nickel (Ni 100-250µin) or Solder Dip Sn60Pb40/SAC305 Lead Free
ESD	Proper ESD Precautions Should be Taken When Handling and Mounting Crystal Oscillators. Built in ESD Protection Circuitry Ratings are as Follows: HBM Class 1C 1,999V per MIL-STD-883, Method 3015.7