HARRIS SEMICONDUCTOR

HFA1205, HFA1245

ADVANCE INFORMATION

August 1993

Dual High-Speed, Low Power, Current Feedback Operational Amplifiers

Features

- Differential Gain 0.02%
- Differential Phase. . . . . 0.02 Deg.
- Wide -3dB Bandwidth (A_V = +2) 350MHz
- Very Fast Slew Rate (A_V = -1) 1100V/μs
- Low Supply Current. . . . . .6mA/Op Amp
- Excellent Gain Flatness (to 50 MHz) . . . . . ±0.04dB
- Individual Output Enable/Disable (HFA1245)

Applications

- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Radar/IF Processing
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- Flash Converter Drivers
- High Speed Pulse Amplifiers

Description

The HFA1205 and HFA1245 are dual versions of the popular HFA1105 and HFA1145 high speed, low power current feedback operational amplifiers.

The HFA1205 comes in a standard 8 lead dual Op Amp pinout. The HFA1245 features separate TTL/CMOS compatible disable control pins for each amplifier, which when pulled low, reduces the supply current and puts the output into a high impedance state.

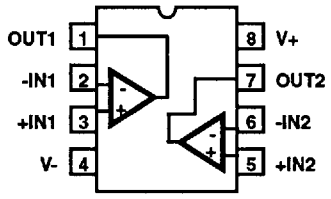
These dual, high performance amplifiers are power and board space savers for users of fast single Op Amps such as the CLC406, CLC409, CLC410, CLC411, EL2070, EL2170, and OPA623.

Ordering Information

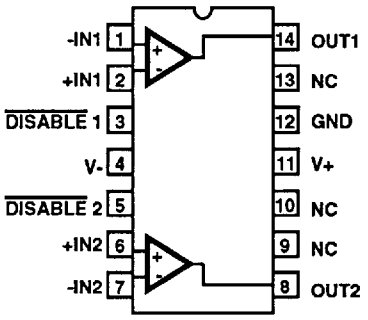
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1205IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1205IB	-40°C to +85°C	8 Lead SOIC
HFA1205MJ/883	-55°C to +125°C	8 Lead Ceramic DIP
HFA1245IP	-40°C to +85°C	14 Lead Plastic DIP
HFA1245IB	-40°C to +85°C	14 Lead SOIC
HFA1245MJ/883	-55°C to +125°C	14 Lead Ceramic DIP

Pinouts

HFA1205
(PDIP, SOIC)
TOP VIEW



HFA1245
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3605

Specifications HFA1205, HFA1245

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage ..... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (Note 1) ..... Short Circuit Protected
Junction Temperature ..... +175°C
Junction Temperature (Plastic Package) ..... +150°C
ESD Rating ..... TBD
Lead Temperature (Soldering 10 sec) ..... +300°C

Operating Conditions

Operating Temperature Range ..... $-40°C \le T_A \le +85°C$
Storage Temperature Range ..... $-65°C \le T_A \le +150°C$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
8 Lead Plastic DIP	98	36
8 Lead SOIC	158	43
14 Lead Plastic DIP	75	-
14 Lead SOIC	110	-

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 500\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified.

PARAMETER	TEST LEVEL (NOTE 2)	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage	A	+25°C	-	2	5	mV
	A	Full	-	-	6	mV
Average Input Offset Voltage Drift	B	Full	-	10	30	µV/°C
Non-Inverting Input Bias Current	A	+25°C	-	6	15	µA
	A	Full	-	-	25	µA
Non-Inverting Input Bias Current Drift	B	Full	-	30	-	nA/°C
Inverting Input Bias Current	A	+25°C	-	1	5	µA
	A	Full	-	-	15	µA
Inverting Input Bias Current Drift	B	Full	-	40	-	nA/°C
Non-Inverting Input Resistance ($\Delta V_{CM} = \pm1.2V$)	A	+25°C	1.0	1.7	-	MΩ
Inverting Input Resistance	C	+25°C	-	66	-	Ω
Input Capacitance (either input)	C	+25°C	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMRR tests)	A	+25°C	1.5	2.0	-	±V
	A	Full	1.2	-	-	±V
Input Noise Voltage Density (f = 10kHz)	B	+25°C	-	3.3	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 10kHz)	B	+25°C	-	2	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (f = 10kHz)	B	+25°C	-	25	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Open Loop Transimpedance Gain ($A_V = -1$)	B	+25°C	100	500	-	kΩ
	B	Full	50	-	-	kΩ
Inverting Input Bias Current Common-Mode Sensitivity ($\Delta V_{CM} = \pm1.2V$)	A	+25°C	-	2	4	µA/V
	A	Full	-	-	10	µA/V
Input Offset Voltage Common-Mode Rejection Ratio ($\Delta V_{CM} = \pm1.2V$)	A	+25°C	45	56	-	dB
	A	Full	-	-	-	dB
-3dB Bandwidth ($A_V = +1$, $R_S = 500\Omega$, $R_F = 500\Omega$, $V_{OUT} = 0.2V_{P-P}$)	B	+25°C	-	300	-	MHz
-3dB Bandwidth ($A_V = +2$, $R_F = 500\Omega$, $V_{OUT} = 0.2V_{P-P}$)	B	+25°C	-	350	-	MHz

Specifications HFA1205, HFA1245

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 500Ω, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST LEVEL (NOTE 2)	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
-3dB Bandwidth (A_V = -1, R_F = 500Ω, V_{OUT} = 0.2V_{P-P})	B	+25°C	-	250	-	MHz
Gain Flatness (to 50MHz, V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	±0.04	-	dB
Gain Flatness (to 75MHz, V_{OUT} = 0.2V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	±0.12	-	dB
Minimum Stable gain	C	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing (A_V = -1)	A	+25°C	3.0	3.2	-	V
	A	Full	2.8	-	-	V
Output Current - implied by output voltage swing into 50Ω (A_V = -1, R_L = 50Ω)	A	+25°C	50	-	-	mA
	A	Full	28	-	-	mA
Output Short Circuit Current (A_V = -1)	A	+25°C	60	80	-	mA
	A	Full	50	-	-	mA
Second Harmonic Distortion (20MHz, V_{OUT} = 2V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	50	-	dBc
Third Harmonic Distortion (20MHz, V_{OUT} = 2V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	55	-	dBc
Third Order Intermodulation Intercept (20MHz, A_V = +2, R_F = 500Ω)	B	+25°C	-	35	-	dBm
1dB Gain Compression (20MHz, A_V = +2)	B	+25°C	-	20	-	dBm
TRANSIENT RESPONSE						
Rise Time (V_{OUT} = 0.5V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	900	-	ps
Overshoot (V_{OUT} = 2V_{P-P}, A_V = +2, R_F = 500Ω, V_{IN} t_{RISE} = 1.0ns)	B	+25°C	-	15	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, R_F = 500Ω)	B	+25°C	-	800	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2, R_F = 500Ω)	B	+25°C	-	900	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1, R_F = 500Ω)	B	+25°C	-	1100	-	V/µs
0.1% Settling Time (V_{OUT} = +2V to 0V step, A_V = +2, R_F = 500Ω)	B	+25°C	-	12	-	ns
Overload Recovery Time (A_V = +2, R_F = 500Ω, V_{IN} = ±2V to 0V step)	B	+25°C	-	8	-	ns
VIDEO CHARACTERISTICS						
Differential Gain (f = 3.58MHz, A_V = +2, R_F = 500Ω, R_L = 150Ω)	B	+25°C	-	0.02	-	%
Differential Phase (f = 3.58MHz, A_V = +2, R_F = 500Ω, R_L = 150Ω)	B	+25°C	-	0.02	-	Degrees
POWER SUPPLY CHARACTERISTICS						
Power Supply Range	C	+25°C	4.5	-	5.5	±V
Power Supply Current	A	+25°C	5.6	5.9	6.0	mA/ Op Amp
	A	Full	-	-	6.2	mA/ Op Amp

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 500Ω, R_L = 100Ω, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST LEVEL (NOTE 2)	TEMP	ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
Non-Inverting Input Bias Current Power Supply Sensitivity (ΔV_{PS} = ±1.25V)	A	+25°C	-	0.5	1	µA/V
	A	Full	-	-	3	µA/V
Inverting Input Bias Current Power Supply Sensitivity (ΔV_{PS} = ±1.25V)	A	+25°C	-	1.6	4	µA/V
	A	Full	-	-	8	µA/V
Input Offset Voltage Power Supply Rejection Ratio (ΔV_{PS} = ±1.25V)	A	+25°C	47	60	-	dB
	A	Full	-	-	-	dB
HFA1245 DISABLE CHARACTERISTICS						
Supply Current ($V_{\overline{DISABLE}}$ = 0V)	A	Full	-	3	4	mA/ Op Amp
$\overline{DISABLE}$ Input Logic Low Voltage	A	Full	-	-	0.8	V
$\overline{DISABLE}$ Input Logic High Voltage	A	+25°C	2.0	-	-	V
	A	Full	2.4	-	-	V
$\overline{DISABLE}$ Input Logic Low Current ($V_{\overline{DISABLE}}$ = 0V)	A	Full	-200	-	200	µA
$\overline{DISABLE}$ Input Logic High Current ($V_{\overline{DISABLE}}$ = 5V)	A	Full	-	-	15	µA
Output Disable Time (V_{IN} = ±1V)	B	+25°C	-	60	-	ns
Output Enable Time (V_{IN} = ±1V)	B	+25°C	-	180	-	ns
Output Capacitance ($V_{\overline{DISABLE}}$ = 0V, V_{OUT} = 5V_{P-P}, 3V/ns)	B	+25°C	-	3	-	pF
Output Leakage ($V_{\overline{DISABLE}}$ = 0V, V_{IN} = ∓2.5V, V_{OUT} = ±2.5V)	A	Full	-10	-	10	µA
Feedthrough ($V_{\overline{DISABLE}}$ = 0V, V_{IN} = 1V_{P-P}, 5MHz, A_V = +2)	B	+25°C	-	-75	-	dBc

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.

Application Information

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Packaging

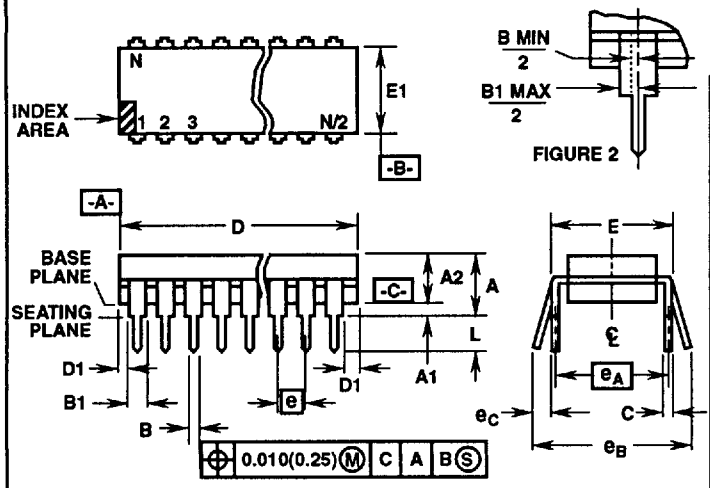


FIGURE 2

FIGURE 1

E8.3 (JEDEC MS-001-AB)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.348	0.430	8.84	10.92	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	8		8		8

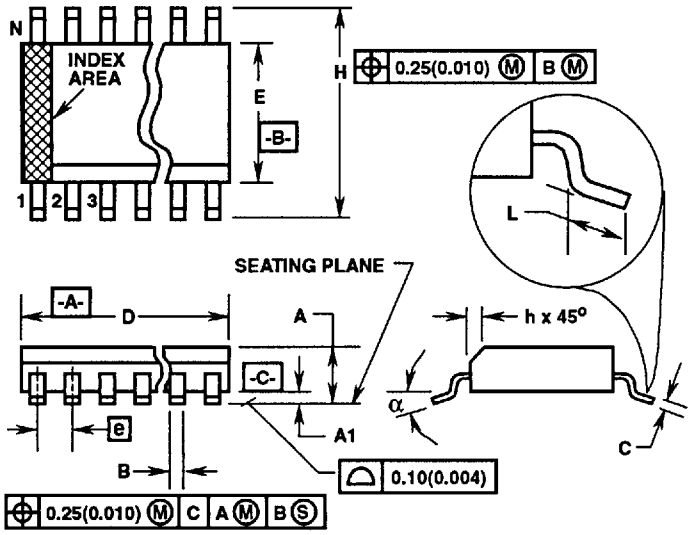
NOTES:

1. Controlling Dimensions: Inch. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to plane C.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. N is the maximum number of terminal positions.
9. Corner leads (1, N, N/2 and N/2 + 1) may be configured as shown in Figure 2.

E14.3 (JEDEC MS-001-AC)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	9
C	0.008	0.015	0.204	0.381	-
D	0.725	0.795	18.42	20.19	5
D1	0.005	-	0.13	-	-
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.160	2.93	4.06	4
N	14		14		8

Packaging



M8.15 (JEDEC MS-012-AA)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

M14.15 (JEDEC MS-012-AB)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.