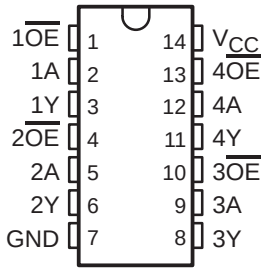
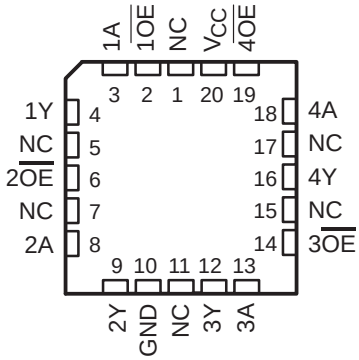
- **High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC125 . . . J OR W PACKAGE
SN74HC125 . . . D, DB, OR N PACKAGE
(TOP VIEW)



SN54HC125 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

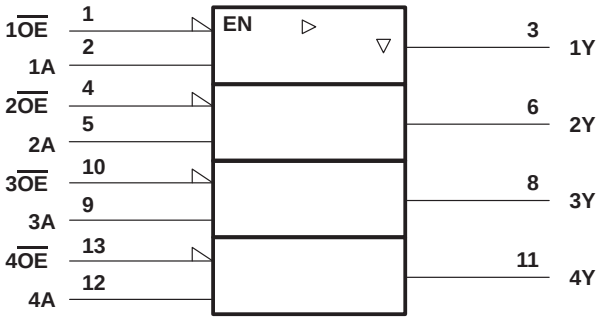
These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

The SN54HC125 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC125 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each buffer)

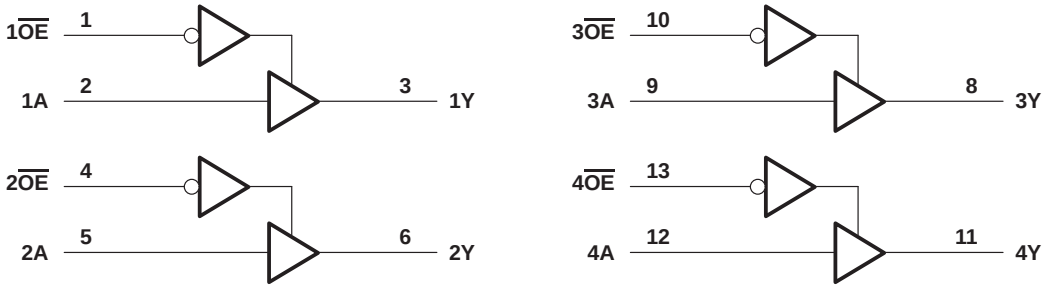
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 127°C/W
DB package . . . . . 158°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC125			SN74HC125			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.01		±10		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		48	120		150		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		25		26	
t_{en}	$\overline{OE}$	Y	2 V		53	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t_{dis}	$\overline{OE}$	Y	2 V		30	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		14	20		31		26	
t_t		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

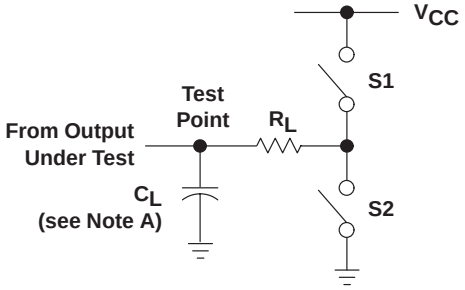
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		67	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		32	
t_{en}	$\overline{OE}$	Y	2 V		100	135		200		170	ns
			4.5 V		20	27		40		34	
			6 V		17	23		34		29	
t_t		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics, T_A = 25°C

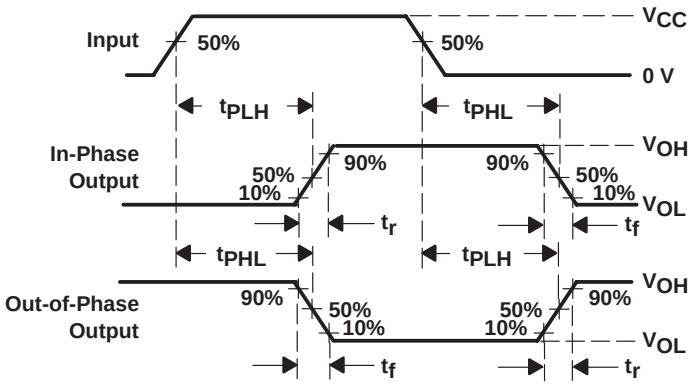
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	45	pF

PARAMETER MEASUREMENT INFORMATION

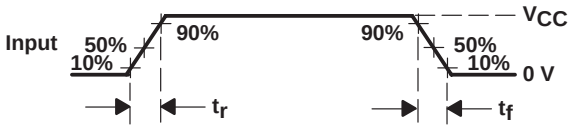


LOAD CIRCUIT

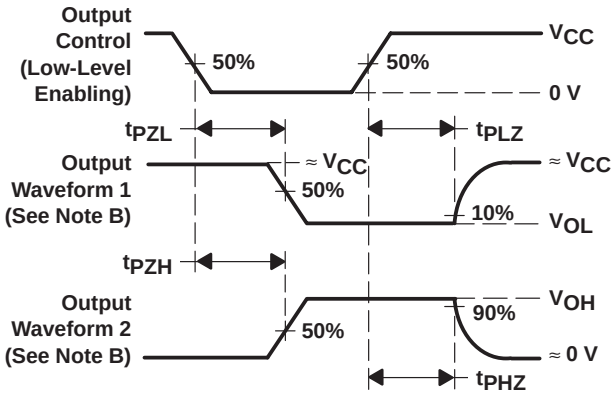
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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SN74HC125, Quadruple Bus Buffer Gates With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HC125	SN74HC125
Voltage Nodes (V)	6, 5, 2	6, 5, 2
Vcc range (V)	2.0 to 6.0	2.0 to 6.0
Input Level	CMOS	CMOS
Output Level	CMOS	CMOS
Output Drive (mA)		-6/6
tpd max (ns)		26
Static Current		0.08

FEATURES

Back to Top

- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

DESCRIPTION

Back to Top

These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE\) input is high.

The SN54HC125 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC125 is characterized for operation from -40°C to 85°C.

TECHNICAL DOCUMENTS

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn74hc125.pdf (93 KB,Rev.B) (Updated: 05/01/1997)

APPLICATION NOTES

Back to Top

View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)

- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 - Updated: 05/01/1996)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 - Updated: 09/07/2001)
- Timing Differences of 10-pF Versus 50pF Loading (SCEA004 - Updated: 11/01/1996)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

Back to Top

View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HC125D	SOP (D)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC125DBR	SSOP (DB)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC125N	PDIP (N)	14	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

Back to Top

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74HC125D	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.22	50	N/A*	10k | 22 Oct	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								3000 | 25 Oct		DigiKey | AMERICA	604	BUY NOW
								>10k | 28 Oct				
SN74HC125DBLE	OBSOLETE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HC125DBR	ACTIVE	SSOP (DB) | 14	-40 TO 85	View Contents	1KU | 0.22	2000	N/A*		2 WKS			
SN74HC125DR	ACTIVE	SOP (D) | 14	-40 TO 85	View Contents	1KU | 0.22	2500	N/A*	5000 | 26 Sep	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 07 Oct		DigiKey | AMERICA	>1k	BUY NOW
								>10k | 21 Oct				
								>10k | 25 Oct				
SN74HC125N	ACTIVE	PDIP (N) | 14	-40 TO 85	View Contents	1KU | 0.22	25	N/A*	>10k | 22 Oct	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 29 Oct		DigiKey | AMERICA	229	BUY NOW

SN74HC125N3	OBSOLETE	PDIP (N) | 14	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HC125NSR	ACTIVE	SOP (NS) | 14		View Contents	1KU | 0.25	2000	N/A*	2000 | 26 Sep	2 WKS			
								>10k | 25 Oct				

Table Data Updated on: 9/26/2002