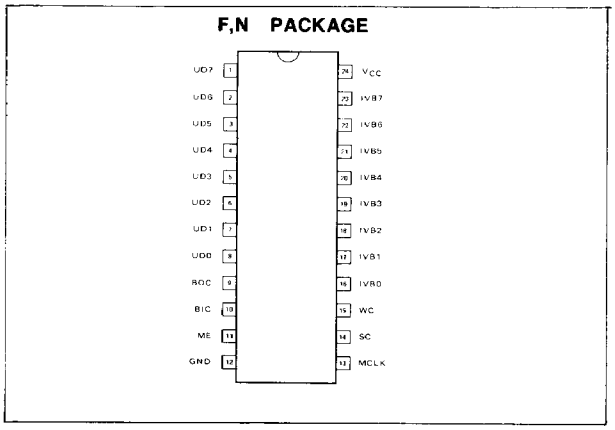
DESCRIPTION

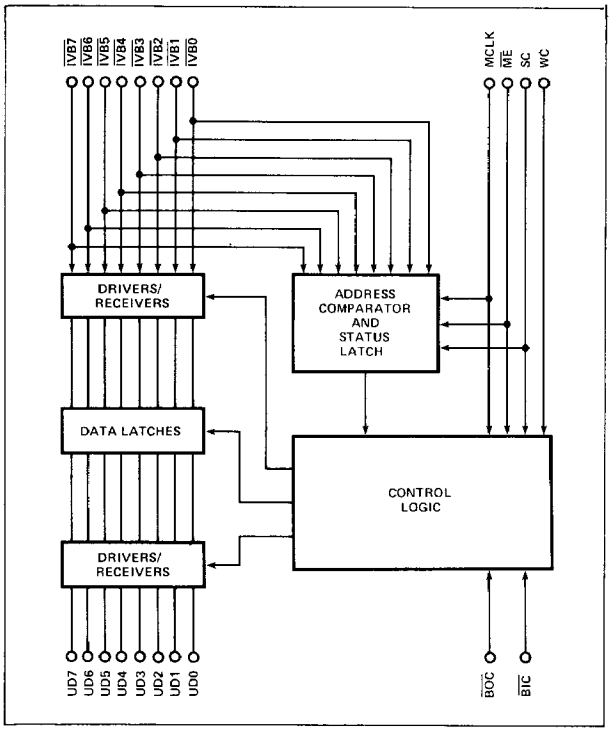
The Interface Vector (IV) Byte is an 8-bit bi-directional data register designed to function as an I/O interface element in microprocessor systems. It contains eight clocked data latches accessible from either a microprocessor (IV) port or a user port. Separate I/O control is provided for each port. The two ports operate independently, except when both are attempting to input data into the IV Byte. In this case, the user port has priority.

A unique feature of the IV Byte is the way in which it is addressed. Each IV Byte has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the IV Byte's internally programmed address, the microprocessor port is enabled, allowing data transfer through it. The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 IV Bytes to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

USER DATA BUS CONTROL

The activity of the User Data Bus is controlled by the $\overline{BIC}$ and $\overline{BOC}$ inputs as shown in Table 1. (H represents high, L represents low.)

Table 1
BIC and BOC function Control

$\overline{BIC}$	$\overline{BOC}$	MCLK	USER DATA BUS
H	L	X	Output Data
L	X	H	Input Data
L	X	L	Inactive
H	H	X	Inactive

To avoid conflicts at the Data Latch, input from the microprocessor port is inhibited when $\overline{BIC}$ indicates user data is being input. Under all other conditions, the two ports operate independently.

INTERFACE VECTOR BUS CONTROL

As is shown in Table 2, the activity of the microprocessor port (IV Bus) is controlled by the $\overline{ME}$, SC, WC and $\overline{BIC}$ inputs, as well as the state of an internal status latch. $\overline{BIC}$ is included to show user port priority over the microprocessor port for data input.

TABLE 2
MICROPROCESSOR PORT FUNCTION CONTROL

ME	SC	WC	MCLK	$\overline{BIC}$	Status Latch	IVBX Function
L	L	L	X	X	SET	Output Data
L	L	H	H	H	SET	Input Data
L	H	L	H	X	X	Input Address
L	H	H	H	L	X	Input Address
L	H	H	H	H	X	Input Data and Address
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	not set	Inactive
H	X	X	X	X	X	Inactive

Each IV Byte's status latch stores the result of the most recent IV Byte select; it is set when the IV Byte's internal address matches the IV Bus. It is cleared when an address that differs from the internal address is presented on the IV Bus. In normal operation, the state of the status latch acts like a master enable; the microprocessor port can transfer data only when the status latch is set.

When SC and WC are both high, data on the IV Bus is accepted as data, whether or not the IV Byte was selected. The data is also interpreted as an address. The IV Byte sets its select status if its address matches the data read when SC and WC were both high; it resets its select status otherwise.

BUS OPERATION

Data written into the IV Byte from one port will appear inverted when read from the other port. Data written into the IV Byte from one port will not be inverted when read from the same port.

Figure 1 shows various ways to use the IV Byte in a system by controlling the states of the $\overline{BIC}$ and $\overline{BOC}$ lines. BYTE 1 is for input only, BYTE 2 is for output only, BYTE 3 is bidirectional under user control. BYTE 4 is output only (6 bits) with two bits reserved for system control of BYTE 5.

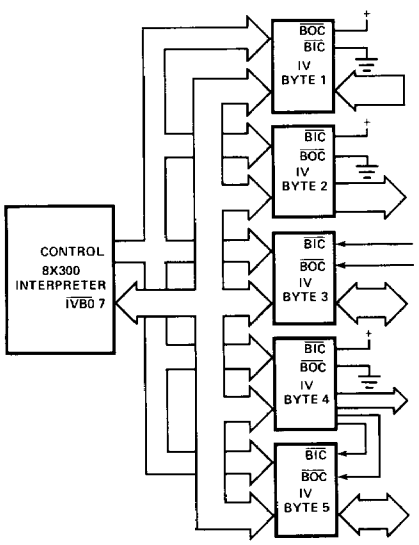
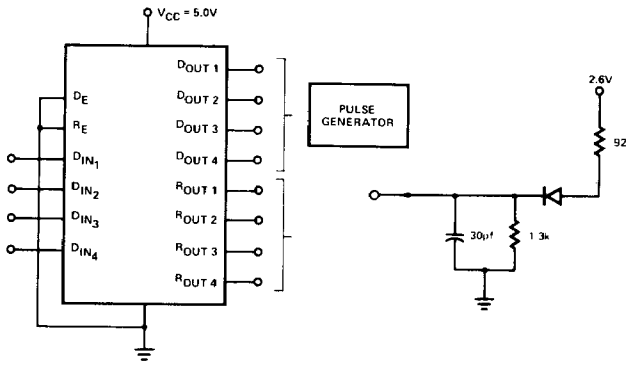
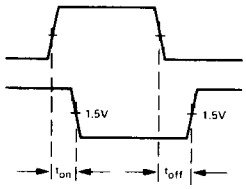


FIGURE 1
SOME IV BYTE CONFIGURATIONS

AC TEST CIRCUITS AND WAVEFORMS

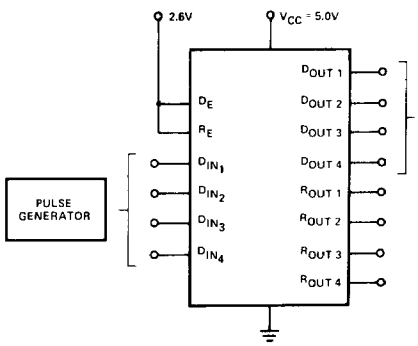
PROPAGATION DELAY (D_{OUT} TO R_{OUT})

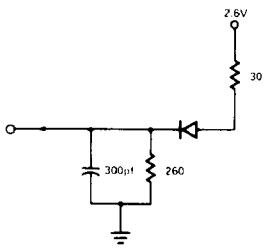


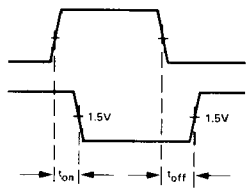


INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (D_{IN} TO D_{OUT})

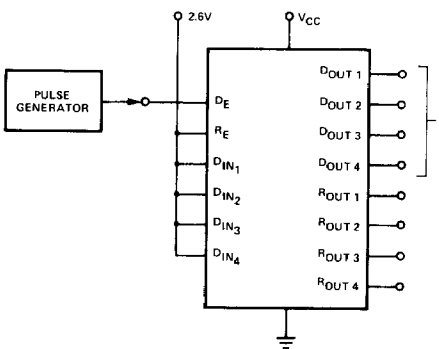


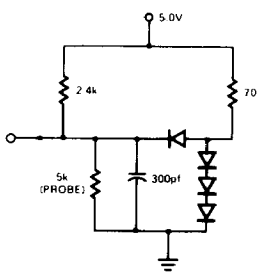


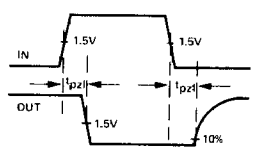


INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 10MHz (50% duty cycle)
Amplitude = 2.6V

PROPAGATION DELAY (DATA ENABLE TO DATA OUTPUT)







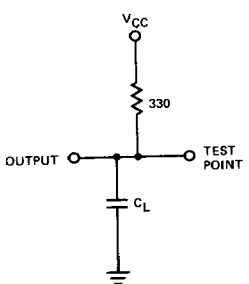
INPUT PULSE:
$t_r = t_f$ = 5ns (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1-8	$\overline{UD0}$ — $\overline{UD7}$:	User Data I/O Lines. Bidirectional data lines to communicate with user's equipment. Either tri-state or open collector outputs are available.	ACTIVE HIGH
16-23	$\overline{IVB0}$ — IVB7:	Interface Vector Bus. Bidirectional tri-state data lines to communicate with controlling digital system (microprocessor).	ACTIVE LOW
10	$\overline{BIC}$:	Byte Input Control. User input to control writing into the IV Byte from the User Data Lines.	ACTIVE LOW
9	BOC:	Byte Output Control. User input to control reading from the IV Byte onto the User Data Lines.	ACTIVE LOW
14	SC:	Selected Command. When SC is high and WC is low, data on IVB0 — IVB7 is interpreted as an address. IV Byte selects itself if its address is identical to IV bus data; it de-selects itself otherwise.	ACTIVE HIGH
15	$\overline{WC}$:	Write Command. When WC is high and SC is low, IV Byte, if selected, stores contents of IVB0 — IVB7 as data.	ACTIVE HIGH
11	ME:	Master Enable. System input to enable or disable all other system inputs and outputs. It has no effect on user inputs and outputs.	ACTIVE LOW
13	MCLK:	Master Clock. Input to strobe data into the latches.	
24	VCC:	5 volt power connection.	
12	GND:	Ground.	

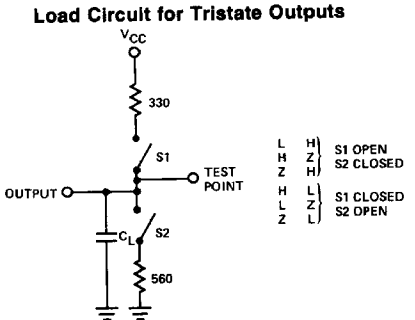
PARAMETER MEASUREMENT INFORMATION

Load Circuit for Open Collector Outputs



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

Load Circuit for Tristate Outputs



NOTE: ALL RESISTORS VALUES ARE TYPICAL AND IN OHMS.

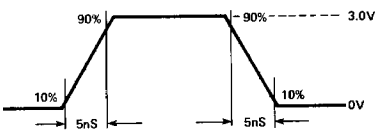
AC ELECTRICAL CHARACTERISTICS

(Limits apply for V_{CC} = 5V ± 5% and 0° C ≤ T_A ≥ 70° C unless specified otherwise.)

Parameter	Symbol	Input	Output	Conditions	Limits			Units
					Min.	Typ.	Max.	
User Data Delay (Note 1)	t_{PD}	UDX	$\overline{IVBX}$	C_L = 30pF		19		ns
		MCLK	$\overline{IVBX}$	C_L = 30pF		36		ns
User Output Enable	t_{OE}	$\overline{BIC}$	UDX	C_L= 30pF		26		ns
		$\overline{BOC}$	UDX	C_L = 30pF		28		ns
User Output Disable	t_{OD}	$\overline{BIC}$	UDX	C_L = 30pF		22		ns
		$\overline{BOC}$	UDX	C_L = 30pF		13		ns
IV Data Delay (Note 1)	t_{PD}	$\overline{IVBX}$	UDX	C_L = 30pF		32		ns
		MCLK	UDX	C_L = 30pF		40		ns
IV Output Enable	t_{OE}	$\overline{ME}$	$\overline{IVBX}$	C_L = 30pF		16		ns
		SC	$\overline{IVBX}$	C_L = 30pF		16		ns
		WC	$\overline{IVBX}$	C_L = 30pF		16		ns
IV Output Disable	t_{OD}	$\overline{ME}$	$\overline{IVBX}$	C_L = 30pF		15		ns
		SC	$\overline{IVBX}$	C_L = 30pF		15		ns
		WC	$\overline{IVBX}$	C_L = 30pF		15		ns
Clock Pulse Width	t_W	MCLK				20		ns
Setup Time (2)	t_{SETUP}	UDX				9		ns
		$\overline{BIC}$				22		ns
		$\overline{IVBX}$		(Note 5)		37		ns
		$\overline{ME}$		(Note 5)		23		ns
		SC		(Note 5)		23		ns
		WC		(Note 5)		12		ns
Hold Time (2)	t_{HOLD}	UDX		(Note 5)		16		ns
		$\overline{BIC}$		(Note 5)		3		ns
		$\overline{IVBX}$		(Note 5)		11		ns
		$\overline{ME}$		(Note 5)		0		ns
		SC		(Note 5)		0		ns
		WC		(Note 5)		4		ns

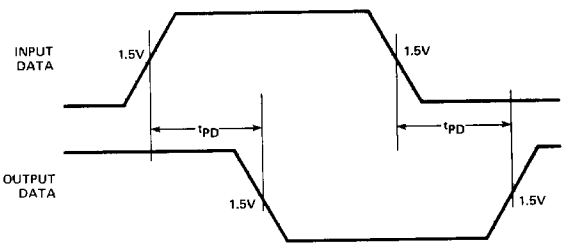
NOTES:
1. Data delays referenced to the clock are valid only if the input data is stable at the arrival of the clock and the hold time requirement is met.
2. Setup and hold times given are for "normal" operation. $\overline{BIC}$ setup and hold times are for a user write operation. SC setup and hold times are for an IV Byte select operation. WC setup and hold times are for an IV Bus write operation. ME setup and hold times are for both IV write and select operations.

INPUT WAVEFORM

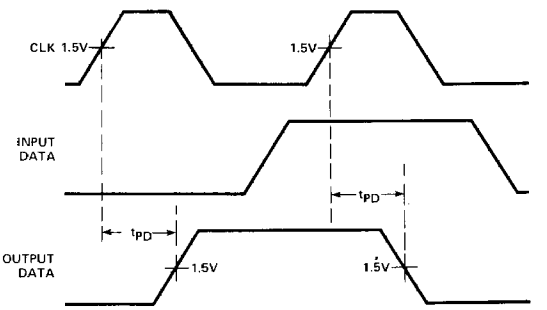


CLOCK PULSE WIDTH

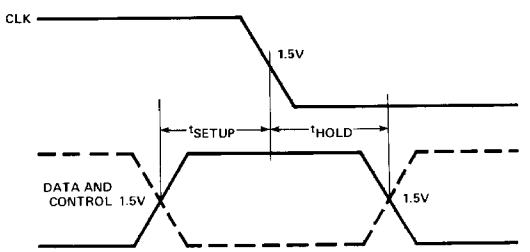
DATA DELAY TIMES
(INPUT DATA REFERENCED—CLK = '1')



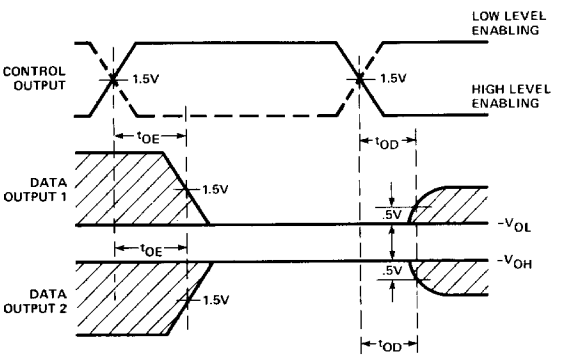
DATA DELAY TIMES
(CLOCK REFERENCED)



SETUP AND HOLD TIMES



OUTPUT ENABLE AND DISABLE TIMES
(TRISTATE OUTPUTS)



WAVEFORM #1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW WHEN THE TRI-STATE DRIVER IS ENABLED. WAVEFORM #2 IS FOR THE OPPOSITE CONDITION.

ADDRESS PROGRAMMING

The IV Byte is manufactured such that an address of all high-levels (> 2V) on the IV Data Bus inputs matches the Byte's internal address. To program a bit so a low-level input (< 0.8V) matches, the following procedure should be used:

1. Set all control inputs to their inactive state (BIC = BOC = ME = V_{CC}, SC = WC = MCLK = GND). Leave all IV Data Bus I/O pins open.
2. Raise V_{CC} to 7.75 V ± .25V.
3. After V_{CC} has stabilized, apply a programming pulse to the User Data Bus bit where a low-level match is desired. The voltage should be limited to 18V; the current should be limited to 75 mA. Apply the pulse as shown in Diagram 1.
4. Return V_{CC} to 0V (Note 6).

5. Repeat this procedure for each bit where a low-level match is desired.
6. Verify that the proper address is programmed by setting the Byte's status latch (IVB0 — IVB7 = desired address, ME = WC = L, SC = MCLK = H) and attempting to write through the IV Byte (BOC = SC = ME = L, BIC = WC = MCLK = H). If the proper address has been programmed, data presented at the IV Bus will appear inverted on the User Bus outputs. (Use normal V_{CC} and input voltages for verification.)

After the desired address has been programmed, a second procedure must be followed to isolate the address circuitry. The procedure is:

1. Set V_{CC} and all control inputs to 0V. (V_{CC} = BIC = BOC = ME = SC WC = MCLK = 0V). Leave all IV Data Bus I/O pins open.
2. Apply a protect programming pulse to every User Data Bus pin, one at a time. The voltage should be limited to 14V; the current should be limited to 150mA. Apply the pulse as shown in Diagram 2.
3. Verify that the address circuitry is isolated by applying 7V to each User Data Bus pin and measuring less than 1mA of input current. The conditions should be the same as in step 1 above. The rise time on the verification voltage must be slower than 100μs.

DIAGRAM 1
ADDRESS PROGRAMMING PULSE

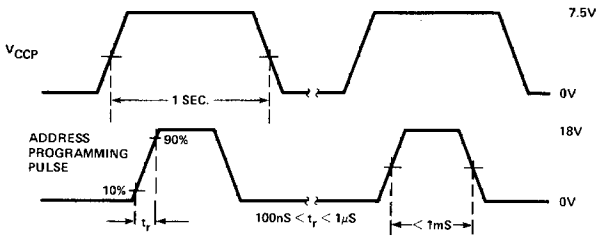
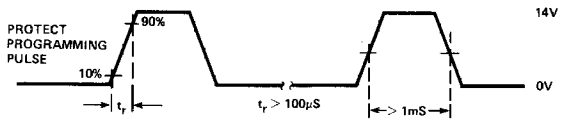


DIAGRAM 2
PROTECT PROGRAMMING PULSE



PROGRAMMING SPECIFICATIONS

Parameter	Symbol	Conditions	Limits Min.	Typ.	Max.	Units
Programming Supply Voltage	V_{CCP}					V
Address			7.5		8.0	V
Protect				0		V
Programming Supply Current	I_{CCP}	V_{CCP} = 8.0V			250	mA
MAX TIME V_{CCP} > 5.25V					1.0	sec.
Programming Voltage						
Address			17.5		18.0	V
Protect			13.5		14.0	V
Programming Current						
Address					75	mA
Protect					150	mA
Programming Pulse Rise Time						
Address			.1		1	μsec
Protect			100			μsec
Programming Pulse Width			.5		1	mS

NOTES:
6. If all programming can be done in less than 1 second, V_{CC} may remain at 7.75V for the entire programming cycle.