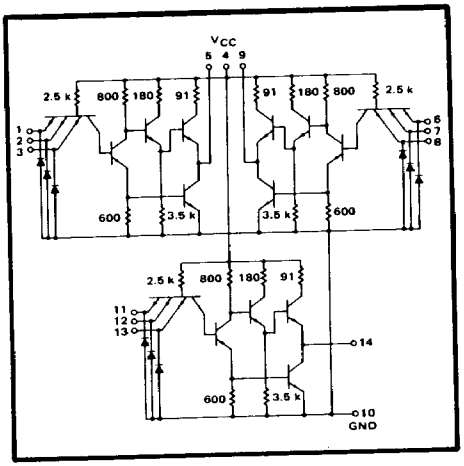
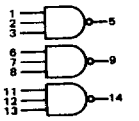
TRIPLE 3-INPUT
"NAND" GATE

MC2107 • MC2157
MC2007 • MC2057



This device consists of three 3-input AND gates driving output inverters. These gates can be used to build a pulse shaping network for interfacing with discrete component circuits.

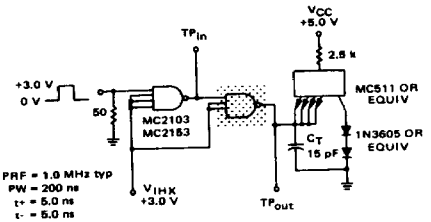


Positive Logic: $5 = \overline{1 + 2 + 3}$
Negative Logic: $5 = \overline{1 + 2 + 3}$

Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 6.0 ns typ

TYPE NO.	INPUT LOADING FACTOR	(I_F)	OUTPUT DRIVE		(I_{OL})	TEMPERATURE RANGE
MC2107 MC2157	1	(-2.0 mA)	11 6	MC2100 series Gates MC2100 series Gates	(22 mA) (12 mA)	−55°C to +125°C
MC2007 MC2057	1	(-2.5 mA)	9 5	MC2000 series Gates MC2000 series Gates	(22.5 mA) (12.5 mA)	0° to +75°C

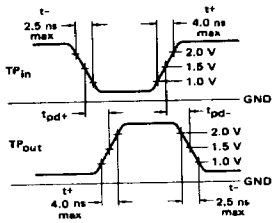
SWITCHING TIME TEST CIRCUIT



PRF = 1.0 MHz typ
PW = 200 ns
t_+ = 5.0 ns
t_- = 5.0 ns

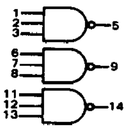
C_T = the total parasitic capacitance which includes probe, wiring, and load capacitances.
Scope rise time < 1.0 ns
Probe capacitance < 5.0 pF
Ground inputs to all gates not under test.

VOLTAGE WAVEFORMS AND DEFINITIONS



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.



TEST CONDITIONS

Device	@ Test Temperature	I_{OL} (mA) Pr*	I_{OL} (mA) Std	I_{OH} (mA) Pr*	I_{OH} (mA) Std	I_{in} (mA)	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}
MC2107*, MC2157	-55°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	2.0	0.9	5.5	5.0	-	-
	+25°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.7	1.1	5.5	5.0	8.0	3.0
	+125°C	22.0	12.0	-2.2	-1.2	1.0	0.45	2.7	4.5	1.4	0.9	5.5	5.0	-	-
MC2007*, MC2057	0°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.9	1.0	5.5	5.0	-	-
	+25°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.8	1.1	5.5	5.0	7.0	3.0
	+75°C	22.5	12.5	-1.8	-1.0	1.0	0.45	2.9	4.5	1.7	1.0	5.5	5.0	-	-

Characteristic	Symbol	Pin Under Test	MC2107, MC2157 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC2007, MC2057 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit
Input Forward Current	I_F	1	-	-2.0	-	-2.0	-	-2.0	-	-2.5	-	-2.5	-	-2.5	mAdc
Leakage Current	I_R	1	-	100	-	100	-	100	-	100	-	100	-	100	µAdc
Inverse Beta Current	I_L	1	-	100	-	100	-	100	-	100	-	100	-	100	µAdc
Breakdown Voltage	$BV_{in\ "0"}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc
	$BV_{in\ "1"}$	1	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	5.5	-	Vdc
Output Output Voltage	$V_{out\ "0"}$	5	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	Vdc
	$V_{out\ "1"}$	5	2.5	-	2.4	-	2.5	-	2.5	-	2.4	-	2.5	-	Vdc
Leakage Current	I_{OLK}	5	-	250	-	250	-	250	-	250	-	250	-	250	µAdc
Short-Circuit Current	I_{SC}	5	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	-25	-100	mAdc
Output Voltage	V_{OL}	5	-	0.40	-	0.40	-	0.45	-	0.40	-	0.40	-	0.45	Vdc
	V_{OH}	5	2.7	-	3.1	-	3.15	-	2.9	-	3.0	-	3.0	-	Vdc
Power Requirements (Total Device) Maximum Power Supply Current	I_{max}	4	-	-	-	19.5	-	-	-	-	-	20.25	-	-	mAdc
Power Supply Drain	I_{PDH}	4	-	22.5	-	22.5	-	22.5	-	30	-	30	-	30	mAdc
	I_{PDL}	4	-	11.25	-	11.25	-	11.25	-	15	-	15	-	15	mAdc
Switching Parameters Turn-On Delay	t_{pd-}	1,5	-	-	-	10	-	-	-	-	-	10	-	-	ns
Turn-Off Delay	t_{pd+}	1,5	-	-	-	10	-	-	-	-	-	10	-	-	ns
Rise Time	t_-	1,5	-	-	-	4.0	-	-	-	-	-	4.0	-	-	ns
Fall Time	t_-	1,5	-	-	-	2.5	-	-	-	-	-	2.5	-	-	ns

TEST CURRENT / VOLTAGE APPLIED TO PINS LISTED BELOW:

Characteristic	Symbol	I_{OL}	I_{OH}	I_{in}	V_{IL}	V_{IH}	V_R	V_{th1}	V_{th0}	V_{out}	V_{CC}	V_{CCH}	V_{IHX}	Gnd†
Forward Current	I_F	-	-	-	-	-	2,3	-	-	-	4	-	-	1,10
Leakage Current	I_R	-	-	-	-	-	1	-	-	-	4	-	-	2,3,10
Inverse Beta Current	I_L	-	-	-	-	-	1	-	-	-	4	-	-	10
Breakdown Voltage	$BV_{in\ "0"}$	-	-	1	-	-	-	-	-	-	4	-	-	10
	$BV_{in\ "1"}$	-	-	1	-	-	-	-	-	-	4	-	-	2,3,10
Output Voltage	$V_{out\ "0"}$	5	-	-	-	-	-	1	-	-	4	-	-	10
	$V_{out\ "1"}$	-	5	-	-	-	-	-	1	-	4	-	-	10
Leakage Current	I_{OLK}	-	-	-	-	-	-	-	-	5	4	-	-	1,2,3,10
Short-Circuit Current	I_{SC}	-	-	-	-	-	-	-	-	-	4	-	-	1,2,3,5,10
Output Voltage	V_{OL}	5	-	-	-	1	-	-	-	-	4	-	-	10
	V_{OH}	-	5	-	1	-	-	-	-	-	4	-	-	10
Maximum Power Supply Current	I_{max}	-	-	-	-	-	-	-	-	-	-	4	-	1,6,10,11
Power Supply Drain	I_{PDH}	-	-	-	-	-	-	-	-	-	4	-	-	10 ‡
	I_{PDL}	-	-	-	-	-	-	-	-	-	4	-	-	1,6,10,11
		Pulse In	Pulse Out											
Turn-On Delay	t_{pd-}	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Turn-Off Delay	t_{pd+}	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Rise Time	t_-	1	5	-	-	-	-	-	-	-	4	-	2,3	10
Fall Time	t_-	1	5	-	-	-	-	-	-	-	4	-	2,3	10

* Prime Fan-Out † Ground inputs to gates not under test, during ALL tests unless otherwise noted. ‡ The inputs to all gates must be ungrounded.

Table 3-4 DSP56001A Identification by Signal Name (Continued)

Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Signal Name	132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.
$\overline{WT}$	45	L13	nc	103	
X/$\overline{Y}$	48	N13	nc	107	
XTAL	126	A6	nc	110	
nc	3		nc	116	
nc	4		nc	117	
nc	7		nc	122	
nc	17		nc	125	
nc	18		nc	132	
nc	21				

Power and ground pins have special considerations for noise immunity. See the section **Design Considerations**.

Table 3-5 DSP56001A Power Supply Pins

132 pin "FC" PQFP or "FE" CQFP Pin No.	88 pin "RC" PGA Pin No.	Power Supply	Circuit Supplied
63	L8	V_{CCN}	Address Bus Buffers
64			
55	L6	GNDN	
56	L9		
73			
74			