Description

The SK10/100E131 is a Quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (CC) LOW and using the Clock Enable (CE*) inputs for clocking. Common clocking is achieved by holding the CE inputs LOW and using CC to clock all four flip-flops. In this case, the CE* inputs perform the function of controlling the common clock to each flip-flop.

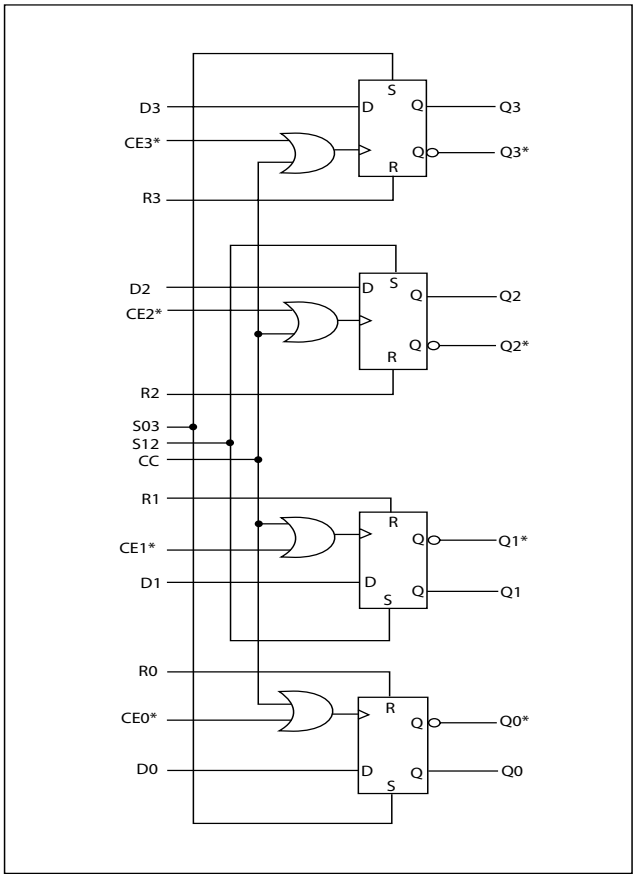
Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both CC and CE* are LOW, and transfers to the slave when either CC or CE (or both) go HIGH.

Features

- 1100 MHz Minimum Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- Extended 100E VEE Range of –4.2V to –5.5V
- Internal 75KΩ Input Pulldown Resistors
- Fully Compatible with MC10/100E131
- Specified Over Industrial Temperature Range: –40°C to +85°C
- ESD Protection of >4000V
- Available in 28-pin PLCC Package

Functional Block Diagram

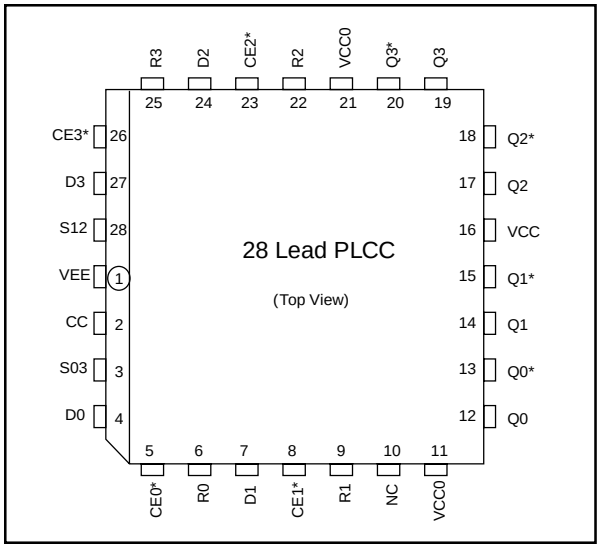


Pin Description

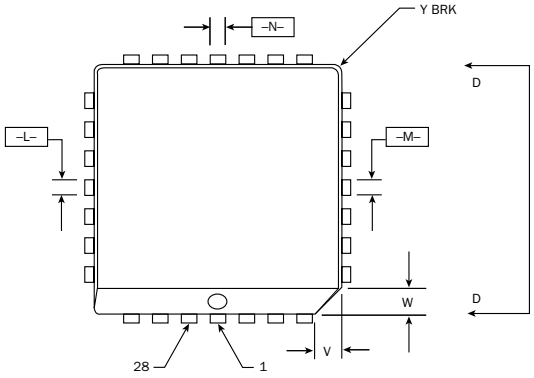
Pin Names

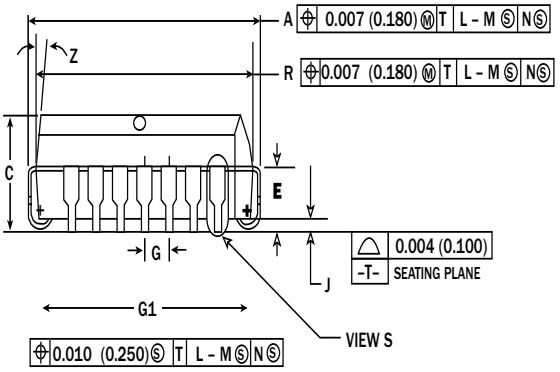
Pin	Function
D0 - D3	Data Inputs
CE0* - CE3*	Clock Enables (individual)
R0 - R3	Resets
CC	Common Clock
S03, S12	Sets (paired)
Q0 - Q3	True Outputs
Q0* - Q3*	Inverting Outputs

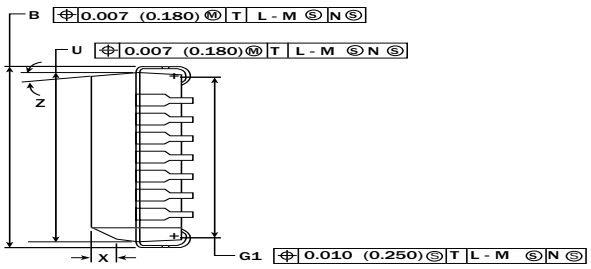
Pinout

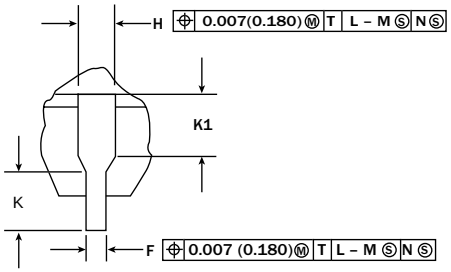


Package Information









View S

NOTES:

1. Datums -L-, -M-, and -N- determined where top of lead shoulder exits plastic body at mold parting line.
2. DIM G1, true position to be measured at Datum -T-, Seating Plane.
3. DIM R and U do not include mold flash. Allowable mold flash is 0.010 (0.250) per side.
4. Dimensioning and tolerances per ANSI Y14.5M, 1982.
5. Controlling Dimension: Inch.
6. The package top may be smaller than the package bottom by up to 0.012 (0.300). Dimensions R and U are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
7. Dimension H does not include Dambar protrusion or intrusion. The Dambar protrusion(s) shall not cause the H dimension to be greater than 0.037 (0.940). The Dambar intrusion(s) shall not cause the H dimension to be smaller than 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	–	0.51	–
K	0.025	–	0.64	–
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	–	0.020	–	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	–	1.02	–

DC Characteristics

SK10/100E131 DC Electrical Characteristics *(Notes 1, 2, 3, 4)*

(V_{CC} – V_{EE} = 4.2V to 5.5V; VOUT Loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IH}	Input HIGH Current													
	CC			350			350			350			350	µA
	S			450			450			450			450	µA
	R, CE			300			300			300			300	µA
	D			150			150			150			150	µA
I_{EE}	Power Supply Current													
	10E	31		52	33		54	33		55	35		57	mA
	100E	34		56	36		60	38		62	42		68	mA

AC Characteristics

SK10/100E131 AC Electrical Characteristics

(V_{CC} – V_{EE} = 4.2V to 5.5V; VOUT Loaded 50Ω to V_{CC} – 2.0V)

Symbol	Characteristic	TA = –40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Max. Toggle Frequency	1000	1400		1100	1400		1100	1400		1100	1400		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output													
	CE	430	495	560	430	500	570	430	510	590	430	500	570	ps
	CC	415	490	565	435	500	565	425	495	565	430	495	560	ps
	R	465	530	595	480	540	600	480	540	600	520	580	640	ps
	S	420	495	570	440	510	580	445	515	585	480	545	610	ps
t_S	Setup Time													
	D	200	20		150	20		150	20		150	20		ps
t_H	Hold Time													
	D	225	-20		175	-20		175	-20		175	-20		ps
t_{RR}	Reset Recovery Time	450	150		400	150		400	150		400	150		ps
t_{PW}	Minimum Pulse Width													
	CLK	400			400			400			400			ps
	R, S	400			400			400			400			ps
t_{SKEW}	Within Device Skew[3]		60			60			60			60		ps
t_r / t_f	Rise/Fall Times (20%-80%)													
	10E	217		325	222		340	225		345	230		365	ps
	100E	380	505	530	345	425	505	335	430	525	255	325	395	ps

AC Information *(continued)*

Notes:

1. 10E circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
2. The same DC parameter values apply across the full VEE range of –4.2 to –5.5V. 100E circuits are designed to meet the DC specifications shown in the table where transverse airflow greater than 500 lfpm is maintained.
3. Within device skew is defined as identical transitions on similar paths through a device.
4. For standard ECL DC Specifications, refer to the ECL Logic Family Standard DC Data Sheet.
5. For part ordering description, see HPP Part Ordering Information Data Sheet.

Ordering Information

Ordering Code	Package ID
SK10E131PJ	28-PLCC
SK10E131PJT	28-PLCC
SK100E131PJ	28-PLCC
SK100E131PJT	28-PLCC

Application Notes

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices
AN1005 - Using ECL / LVECL Devices as PECL / LVPECL
AN1006 - Designing with 10K and 100K ECL / PECL Devices

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