



**32K x 8 3.0V Static RAM**

**Features**

- Single 3.0V power supply
- Ideal for low-voltage cache memory applications
- High speed
  - 12/15 ns
- Low active power
  - 198 mW (max.)
- Low CMOS standby power (L)
  - 165  $\mu$ W (max.),  $f=f_{MAX}$
- 2.0V data retention (L)
  - 40  $\mu$ W (max.)
- Low-power alpha immune 6T cell
- Plastic SOJ and TSOP packaging

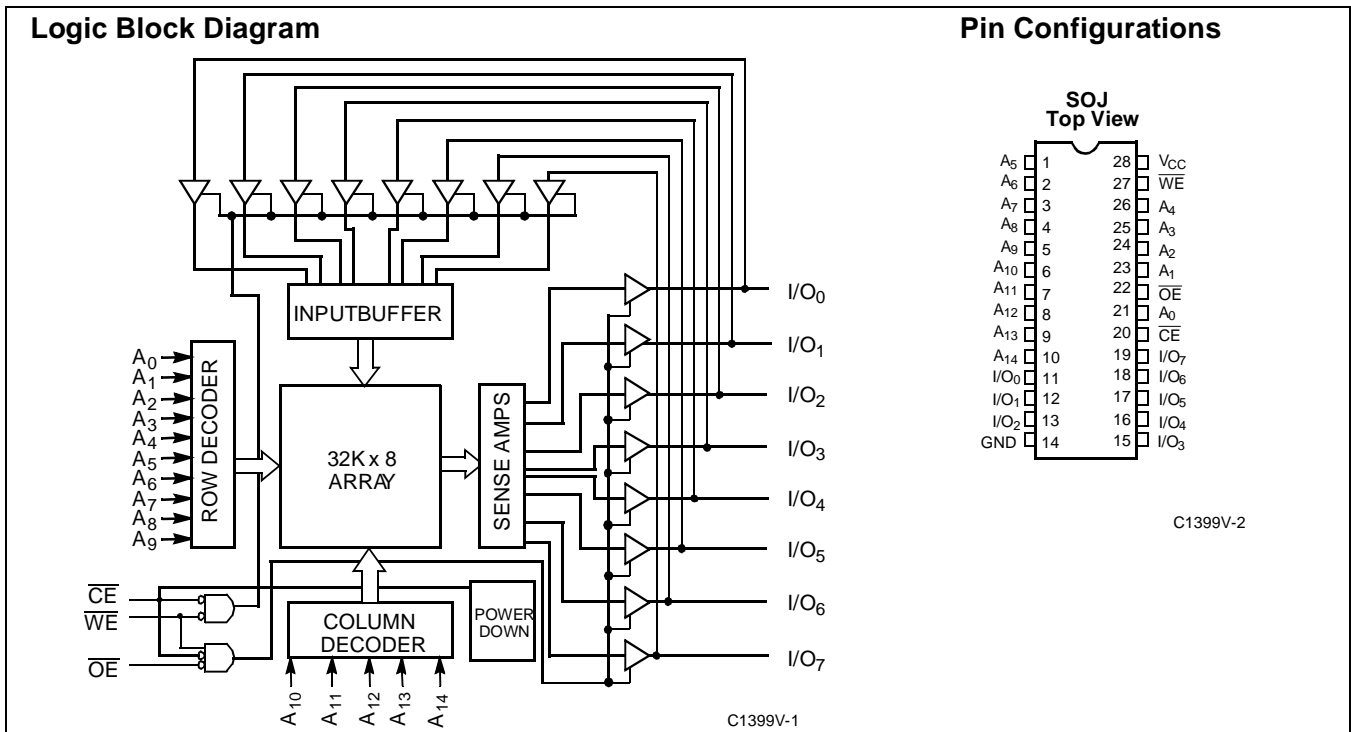
pansion is provided by an active LOW chip enable ( $\overline{CE}$ ) and active LOW output enable ( $\overline{OE}$ ) and three-state drivers. The device has an automatic power-down feature, reducing the power consumption by more than 95% when deselected.

An active LOW write enable signal ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When  $\overline{CE}$  and  $\overline{WE}$  inputs are both LOW, data on the eight data input/output pins ( $I/O_0$  through  $I/O_7$ ) is written into the memory location addressed by the address present on the address pins ( $A_0$  through  $A_{14}$ ). Reading the device is accomplished by selecting the device and enabling the outputs,  $\overline{CE}$  and  $\overline{OE}$  active LOW, while  $\overline{WE}$  remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ( $\overline{WE}$ ) is HIGH. The CY7C1399V is available in standard 300-mil-wide SOJ and 28-pin TSOP type I packages.

**Functional Description**

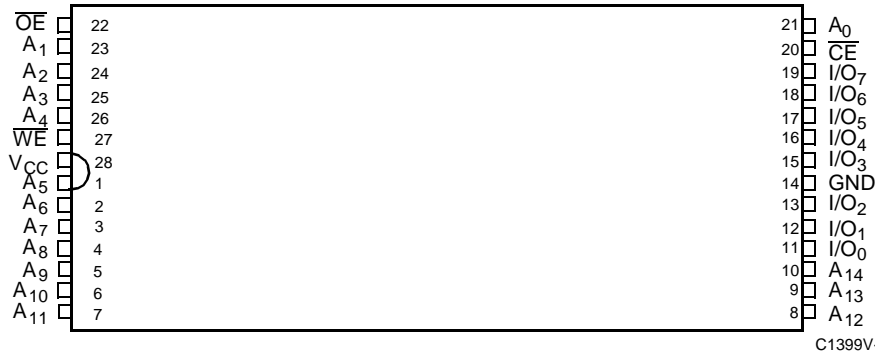
The CY7C1399V is a high-performance 3.0V CMOS static RAM organized as 32,768 words by 8 bits. Easy memory ex-



**Selection Guide**

	7C1399V-12	7C1399V-15	7C1399V-20	7C1399V-25	7C1399V-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	60	55	50	45	40
Maximum CMOS Standby Current ( $\mu$ A)	500	500	500	500	500
Maximum CMOS Standby Current ( $\mu$ A)   L	50	50	50	50	50

Shaded area contains advanced information.

**Pin Configurations (continued)**
**TSOP  
Top View**

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -65°C to +150°C
- Ambient Temperature with Power Applied ..... -55°C to +125°C
- Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[1]</sup> ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V
- DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

- Output Current into Outputs (LOW) ..... 20 mA
- Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.0V ±300 mV
Industrial	-40°C to +85°C	3.0V ±300 mV

**Electrical Characteristics Over the Operating Range<sup>[2]</sup>**

Parameter	Description	Test Conditions	7C1399V-12		7C1399V-15		7C1399V-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current		-1	+1	-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		60		55		50	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> , or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		5		5		5	mA
			L	3		3		3	
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs <sup>[4]</sup>	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> -0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.3V, or V <sub>IN</sub> ≤ 0.3V, WE ≥ V <sub>CC</sub> -0.3V or WE ≤ 0.3V, f = f <sub>MAX</sub>		500		500		500	μA
			L	50		50		50	

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**Notes:**

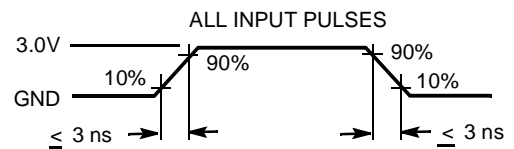
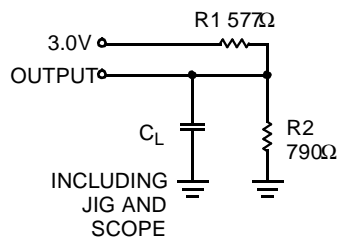
1. Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.

**Electrical Characteristics** Over the Operating Range<sup>[2]</sup> (continued)

Parameter	Description	Test Conditions	7C1399V-25		7C1399V-35		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3V	2.0	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Load Current		-1	+1	-1	+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		45		40	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> , or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		5		5	mA
			L	3		3	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs <sup>[4]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC}-0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, WE ≥ V <sub>CC</sub> -0.3V or WE ≤ 0.3V, f = f <sub>MAX</sub>		500		500	μA
			L	50		50	μA

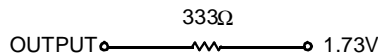
**Capacitance<sup>[5]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.0V	5	pF
C <sub>IN</sub> : Controls			6	pF
C <sub>OUT</sub>	Output Capacitance		6	pF

**AC Test Loads and Waveforms**


C1399V-4

Equivalent to: THÉVENIN EQUIVALENT


**Notes:**

- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Device draws low standby current regardless of switching on the addresses.
- Tested initially and after any design or process changes that may affect these parameters.

**Switching Characteristics** Over the Operating Range<sup>[2, 6]</sup>

Parameter	Description	7C1399V-12		7C1399V-15		7C1399V-20		7C1399V-25		7C1399V-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		ns
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		3		3		3		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		5		6		7		8		10	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[7]</sup>	0		0		0		0		0		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>		5		6		6		7		7	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		3		3		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z <sup>[7, 8]</sup>		6		7		7		8		8	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35	ns
<b>WRITE CYCLE</b> <sup>[9, 10]</sup>												
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		35		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	8		10		12		15		20		ns
t <sub>AW</sub>	Address Set-Up to Write End	8		10		12		15		20		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	8		10		12		15		20		ns
t <sub>SD</sub>	Data Set-Up to Write End	6		9		10		11		12		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[8]</sup>		7		7		7		7		7	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		3		3		ns

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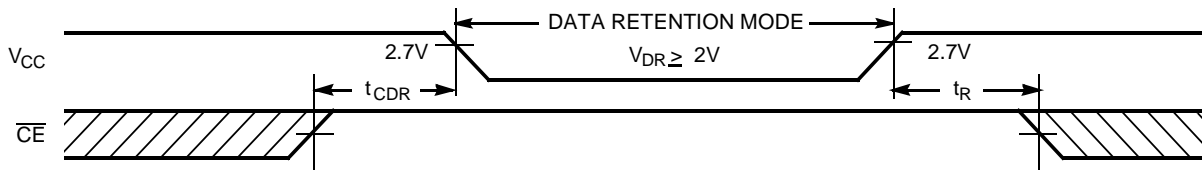
**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0		V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = V <sub>DR</sub> = 2.0V, CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		200	μA
	Data Retention Current		L	20	μA
t <sub>CDR</sub> <sup>[5]</sup>	Chip Deselect to Data Retention Time			0	ns
t <sub>R</sub> <sup>[5]</sup>	Operation Recovery Time		t <sub>RC</sub>		ns

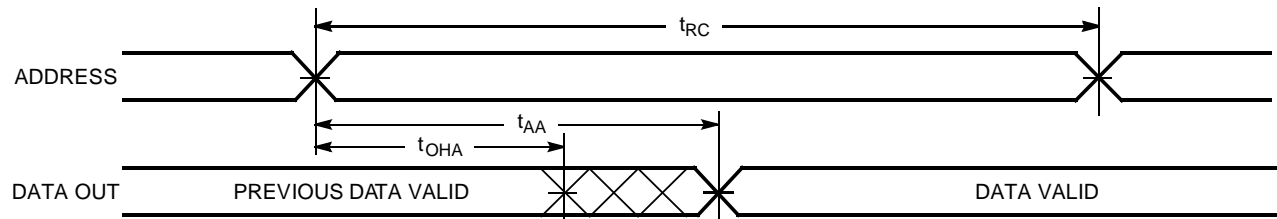
**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and capacitance C<sub>L</sub> = 30 pF.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

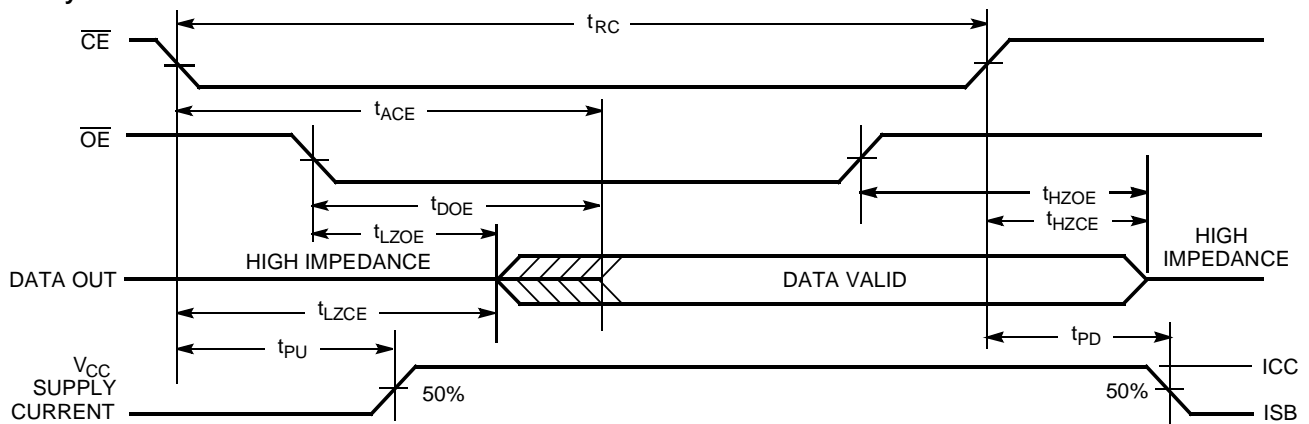


**Data Retention Waveform**


C1399V-5

**Switching Waveforms**
**Read Cycle No. 1** <sup>[11,12]</sup>


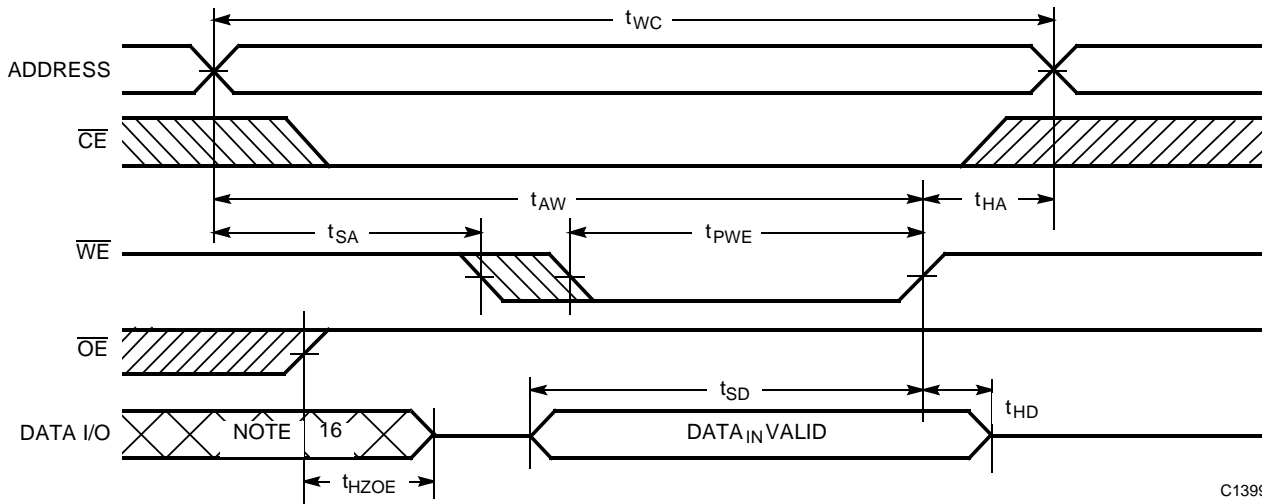
C1399V-6

**Read Cycle No. 2** <sup>[12,13]</sup>


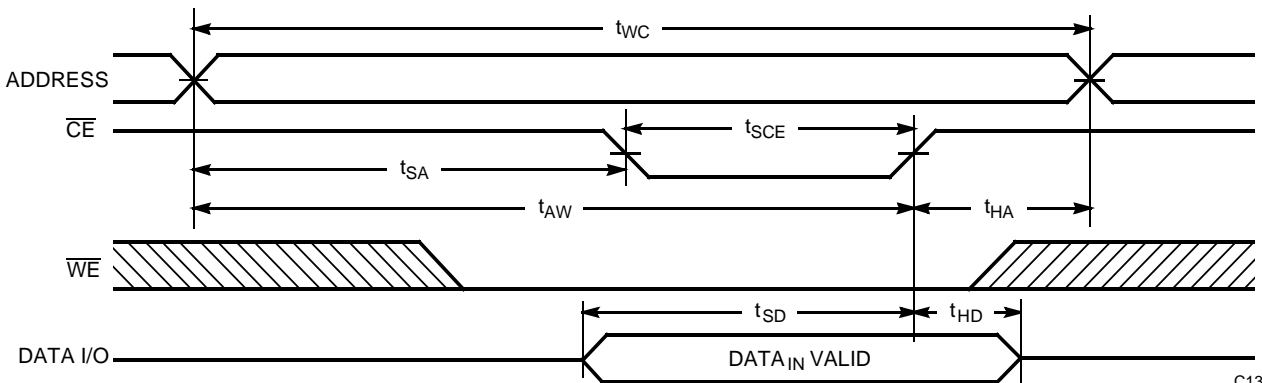
C1399V-7

**Notes:**

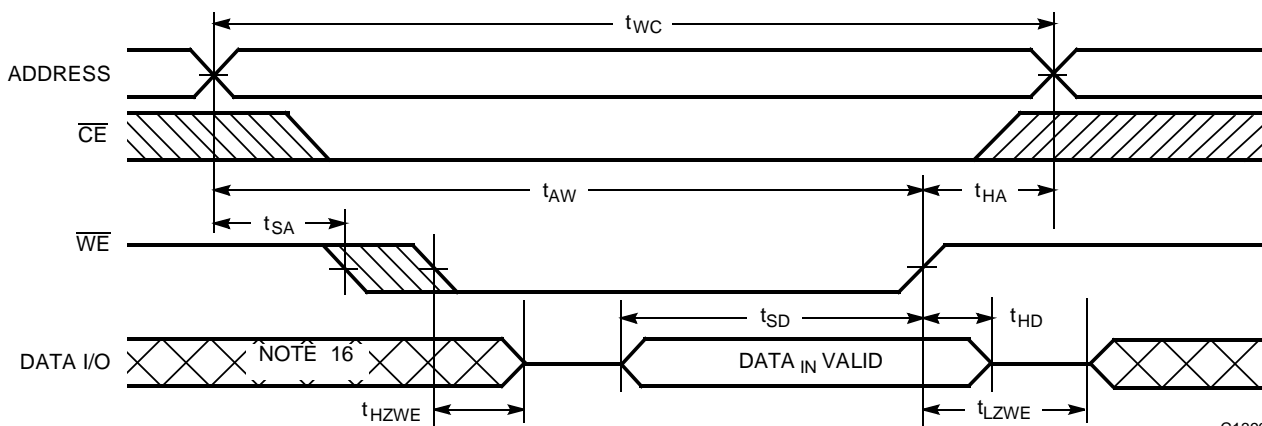
11. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
12.  $\overline{WE}$  is HIGH for read cycle.
13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{WE}$  Controlled)** <sup>[9,14,15]</sup>


C1399V-8

**Write Cycle No. 2 ( $\overline{CE}$  Controlled)** <sup>[9,14,15]</sup>


C1399V-9

**Write Cycle No.3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** <sup>[10,15]</sup>


C1399V-10

**Notes:**

14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in the output state and input signals should not be applied.

**Truth Table**

CE	WE	OE	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1399V-12VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399VL-12VC	V21	28-Lead Molded SOJ	
	CY7C1399V-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399VL-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C1399V-15VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399VL-15VC	V21	28-Lead Molded SOJ	
	CY7C1399V-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399VL-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399V-15ZI	Z28	28-Lead Thin Small Outline Package	Industrial
	CY7C1399VL-15ZI	Z28	28-Lead Thin Small Outline Package	
20	CY7C1399V-20VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399VL-20VC	V21	28-Lead Molded SOJ	
	CY7C1399V-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399VL-20ZC	Z28	28-Lead Thin Small Outline Package	
25	CY7C1399V-25VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399VL-25VC	V21	28-Lead Molded SOJ	
	CY7C1399V-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399VL-25ZC	Z28	28-Lead Thin Small Outline Package	
35	CY7C1399V-35VC	V21	28-Lead Molded SOJ	Commercial
	CY7C1399VL-35VC	V21	28-Lead Molded SOJ	
	CY7C1399V-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C1399VL-35ZC	Z28	28-Lead Thin Small Outline Package	

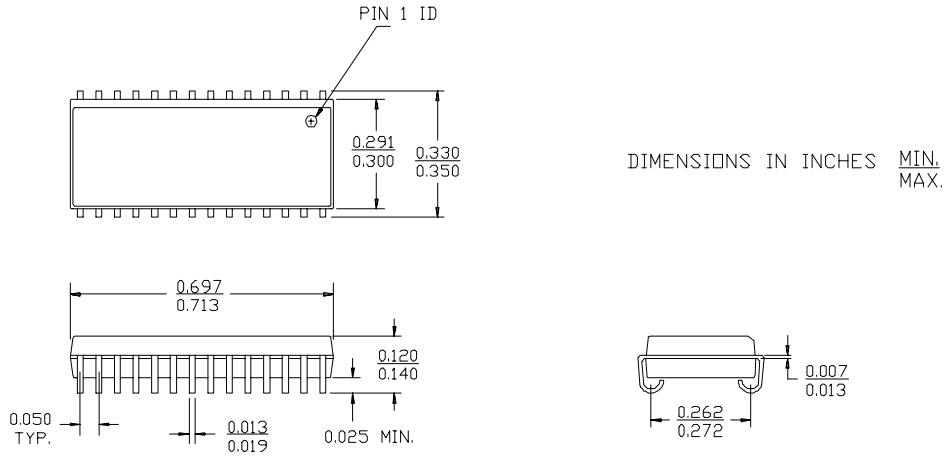
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**Package Diagrams**

**28-Lead Molded SOJ V21**



**28-Lead Thin Small Outline Package Z28**

