

LM5113

LM5113 5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs



Literature Number: SNVS725D

LM5113

5A, 100V Half-Bridge Gate Driver for Enhancement Mode GaN FETs

General Description

The LM5113 is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride (GaN) FETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of driving a high-side enhancement mode GaN FET operating up to 100V. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.2V, which prevents the gate voltage from exceeding the maximum gate-source voltage rating of enhancement mode GaN FETs. The inputs of the LM5113 are TTL logic compatible, and can withstand input voltages up to 14V regardless of the VDD voltage. The LM5113 has split gate outputs, providing flexibility to adjust the turn-on and turn-off strength independently.

In addition, the strong sink capability of the LM5113 maintains the gate in the low state, preventing unintended turn-on during switching. The LM5113 can operate up to several MHz. The LM5113 is available in a standard LLP-10 pin package, which contains an exposed pad to aid power dissipation.

Features

- Independent high-side and low-side TTL logic inputs
- 1.2A/5A peak source/sink current
- High-side floating bias voltage rail operates up to 100VDC
- Internal bootstrap supply voltage clamping
- Split outputs for adjustable turn-on/turn-off strength
- 0.6Ω / 2.1Ω pull-down/pull-up resistance
- Fast propagation times (28ns typical)
- Excellent propagation delay matching (1.5ns typical)
- Supply rail under-voltage lockout
- Low power consumption

Typical Applications

- Current Fed Push-Pull converters
- Half and Full-Bridge converters
- Synchronous Buck converters
- Two-switch Forward converters
- Forward with Active Clamp converters

Package

- LLP-10 (4 mm x 4 mm)

Typical Application

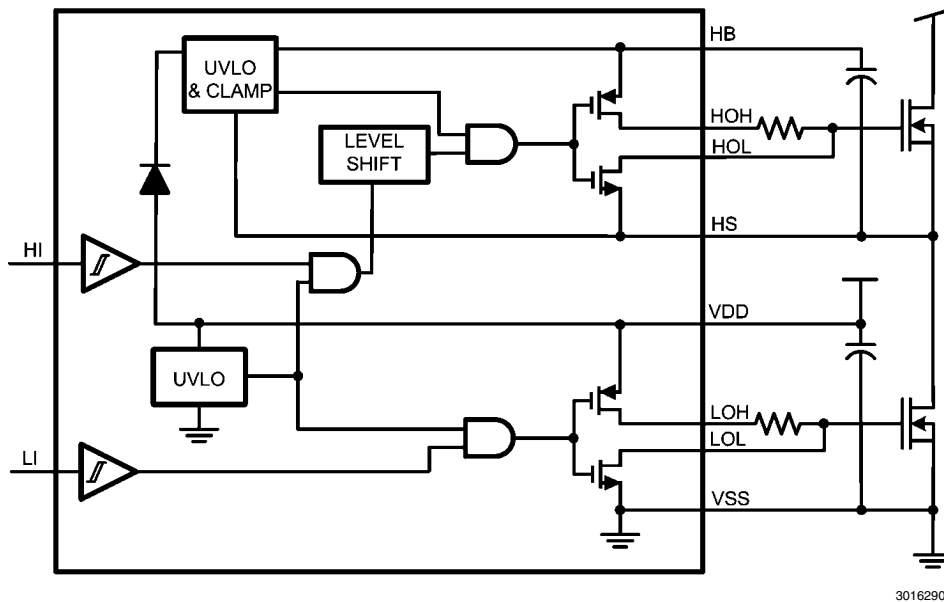
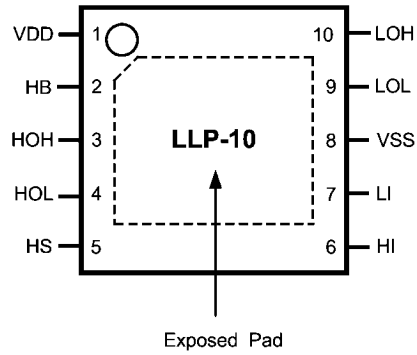


FIGURE 1.

Truth Table

HI	LI	HOH	HOL	LOH	LOL
L	L	Open	L	Open	L
L	H	Open	L	H	Open
H	L	H	Open	Open	L
H	H	H	Open	H	Open

Connection Diagram



30162901

Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5113SD	LLP-10	SDC10A	1000 units shipped in Tape & Reel
LM5113SDE	LLP-10	SDC10A	250 units shipped in Tape & Reel
LM5113SDX	LLP-10	SDC10A	4500 units shipped in Tape & Reel

Pin Descriptions

Pin Number	Name	Description	Applications Information
LLP-10			
1	VDD	5V Positive gate drive supply	Locally decouple to VSS using low ESR/ESL capacitor located as close to the IC as possible.
2	HB	High-side gate driver bootstrap rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to the IC as possible.
3	HOH	High-side gate driver source-current output	Connect to the gate of high-side GaN FET with a short, low inductance path.
4	HOL	High-side gate driver sink-current output	Connect to the gate of high-side GaN FET with a short, low inductance path.
5	HS	High-side GaN FET source connection	Connect to the bootstrap capacitor negative terminal and the source of the high-side GaN FET.
6	HI	High-side driver control input	The LM5113 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7	LI	Low-side driver control input	The LM5113 inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
8	VSS	Ground return	All signals are referenced to this ground.
9	LOL	Low-side gate driver sink-current output	Connect to the gate of the low-side GaN FET with a short, low inductance path.
10	LOH	Low-side gate driver source-current output	Connect to the gate of high-side GaN FET with a short, low inductance path.
EP		Exposed Pad	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PC board to aid thermal dissipation.

Absolute Maximum Ratings (Note 1)

VDD to VSS	-0.3V to 7V
HB to HS	-0.3V to 7V
LI or HI Input	-0.3V to 15V
LOH, LOL Output	-0.3V to VDD +0.3V
HOH, HOL Output	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
HS to VSS	-5V to +100V
HB to VSS	0 to 107V
HB to VDD	0 to 100V
Junction Temperature	+150°C

Storage Temperature Range

-55°C to +150°C

ESD Rating HBM

2 kV

Recommended Operating Conditions

VDD	+4.5V to +5.5V
LI or HI Input	0V to +14V
HS	-5V to 100V
HB	$V_{HS} + 4V$ to $V_{HS} + 5.5V$
HS Slew Rate	<50 V/ns
Junction Temperature	-40°C to +125°C

Electrical Characteristics

Limits in standard type are for $T_J = 25^\circ\text{C}$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = V_{HB} = 5V$, $V_{SS} = V_{HS} = 0V$, No Load on LOL and HOL or HOH and HOL (Note 2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current	LI = HI = 0V		0.07	0.1	mA
I_{DDO}	VDD Operating Current	f = 500 kHz		2.0	3.0	mA
I_{HB}	Total HB Quiescent Current	LI = HI = 0V		0.08	0.1	mA
I_{HBO}	Total HB Operating Current	f = 500 kHz		1.5	2.5	mA
I_{HBS}	HB to VSS Current, Quiescent	HS = HB = 100V		0.1	8	μA
I_{HBSO}	HB to VSS Current, Operating	f = 500 kHz		0.4	1.0	mA
INPUT PINS						
V_{IR}	Input Voltage Threshold	Rising Edge	1.89	2.06	2.18	V
V_{IF}	Input Voltage Threshold	Falling Edge	1.48	1.66	1.76	V
V_{IHYS}	Input Voltage Hysteresis			400		mV
R_I	Input Pulldown Resistance		100	200	300	k Ω
UNDER VOLTAGE PROTECTION						
V_{DDR}	VDD Rising Threshold		3.2	3.8	4.5	V
V_{DDH}	VDD Threshold Hysteresis			0.2		V
V_{HBR}	HB Rising Threshold		2.5	3.2	3.9	V
V_{HBH}	HB Threshold Hysteresis			0.2		V
BOOTSTRAP DIODE						
V_{DL}	Low-Current Forward Voltage	$I_{VDD-HB} = 100 \mu\text{A}$		0.45	0.65	V
V_{DH}	High-Current Forward Voltage	$I_{VDD-HB} = 100 \text{mA}$		0.90	1.00	V
R_D	Dynamic Resistance	$I_{VDD-HB} = 100 \text{mA}$		1.85	3.60	Ω
	HB-HS Clamp	Regulation Voltage	4.7	5.2	5.45	V
LOW & HIGH SIDE GATE DRIVER						
V_{OL}	Low-Level Output Voltage	$I_{HOL} = I_{LOL} = 100 \text{mA}$		0.06	0.10	V
V_{OH}	High-Level Output Voltage $V_{OH} = V_{DD} - LOH$ or $V_{OH} = HB - HOH$	$I_{HOH} = I_{LOH} = 100 \text{mA}$		0.21	0.31	V
I_{OHL}	Peak Source Current	HOH, LOH = 0V		1.2		A
I_{OLL}	Peak Sink Current	HOL, LOL = 5V		5		A
I_{OHLK}	High-Level Output Leakage Current	HOH, LOH = 0V			1.5	μA
I_{OLLK}	Low-Level Output Leakage Current	HOL, LOL = 5V			1.5	μA
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	LLP-10 (Note 3)		40		$^\circ\text{C/W}$

Switching Characteristics

Limits in standard type are for $T_J = 25^\circ\text{C}$ only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to $+125^\circ\text{C}$. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise specified, $V_{DD} = V_{HB} = 5\text{V}$, $V_{SS} = V_{HS} = 0\text{V}$, No Load on LOL and LOH or HOL and HOH (*Note 2*).

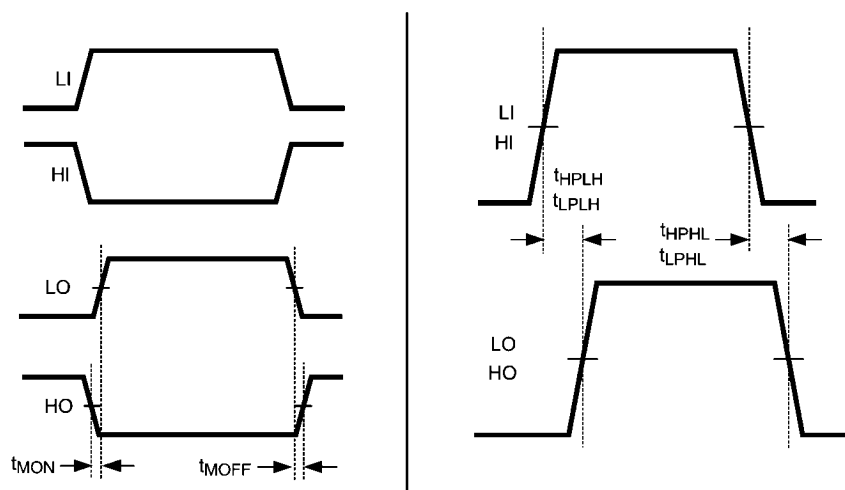
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LPHL}	LO Turn-Off Propagation Delay	LI Falling to LOL Falling		26.5	45.0	ns
t_{LPLH}	LO Turn-On Propagation Delay	LI Rising to LOH Rising		28.0	45.0	ns
t_{HPHL}	HO Turn-Off Propagation Delay	HI Falling to HOL Falling		26.5	45.0	ns
t_{HPLH}	HO Turn-On Propagation Delay	HI Rising to HOH Rising		28.0	45.0	ns
t_{MON}	Delay Matching: LO on & HO off			1.5	8.0	ns
t_{MOFF}	Delay Matching: LO off & HO on			1.5	8.0	ns
t_{HRC}	HO Rise Time (0.5V - 4.5V)	$C_L = 1000\text{ pF}$		7.0		ns
t_{LRC}	LO Rise Time (0.5V - 4.5V)	$C_L = 1000\text{ pF}$		7.0		ns
t_{HFC}	HO Fall Time (0.5V - 4.5V)	$C_L = 1000\text{ pF}$		1.5		ns
t_{LFC}	LO Fall Time (0.5V - 4.5V)	$C_L = 1000\text{ pF}$		1.5		ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			10		ns
t_{BS}	Bootstrap Diode Reverse Recovery Time	$I_F = 100\text{mA}$, $I_R = 100\text{mA}$		40		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: Min and Max limits are 100% production tested at 25°C . Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 3: Four layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

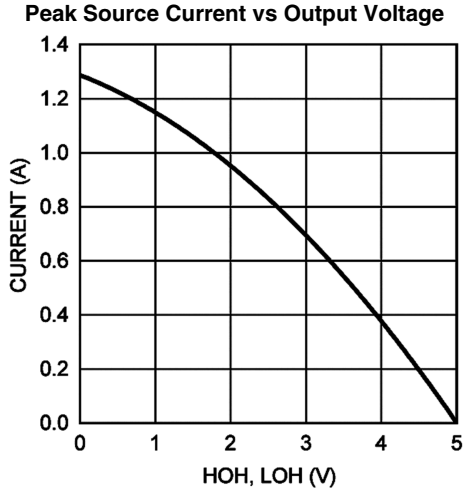
Timing Diagram



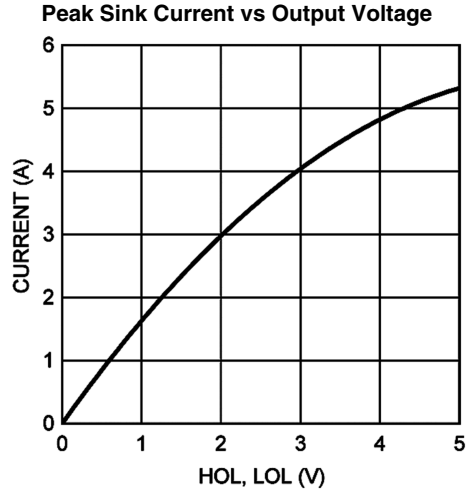
30162904

FIGURE 2. Timing Diagram

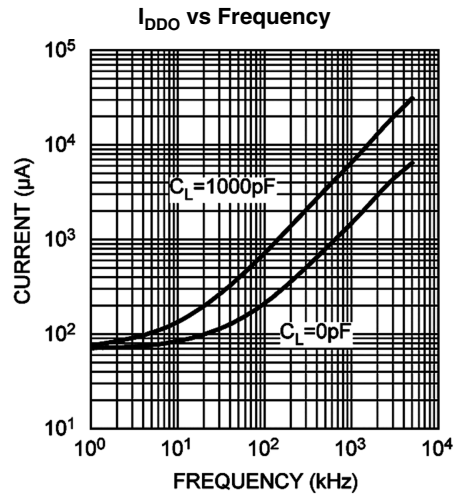
Typical Performance Characteristics (Note 4)



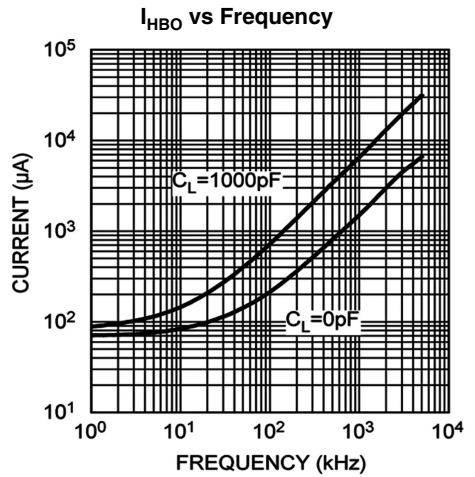
30162905



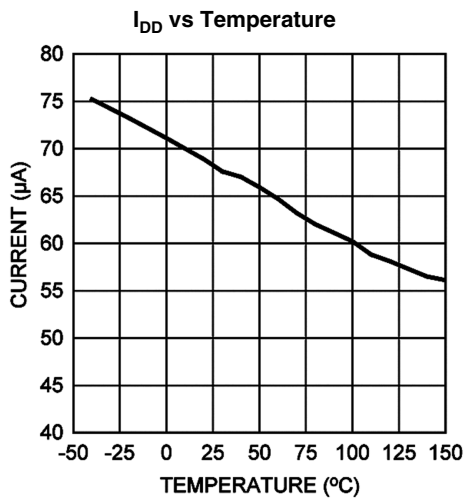
30162906



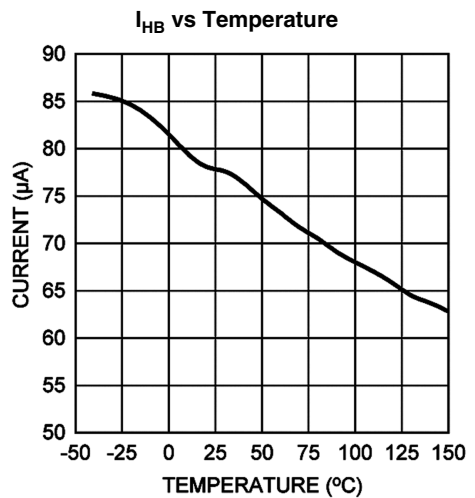
30162907



30162908

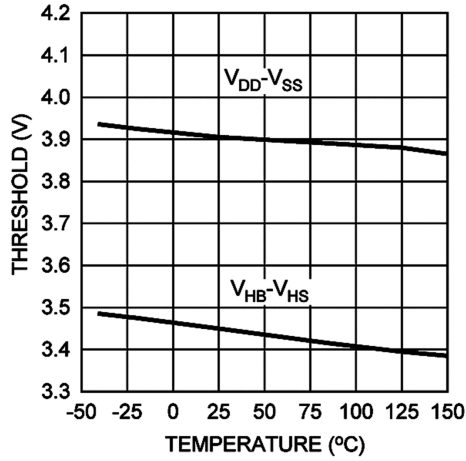


30162909



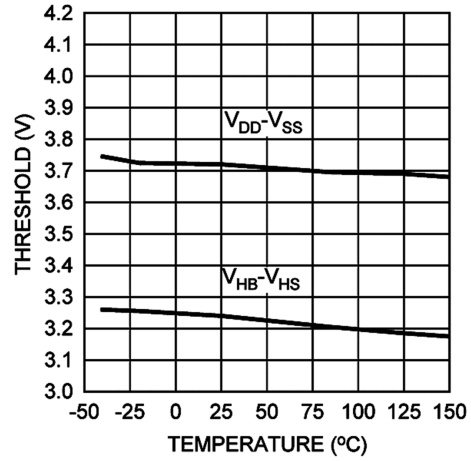
30162910

UVLO Rising Thresholds vs Temperature



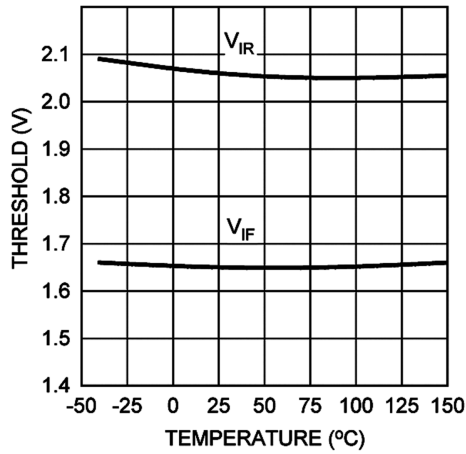
30162911

UVLO Falling Thresholds vs Temperature



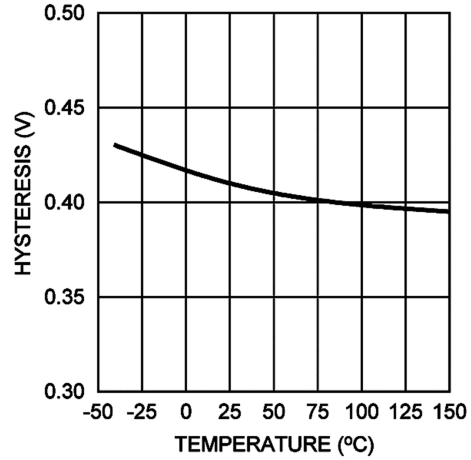
30162912

Input Thresholds vs Temperature



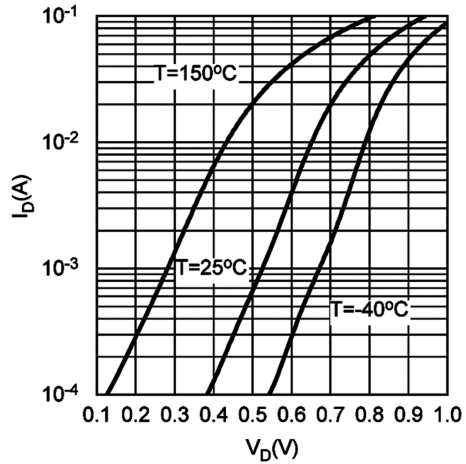
30162913

Input Threshold Hysteresis vs Temperature



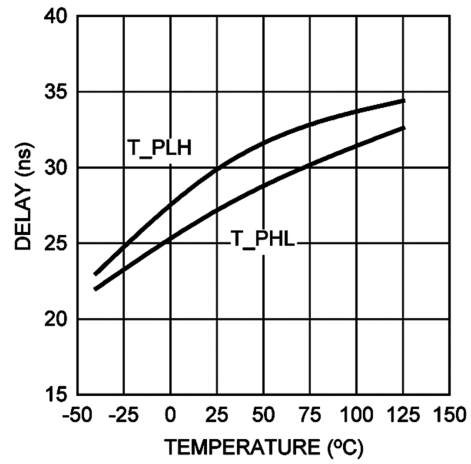
30162914

Bootstrap Diode Forward Voltage



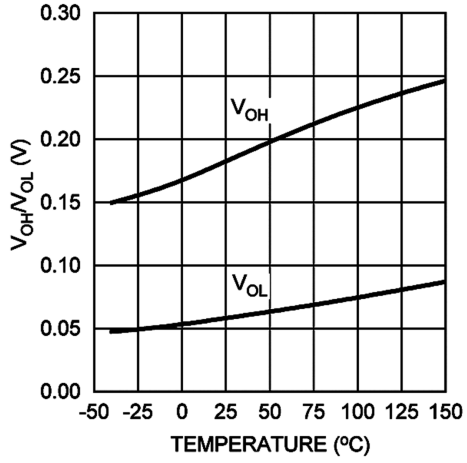
30162915

Propagation Delay vs Temperature



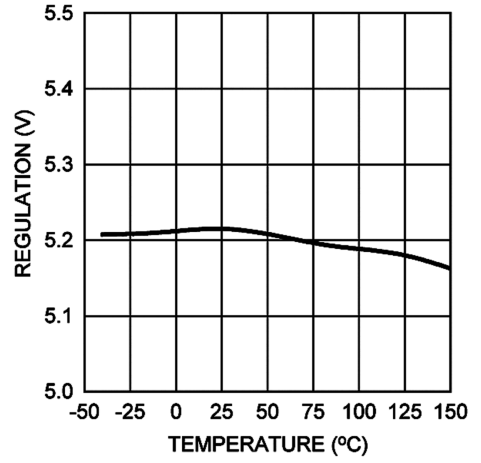
30162916

LO&HO Gate Drive — High/Low Level Output Voltage vs Temperature



30162917

HB Regulation Voltage vs Temperature



30162918

Note 4: Unless otherwise specified, VDD = VHB = 5V, VSS = VHS = 0V.

Detailed Operating Description

The LM5113 is designed to drive both the high-side and the low-side enhancement mode Gallium Nitride FETs in a synchronous buck or a half-bridge configuration. The outputs of the LM5113 are independently controlled with TTL input thresholds. The inputs of the LM5113 can withstand voltages up to 14V regardless of the VDD voltage, and can be directly connected to the outputs of PWM controllers.

The high side driver uses the floating bootstrap capacitor voltage to drive the high-side FET. As shown in *Figure 1*, the bootstrap capacitor is recharged through an internal bootstrap diode each cycle when the HS pin is pulled below the VDD voltage. For inductive load applications the HS node will fall to a negative potential, clamped by the low side FET.

Due to the intrinsic feature of enhancement mode GaN FETs the source-to-drain voltage, when the gate is pulled low, is usually higher than a diode forward voltage drop. This can lead to an excessive bootstrap voltage that can damage the high-side GaN FET. The LM5113 solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5V.

The output pull-down and pull-up resistance of LM5113 is optimized for enhancement mode GaN FETs to achieve high frequency, efficient operation. The 0.6Ω pull-down resistance provides a robust low impedance turn-off path necessary to eliminate undesired turn-on induced by high dv/dt or high di/dt. The 2.1Ω pull-up resistance helps reduce the ringing and over-shoot of the switch node voltage. The split outputs of the LM5113 offer flexibility to adjust the turn-on and turn-off speed by independently adding additional impedance in either the turn-on path and/or the turn-off path.

The LM5113 has an Under-voltage Lockout (UVLO) on both the VDD and bootstrap supplies. When the VDD voltage is below the threshold voltage of 3.8V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also if there is sufficient VDD voltage, the UVLO will actively pull the LOL and HOL low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.2V, only HOL is pulled low. Both UVLO threshold voltages have 200mV of hysteresis to avoid chattering.

Bypass Capacitor

The VDD bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated as follows:

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} + Q_{rr}}{\Delta V}$$

Q_{gH} and Q_{gL} are gate charge of the high-side and low-side transistors respectively. Q_{rr} is the reverse recovery charge of

the bootstrap diode, which is typically around 4nC. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 0.1μF or larger value, good quality, ceramic capacitor is recommended. The bypass capacitor should be placed as close to the pins of the IC as possible to minimize the parasitic inductance.

Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, dc bias power for HB under-voltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated as follows:

$$C_{BST} > \frac{Q_{gH} + I_{HB} \times t_{ON} + Q_{rr}}{\Delta V}$$

I_{HB} is the quiescent current of the high-side driver. t_{on} is the maximum on-time period of the high-side transistor. A good quality, ceramic capacitor should be used for the bootstrap capacitor. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

Power Dissipation

The power consumption of the driver is an important measure that determines the maximum achievable operating frequency of the driver. It should be kept below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation of the LM5113 is the sum of the gate driver losses and the bootstrap diode power loss.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated as

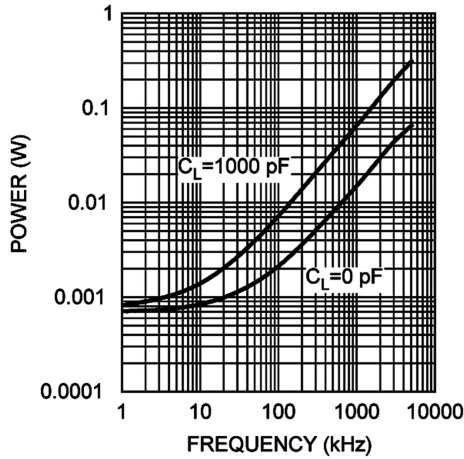
$$P = (C_{LoadH} + C_{LoadL}) \times V_{DD}^2 \times f_{sw}$$

C_{LoadH} and C_{LoadL} are the high-side and the low-side capacitive loads respectively. It can also be calculated with the total input gate charge of the high-side and the low-side transistors as

$$P = (Q_{gH} + Q_{gL}) \times V_{DD} \times f_{sw}$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equations. This plot can be used to approximate the power losses due to the gate drivers.

Gate Driver Power Dissipation (LO+HO)
VDD=+5V, Neglecting Bootstrap Diode Losses

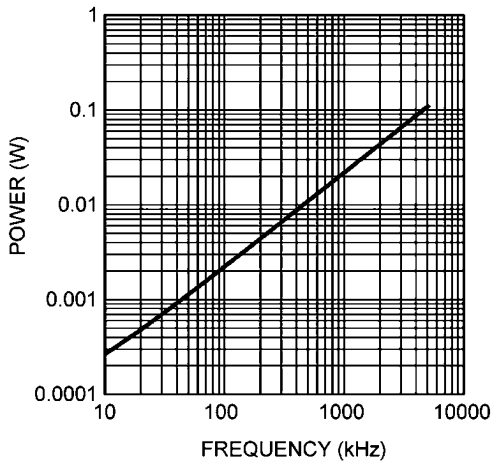


30162919

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

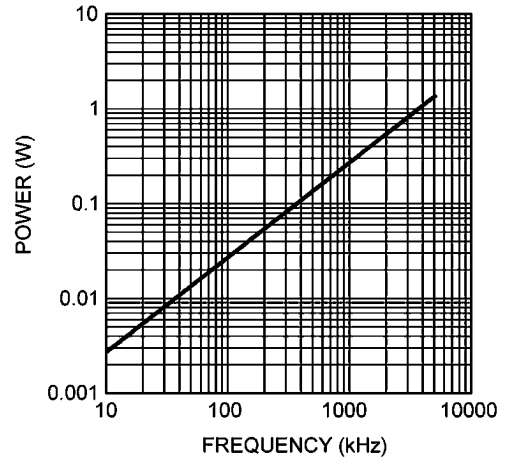
The following two plots illustrate the forward bias power loss and the reverse bias power loss of the bootstrap diode respectively. The plots are generated based on calculations and lab measurements of the diode reverse time and current under several operating conditions. The plots can be used to predict the bootstrap diode power loss under different operating conditions.

Forward Bias Power Loss of Bootstrap Diode
 $V_{IN}=50V$
The Load of High-Side Driver is a GaN FET
with Total Gate Charge of 10nC



30162943

Reverse Recovery Power Loss of Bootstrap Diode
 $V_{IN}=50V$
The Load of High-Side Driver is a GaN FET
with Total Gate Charge of 10nC



30162944

The sum of the driver loss and the bootstrap diode loss is the total power loss of the IC. For a given ambient temperature, the maximum allowable power loss of the IC can be defined as

$$P = \frac{(T_J - T_A)}{\theta_{JA}}$$

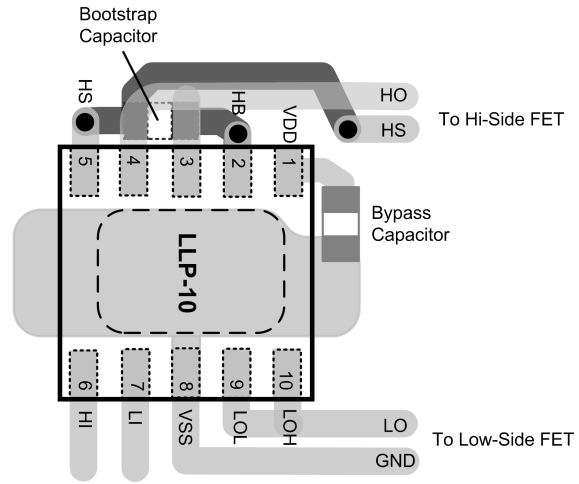
Layout Considerations

Small gate capacitance and miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt , coupled with a low gate threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some hints.

1. The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs should be placed close to the driver.
2. The second high current path includes the bootstrap capacitor, the local ground referenced VDD bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
3. The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. It is recommended to connect HS pin and VSS pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.
4. The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.
5. Low ESR/ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak current being drawn from VDD during turn-on of the FETs. It is most desirable to place the VDD decoupling capacitor and the HB to HS bootstrap capacitor on the same side of the PC board as the driver. The inductance of vias can impose excessive ringing on the IC pins.
6. To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low ESR ceramic capacitors adjacent to the GaN FETs.

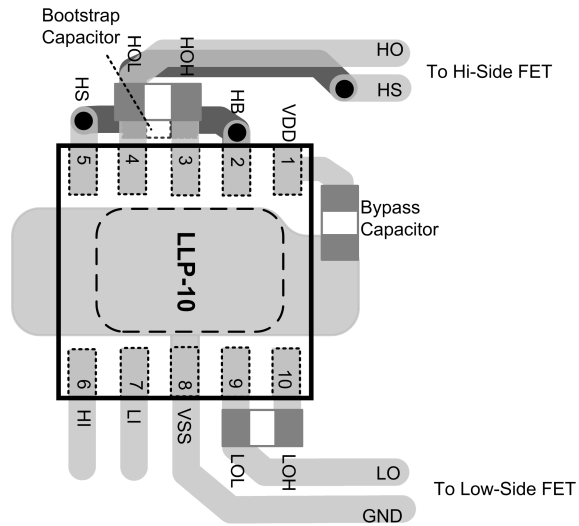
The following figures show recommended layout patterns. Two cases are considered: (1) Without any gate resistors; (2)

With an optional turn-on gate resistor. It should be noted that 0402 SMD package is assumed for the passive components in the drawings.



Without Gate Resistors

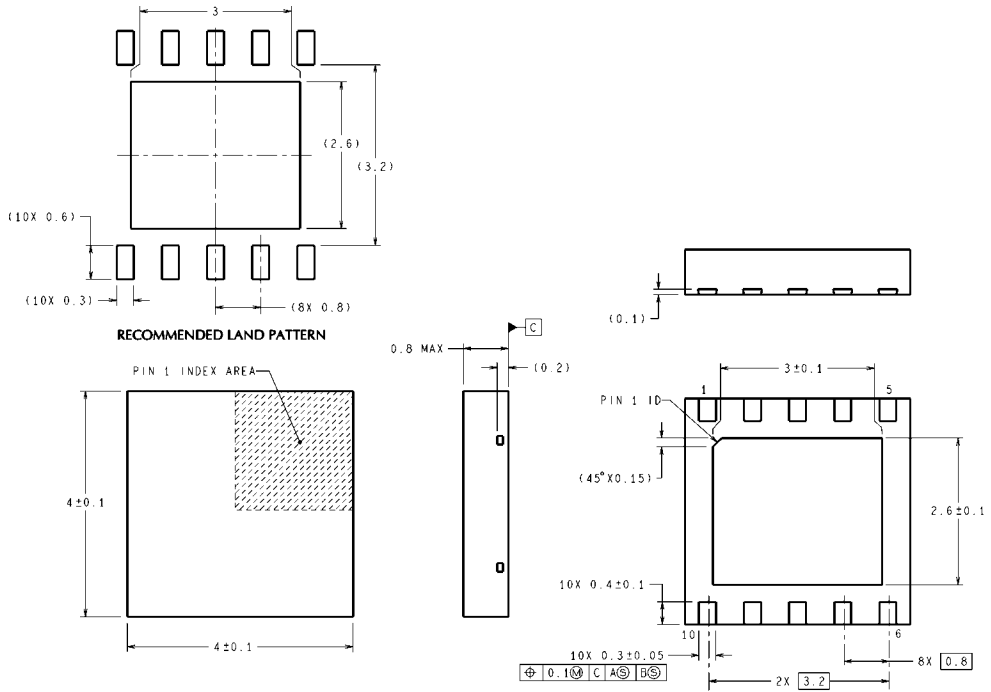
30162921



With HOH and LOH Gate Resistors

30162922

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

**LLP-10 Outline Drawing
NS Package Number SDC10A**

SDC10A (Rev A)

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2011 National Semiconductor Corporation

For the most current product information visit us at www.national.com



National Semiconductor
Americas Technical
Support Center
 Email: support@nsc.com
 Tel: 1-800-272-9959

National Semiconductor Europe
Technical Support Center
 Email: europe.support@nsc.com

National Semiconductor Asia
Pacific Technical Support Center
 Email: ap.support@nsc.com

National Semiconductor Japan
Technical Support Center
 Email: jpn.feedback@nsc.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated