

54F/74F132

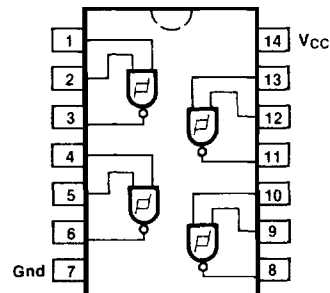
Quad 2-Input NAND Schmitt Trigger

Description

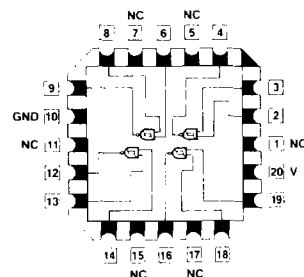
The 'F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code: See Section 5

Connection Diagrams

**Pin Assignment
for DIP and SOIC**



**Pin Assignment
for LCC and PCC**

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Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A, B	Inputs	0.5/0.375
O	Outputs	25/12.5

Function Table

Inputs		Outputs
A	B	O
L	L	H
L	H	H
H	L	H
H	H	L

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		8.5	12.0	mA	Outputs HIGH	$V_{CC} = \text{Max}$
I_{CCL}			13.0	19.5		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		7.0					ns	3-1 3-3	