

# M5M416160BJ, TP-6, -7, -6S, -7S

FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

## FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M416160BXX-6, -6S	60	15	30	15	110	430
M5M416160BXX-7, -7S	70	20	35	20	130	385

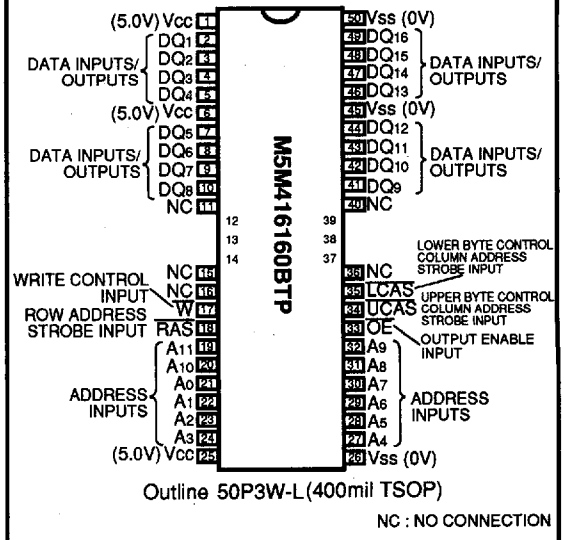
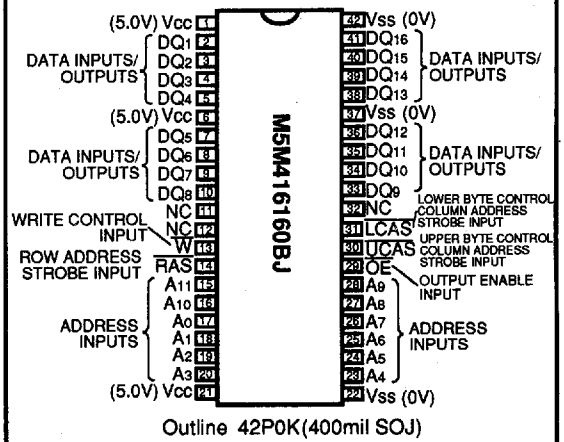
XX=J,TP

- Standard 42pin SOJ, 50pin TSOP
- Single 5.0V ± 10% supply
- Low stand-by power dissipation  
5.5mW (Max) ..... CMOS Input level
- Low operating power dissipation  
M5M416160Bxx -6, -6S ..... 530.0mW (Max)  
M5M416160Bxx -7, -7S ..... 470.0mW (Max)
- Fast-page mode, Read-modify-write, RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A<sub>0</sub> ~ A<sub>11</sub>)

## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

## PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

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**FUNCTION**

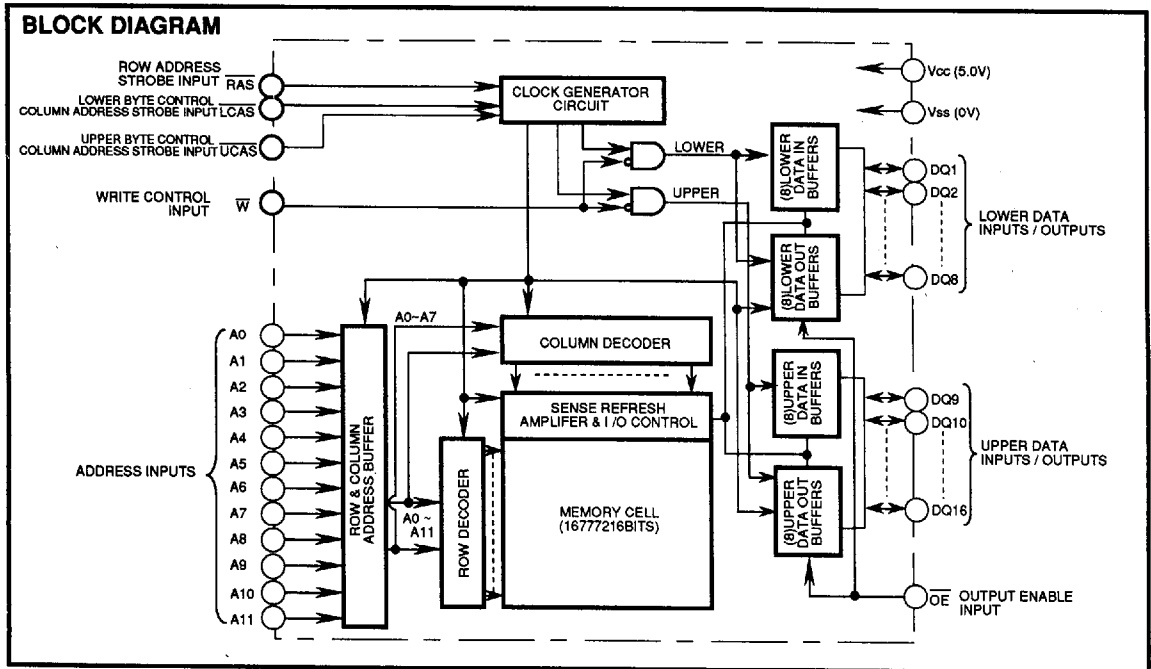
The M5M416160BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions,

e.g., fast page mode,  $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

**Table 1 Input conditions for each mode**

Operation	Inputs					Input/Output	
	$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Lower Byte Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper Byte Hidden refresh	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-1~7	V
V <sub>I</sub>	Input voltage	With respect to V <sub>SS</sub>	-1~7	V
V <sub>O</sub>	Output voltage		-1~7	V
I <sub>O</sub>	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.4		6.0	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-1		0.8	V

Note 1: All voltage values are with respect to V<sub>SS</sub>.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-5mA	2.4		Vcc	V	
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =4.2mA	0		0.4	V	
I <sub>OZ</sub>	Off-state output current	Q floating, 0V ≤ V <sub>OUT</sub> ≤ 5.5V	-10		10	μA	
I <sub>I</sub>	Input current	0V ≤ V <sub>IN</sub> ≤ 6V, Other inputs pins=0V	-10		10	μA	
I <sub>CC1</sub> (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M416160B-6,-6S	RAS, CAS cycling trc=twc=min, output open			95	mA
		M5M416160B-7,-7S				85	
I <sub>CC2</sub>	Supply current from Vcc, stand-by (Note 6)			RAS= CAS =V <sub>IH</sub> , output open		2	mA
		M5M416160B-6,-7	RAS= CAS ≥ Vcc-0.2V, output open		1		
		M5M416160B-6S,-7S	RAS= CAS ≥ Vcc-0.2V, output open		0.3		
I <sub>CC3</sub> (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M416160B-6,-6S	RAS cycling, CAS= V <sub>IH</sub> trc=min, output open			95	mA
		M5M416160B-7,-7S				85	
I <sub>CC4</sub> (AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M416160B-6,-6S	RAS=V <sub>IL</sub> , CAS cycling trc=min, output open			70	mA
		M5M416160B-7,-7S				60	
I <sub>CC8</sub> (AV)	Average supply current from Vcc CAS before RAS refresh mode (Note 3)	M5M416160B-6,-6S	CAS before RAS refresh cycling trc=min, output open			95	mA
		M5M416160B-7,-7S				85	

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1</sub>(AV), I<sub>CC3</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I<sub>CC1</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V<sub>IL</sub> and LCAS/UCAS=V<sub>IH</sub>.

CAPACITANCE (Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I(A)</sub>	Input capacitance, address inputs	V <sub>I</sub> =V <sub>SS</sub> f=1MHz V <sub>I</sub> =25mVrms			5	pF
C <sub>I(OE)</sub>	Input capacitance, OE input				7	pF
C <sub>I(W)</sub>	Input capacitance, W input				7	pF
C <sub>I(RAS)</sub>	Input capacitance, RAS input				7	pF
C <sub>I(CAS)</sub>	Input capacitance, CAS input				7	pF
C <sub>I/O</sub>	Input/Output capacitance, data ports				8	pF

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SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note7,8)		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note7,9)		60		70	ns
tAA	Column address access time (Note 7,10)		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		35		40	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	15	0	15	ns

Note 8: An initial pause of 500  $\mu$ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock such as  $\overline{\text{RAS}}$ -Only refresh).

Note the  $\overline{\text{RAS}}$  may be cycled during the initial pause. And any 8  $\overline{\text{RAS}}$  or  $\overline{\text{RAS}}/\overline{\text{CAS}}$  cycles are required after prolonged periods (greater than 64 ms) of  $\overline{\text{RAS}}$  inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 100pF,  $V_{OH}=2.4V$  ( $I_{OH}=-5mA$ ) and  $V_{OL}=0.4V$  ( $I_{OL}=4.2mA$ ).

8: Assumes that  $t_{RCD} \geq t_{RCD(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$ .

9: Assumes that  $t_{RCD} \leq t_{RCD(max)}$  and  $t_{RAD} \leq t_{RAD(max)}$ . If  $t_{RCD}$  or  $t_{RAD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by amount that  $t_{RCD}$  exceeds the value shown.

10: Assumes that  $t_{RAD} \geq t_{RAD(max)}$  and  $t_{ASC} \leq t_{ASC(max)}$ .

11: Assumes that  $t_{CP} \leq t_{CP(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$ .

12:  $t_{OFF(max)}$  and  $t_{OEZ(max)}$  defines the time at which the output achieves the high impedance state ( $I_{OH} \leq \pm 10 \mu A$ ) and is not reference to  $V_{OH(min)}$  or  $V_{OL(max)}$ .

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted, see notes 13,14)

Symbol	Parameter	Limits				Unit	
		M5M416160B-6,-6S		M5M416160B-7,-7S			
		Min	Max	Min	Max		
tREF	Refresh cycle time	-6, -7	64		64	ms	
tREF	Refresh cycle time	-6S, -7S	128		128	ms	
tRP	$\overline{\text{RAS}}$ high pulse width		40		50	ns	
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note15)		20	45	20	50	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low		10		10	ns	
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low		0		0	ns	
tCPN	$\overline{\text{CAS}}$ high pulse width		10		10	ns	
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note16)		15	30	15	35	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low		0		0	ns	
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note17)		0	10	0	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low		10		10	ns	
tCAH	Column address hold time after $\overline{\text{CAS}}$ low		15		15	ns	
tDZC	Delay time, data to $\overline{\text{CAS}}$ low (Note18)		0		0	ns	
tDZO	Delay time, data to $\overline{\text{OE}}$ low (Note18)		0		0	ns	
tCDD	Delay time, $\overline{\text{CAS}}$ high to data (Note19)		15		15	ns	
tODD	Delay time, $\overline{\text{OE}}$ high to data (Note19)		15		15	ns	
tT	Transition time (Note20)		1	50	1	50	ns

Note 13: The timing requirements are assumed  $t_r = 5ns$ .

14:  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals.

15:  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD(max)}$ , access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD(max)}$ , access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .  $t_{RCD(min)}$  is specified as  $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$ .

16:  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD} \geq t_{RAD(max)}$  and  $t_{ASC} \leq t_{ASC(max)}$ , access time is controlled exclusively by  $t_{AA}$ .

17:  $t_{ASC(max)}$  is specified as a reference point only. If  $t_{RCD} \geq t_{RCD(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$ , access time is controlled exclusively by  $t_{CAC}$ .

18: Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.

19: Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.

20:  $t_T$  is measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ .

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**Read and Refresh Cycles**

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
tRC	Read cycle time	110		130		ns
tRAS	RAS low pulse width	60	10000	70	10000	ns
tCAS	CAS low pulse width	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	60		70		ns
tRSH	RAS hold time after CAS low	15		20		ns
tRCS	Read Setup time before CAS low	0		0		ns
tRCH	Read hold time after CAS high (Note 21)	0		0		ns
tRRH	Read hold time after RAS high (Note 21)	10		10		ns
tRAL	Column address to RAS hold time	30		35		ns
tOCH	CAS hold time after OE low	15		20		ns
tORH	RAS hold time after OE low	15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

**Write Cycle (Early Write and Delayed Write)**

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
tWC	Write cycle time	110		130		ns
tRAS	RAS low pulse width	60	10000	70	10000	ns
tCAS	CAS low pulse width	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	60		70		ns
tRSH	RAS hold time after CAS low	15		20		ns
tWCS	Write setup time before CAS low (Note 23)	0		0		ns
tWCH	Write hold time after CAS low	10		10		ns
tCWL	CAS hold time after W low	15		20		ns
tRWL	RAS hold time after W low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before CAS low or W low	0		0		ns
tDH	Data hold time after CAS low or W low	10		15		ns
tOEH	OE hold time after W low	15		20		ns

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**Read-Write and Read-Modify-Write Cycles**

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note22)	155		180		ns
trAS	RAS low pulse width	105	10000	120	10000	ns
tcAS	CAS low pulse width	60	10000	70	10000	ns
tcSH	CAS hold time after RAS low	105		120		ns
trSH	RAS hold time after CAS low	60		70		ns
trCS	Read setup time before CAS low	0		0		ns
tcWD	Delay time, CAS low to $\bar{W}$ low (Note23)	40		45		ns
trWD	Delay time, RAS low to $\bar{W}$ low (Note23)	85		95		ns
tAWD	Delay time, address to $\bar{W}$ low (Note23)	55		60		ns
tcWL	CAS hold time after $\bar{W}$ low	15		20		ns
trWL	RAS hold time after $\bar{W}$ low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before $\bar{W}$ low	0		0		ns
tDH	Data hold time after $\bar{W}$ low	10		15		ns
tOEH	OE hold time after $\bar{W}$ low	15		15		ns

Note 22: trWC is specified as  $trWC_{(min)} = trAC_{(max)} + tODD_{(min)} + trWL_{(min)} + trP_{(min)} + 5t$ .

23: twCS, tcWD, trWD and tAWD and tcPWD are specified as reference points only. If  $twCS \geq twCS_{(min)}$  the cycle is an early write cycle and the DQpins will remain high impedance throughout the entire cycle. If  $tcWD \geq tcWD_{(min)}$ ,  $trWD \geq trWD_{(min)}$ ,  $tAWD \geq tAWD_{(min)}$  and  $tcPWD \geq tcPWD_{(min)}$  (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to  $V_{IH}$ ) is indeterminate.

**Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)**

Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	85		95		ns
trAS	RAS low pulse width for read write cycle (Note25)	100	125000	115	125000	ns
tcP	CAS high pulse width (Note26)	10	15	10	15	ns
tcPRH	RAS hold time after CAS precharge	35		40		ns
tcPWD	Delay time, CAS precharge to $\bar{W}$ low (Note23)	60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: trAS<sub>(min)</sub> is specified as two cycles of CAS input are performed.

26: tcP<sub>(max)</sub> is specified as a reference point only.

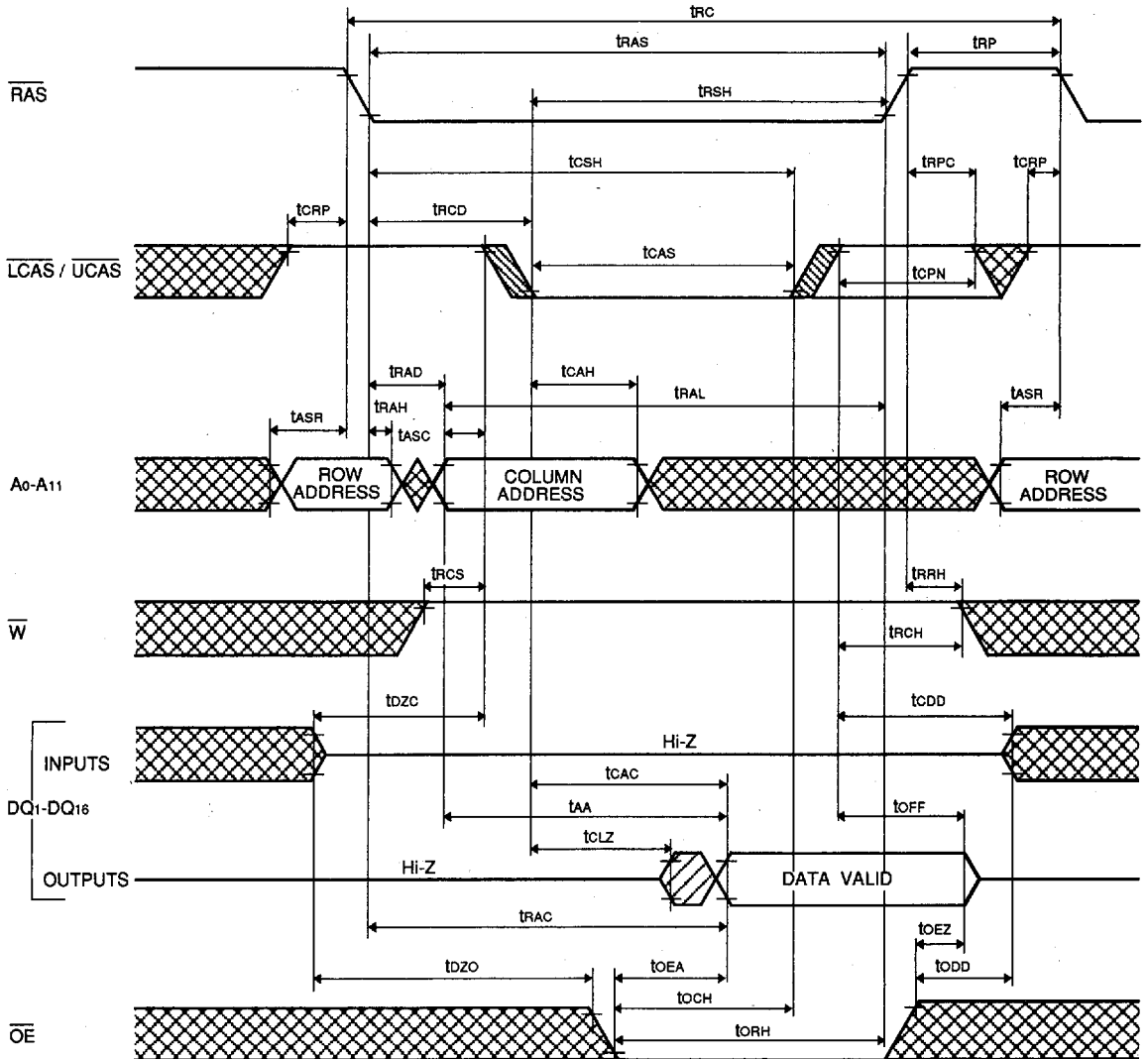
**CAS before RAS Refresh Cycle (Note 27)**




Symbol	Parameter	Limits				Unit
		M5M416160B-6,-6S		M5M416160B-7,-7S		
		Min	Max	Min	Max	
tcSR	CAS setup time before RAS low	10		10		ns
tCHR	CAS hold time after RAS low	10		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

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Timing Diagrams (Note 28)  
Read Cycle



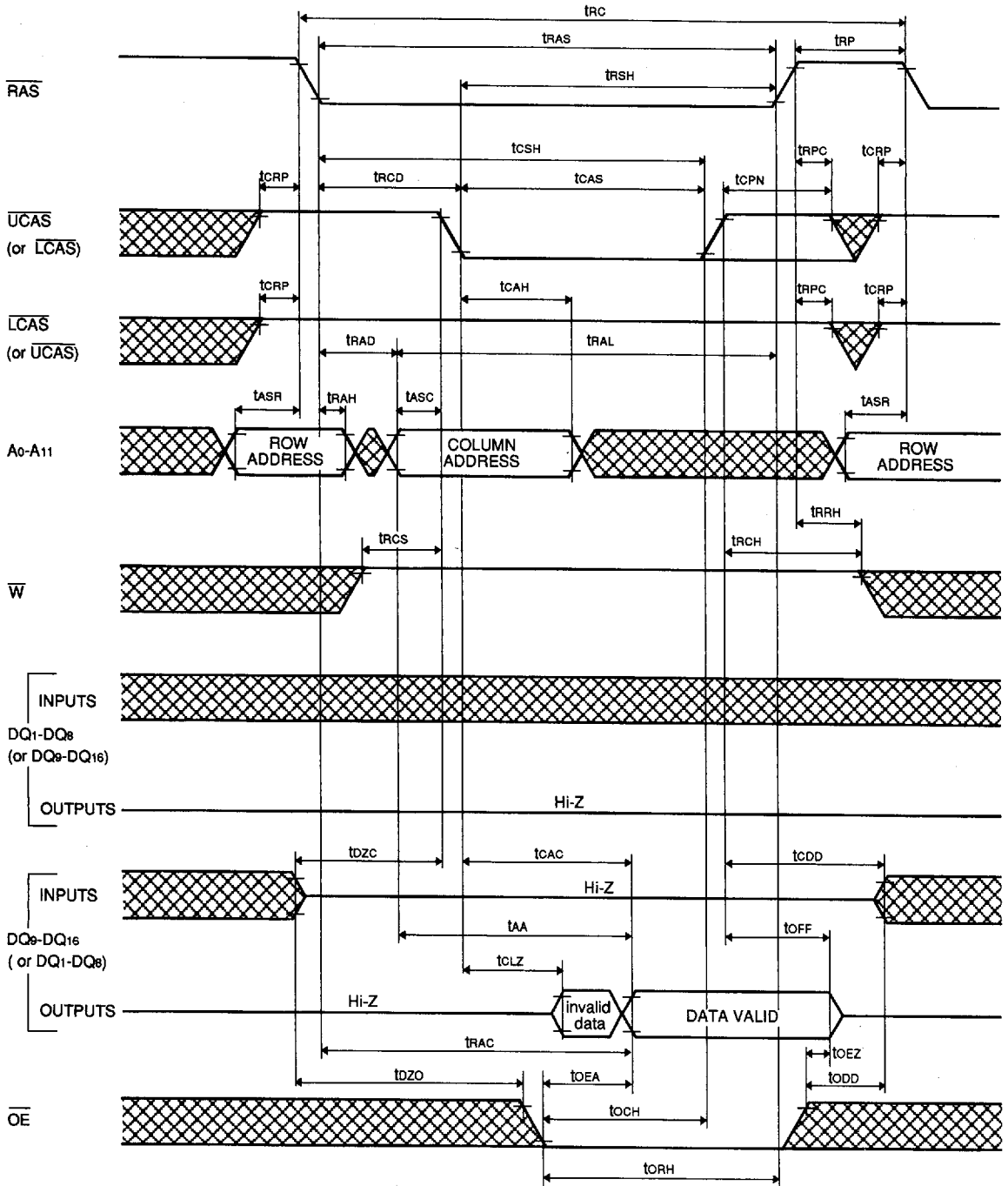
- Note 28
-  Indicates the don't care input.  
 $V_{IH(min.)} \leq V_{IN} \leq V_{IH(max.)}$  or  $V_{IL(min.)} \leq V_{IN} \leq V_{IL(max.)}$
  -  Indicates the invalid output.
  -  Indicates the skew of the two inputs.

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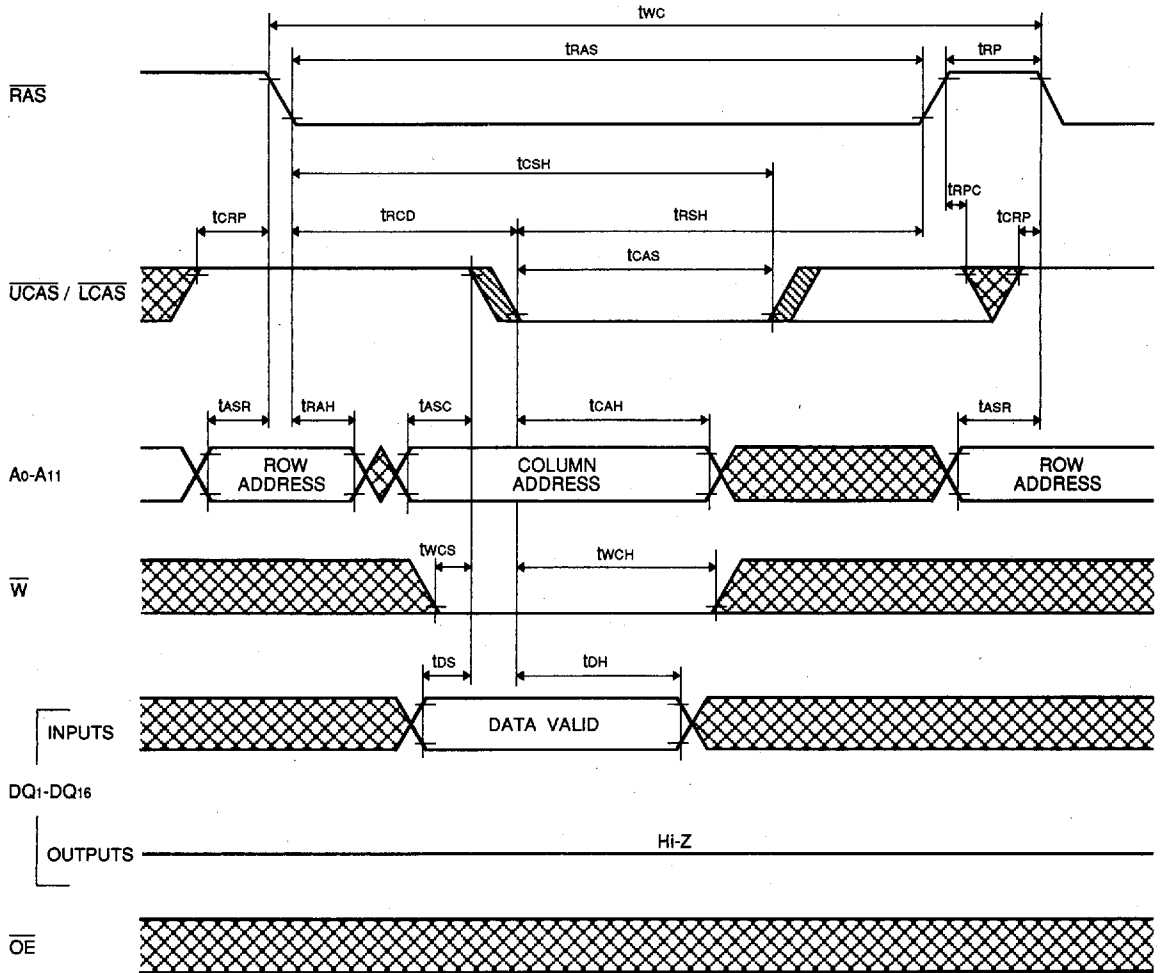
Upper / (Lower) Byte Read Cycle



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**Write Cycle ( Early write )**

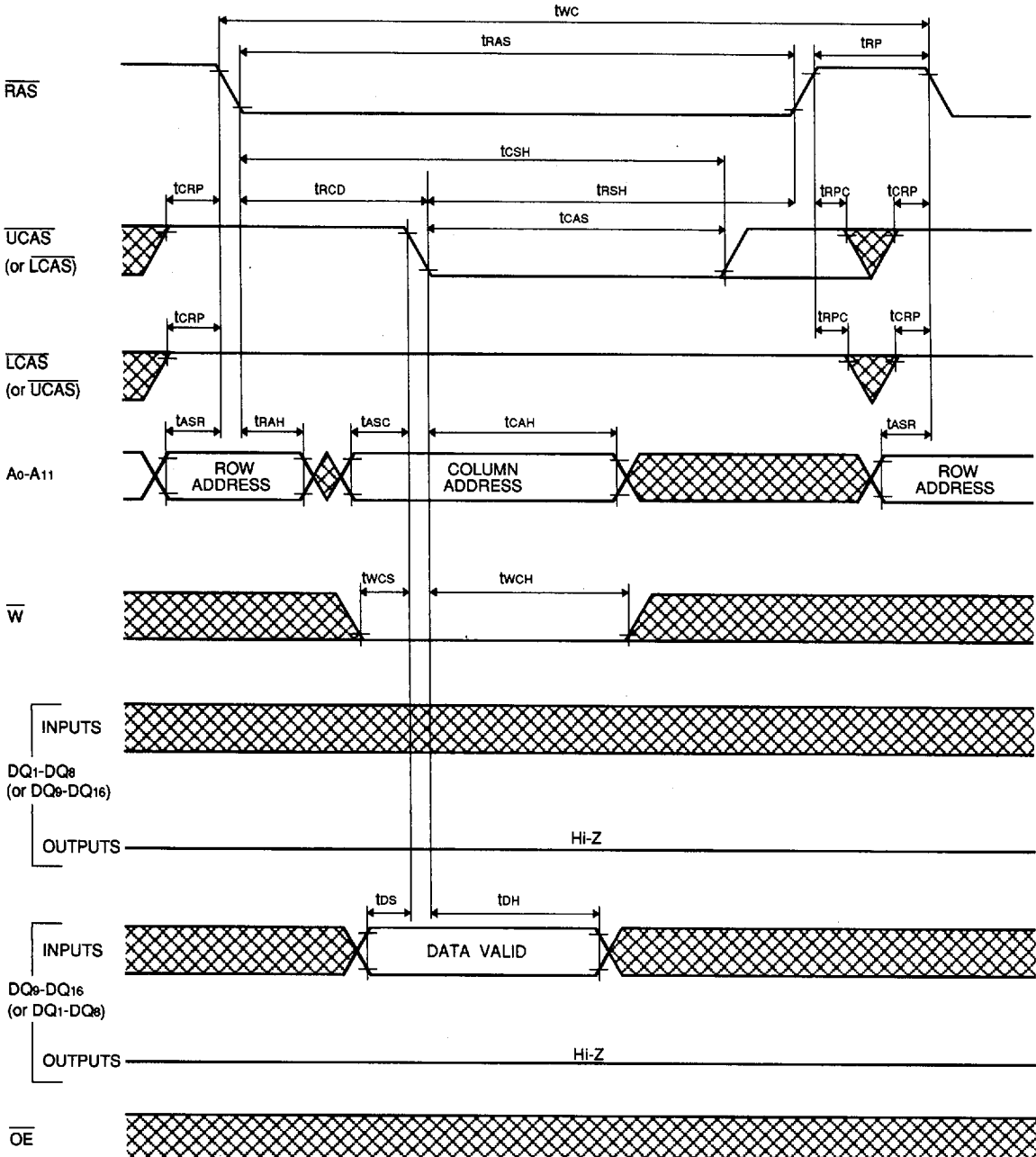


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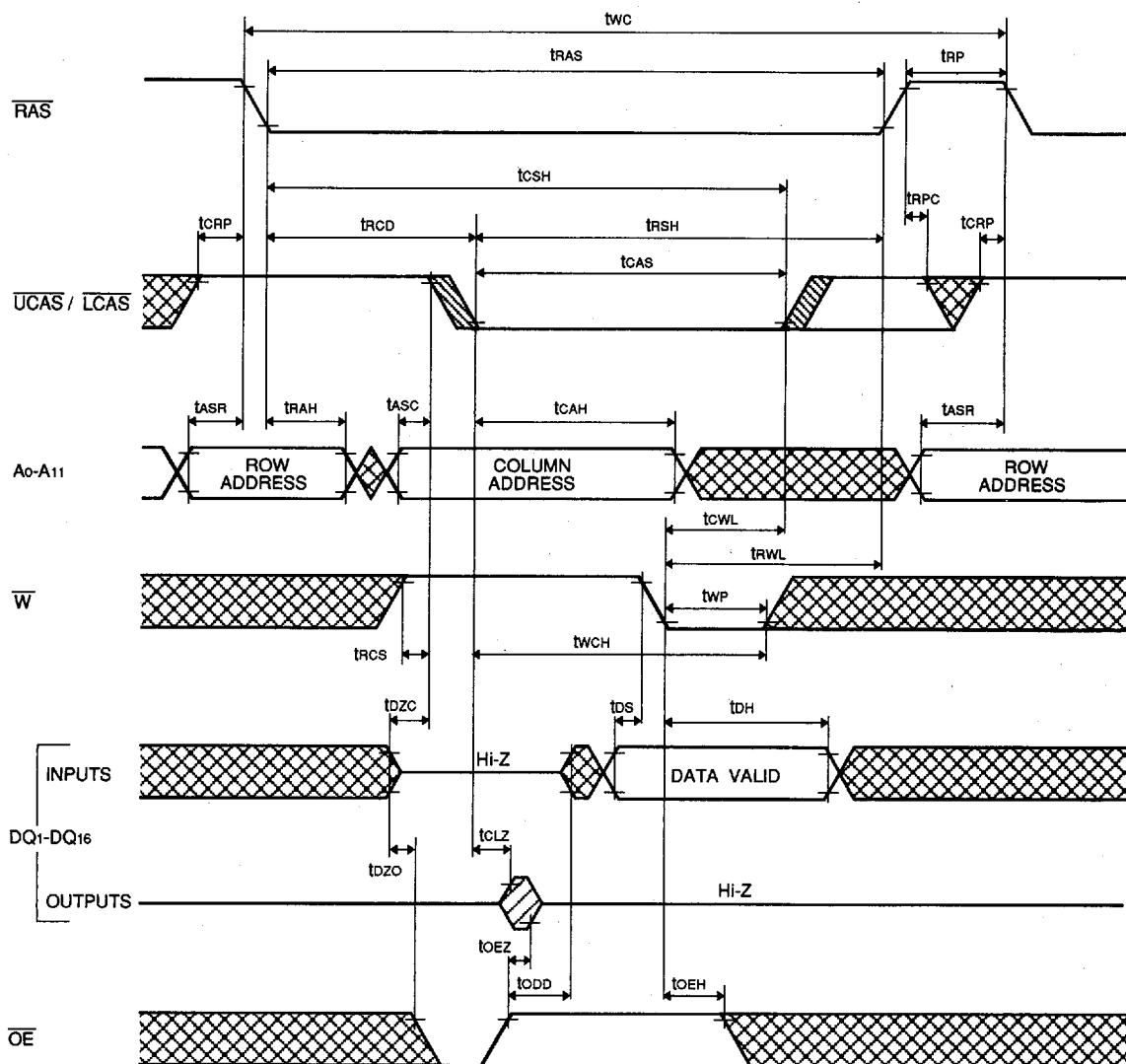
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Upper/(Lower) Byte Write Cycle ( Early write )



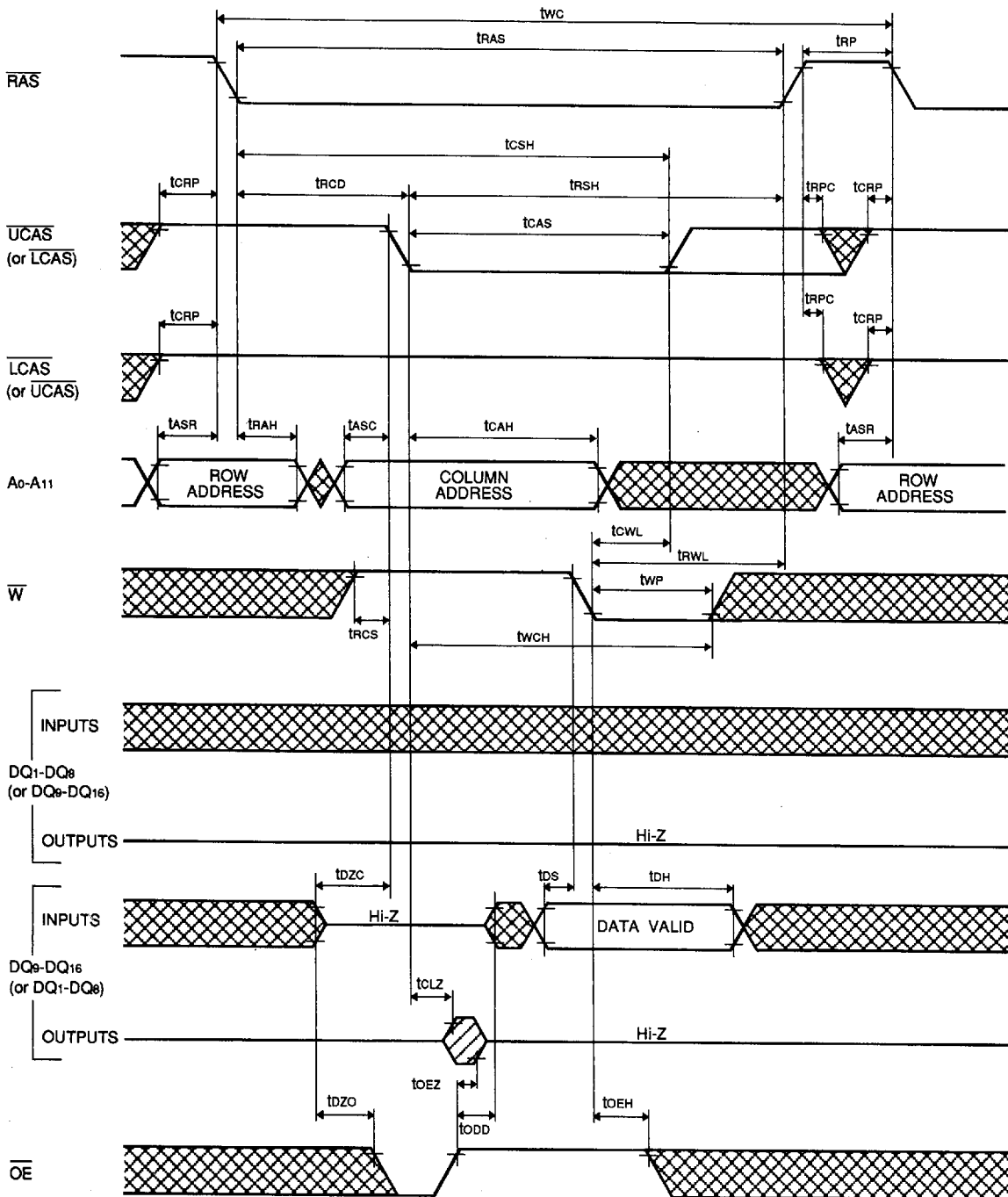
**Write Cycle ( Delayed write )**



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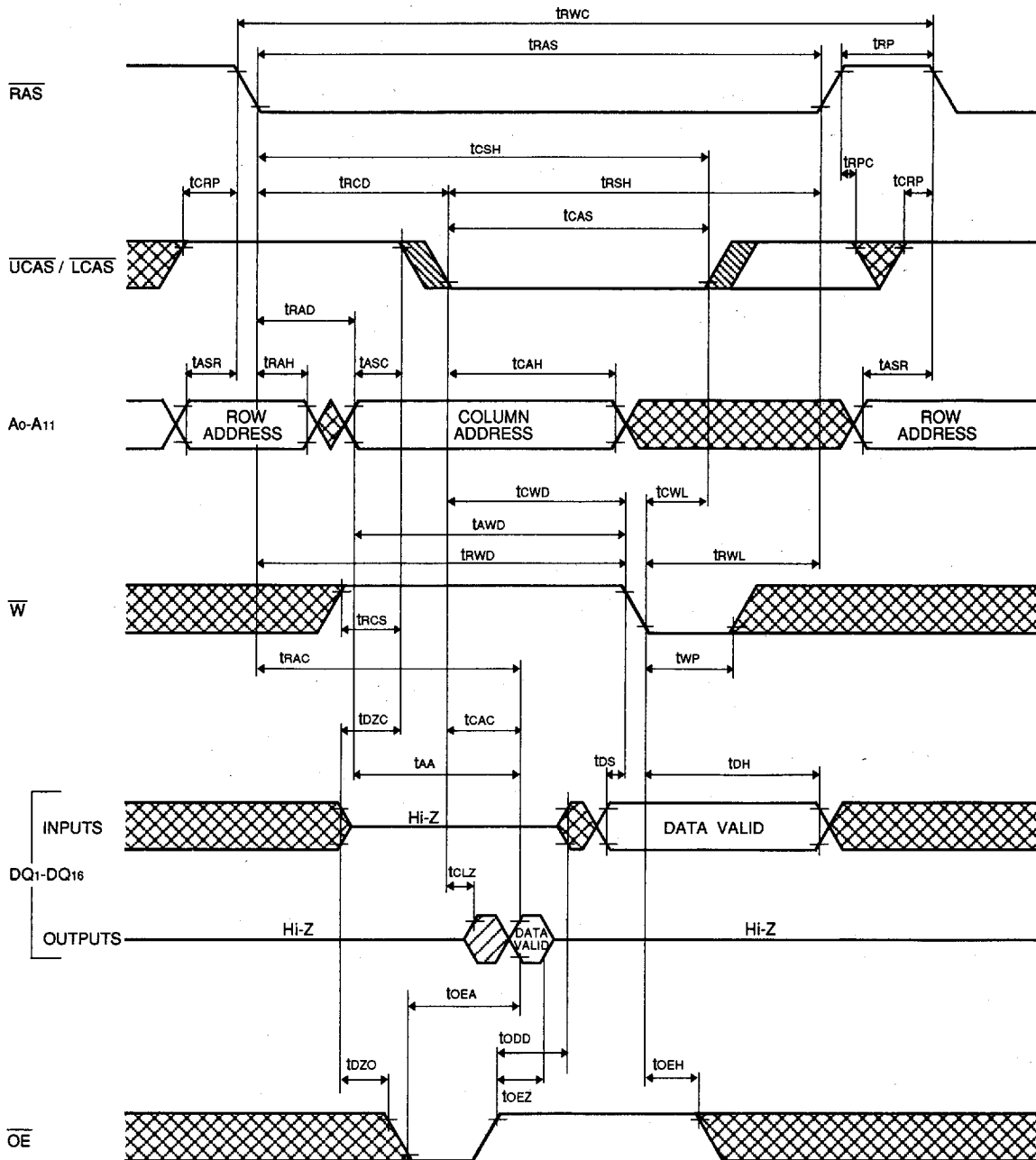
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**Upper/(Lower) Byte Write Cycle ( Delayed write )**



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Read-Write, Read-Modify-Write Cycle

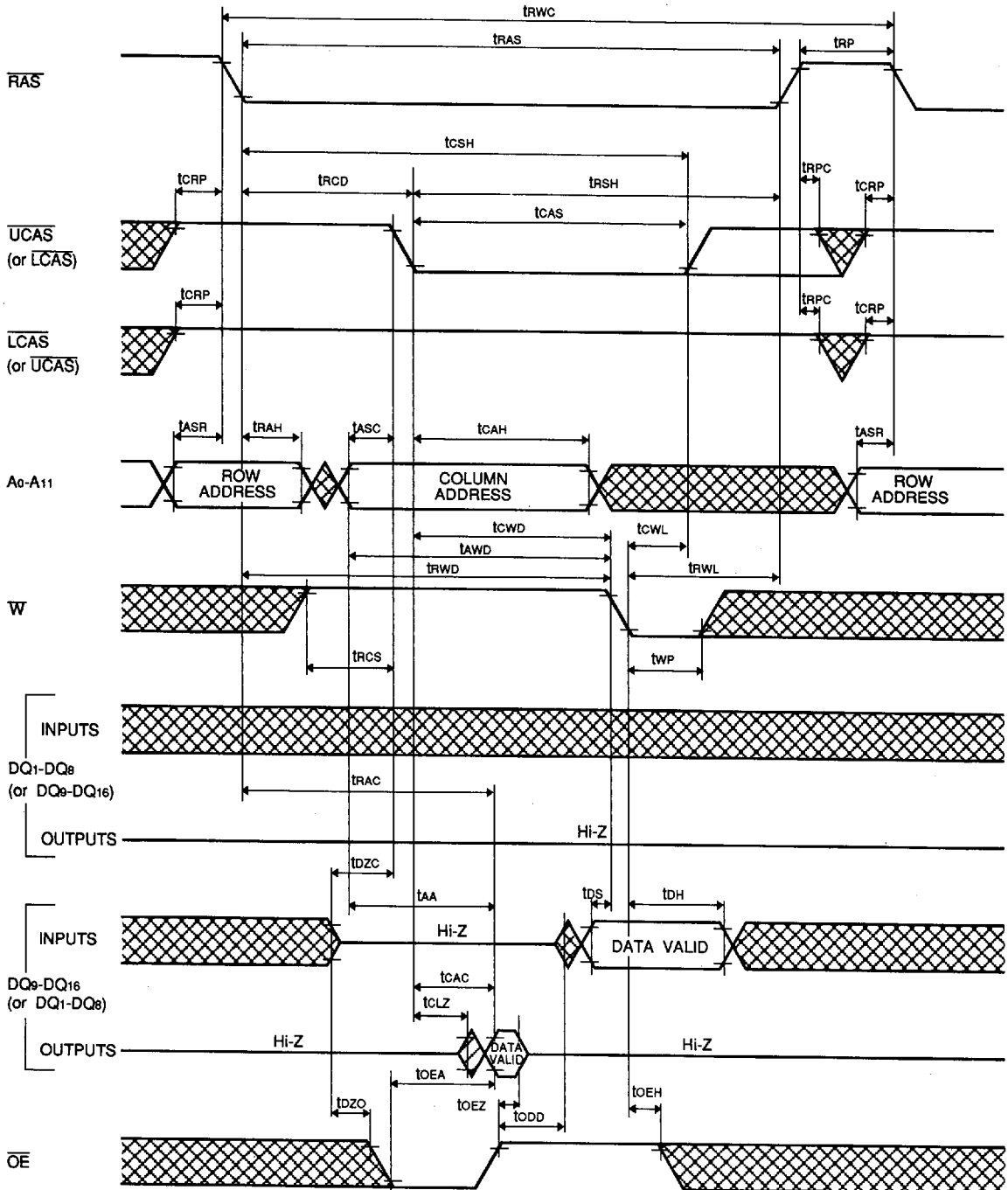


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Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle

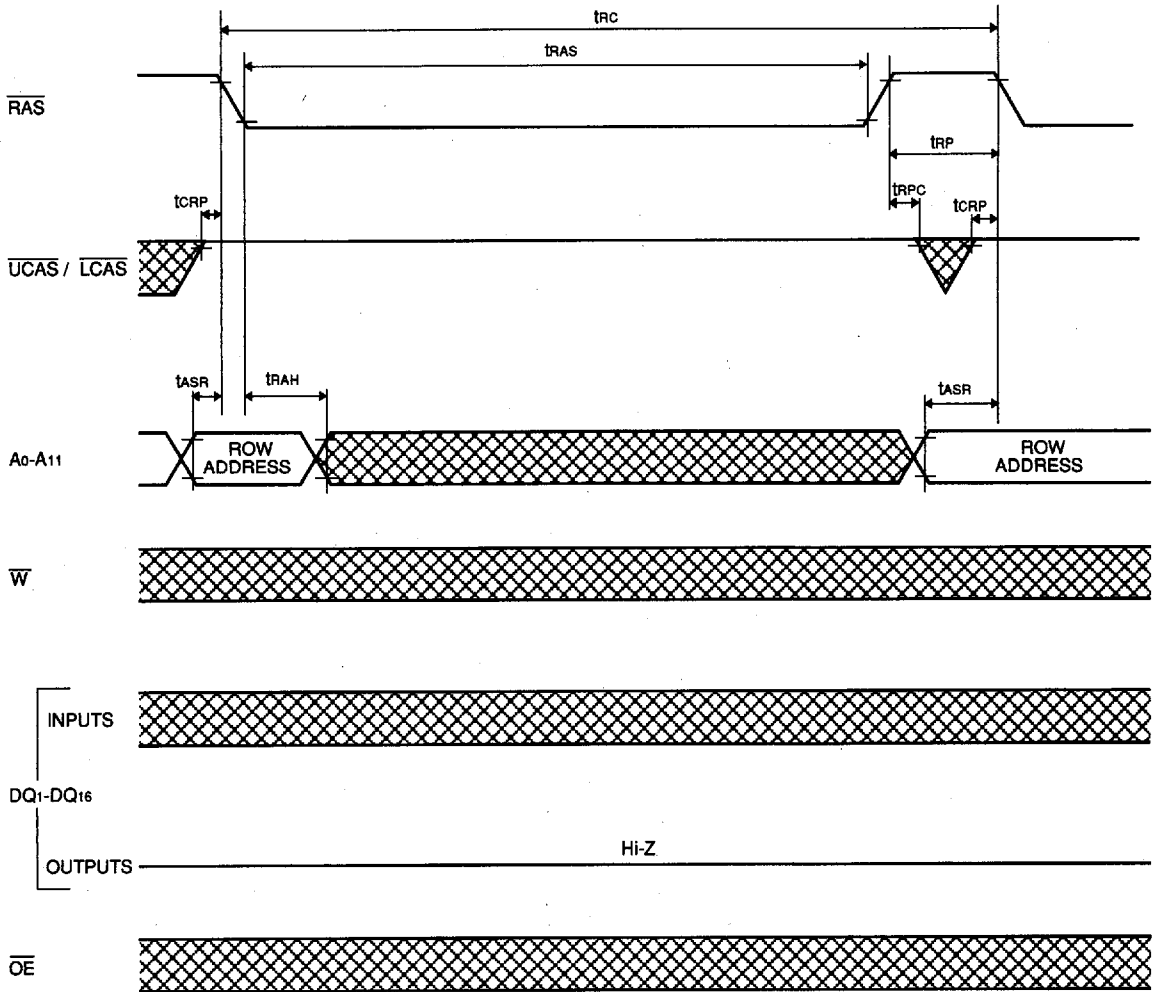


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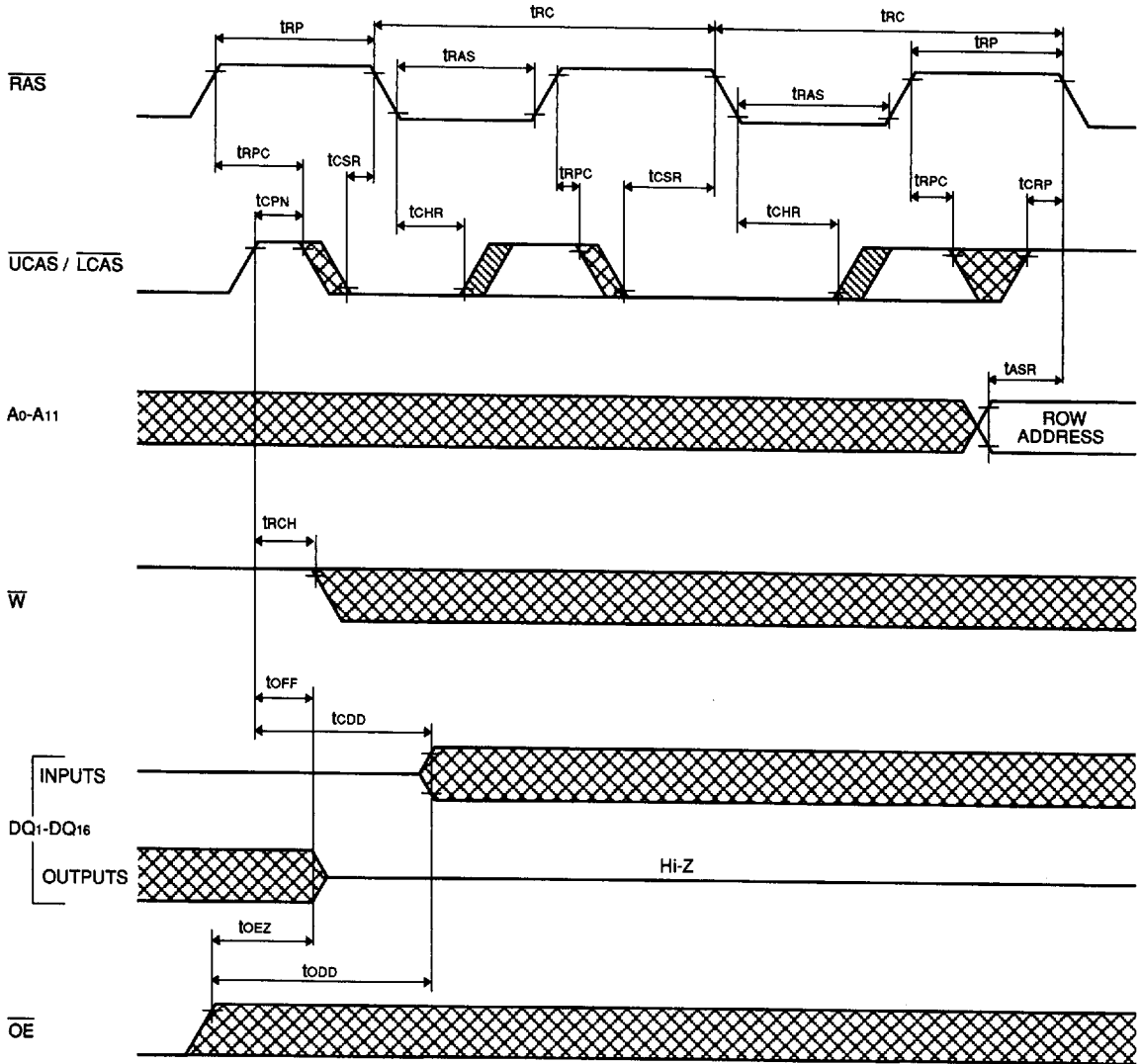
**RAS-only Refresh Cycle**



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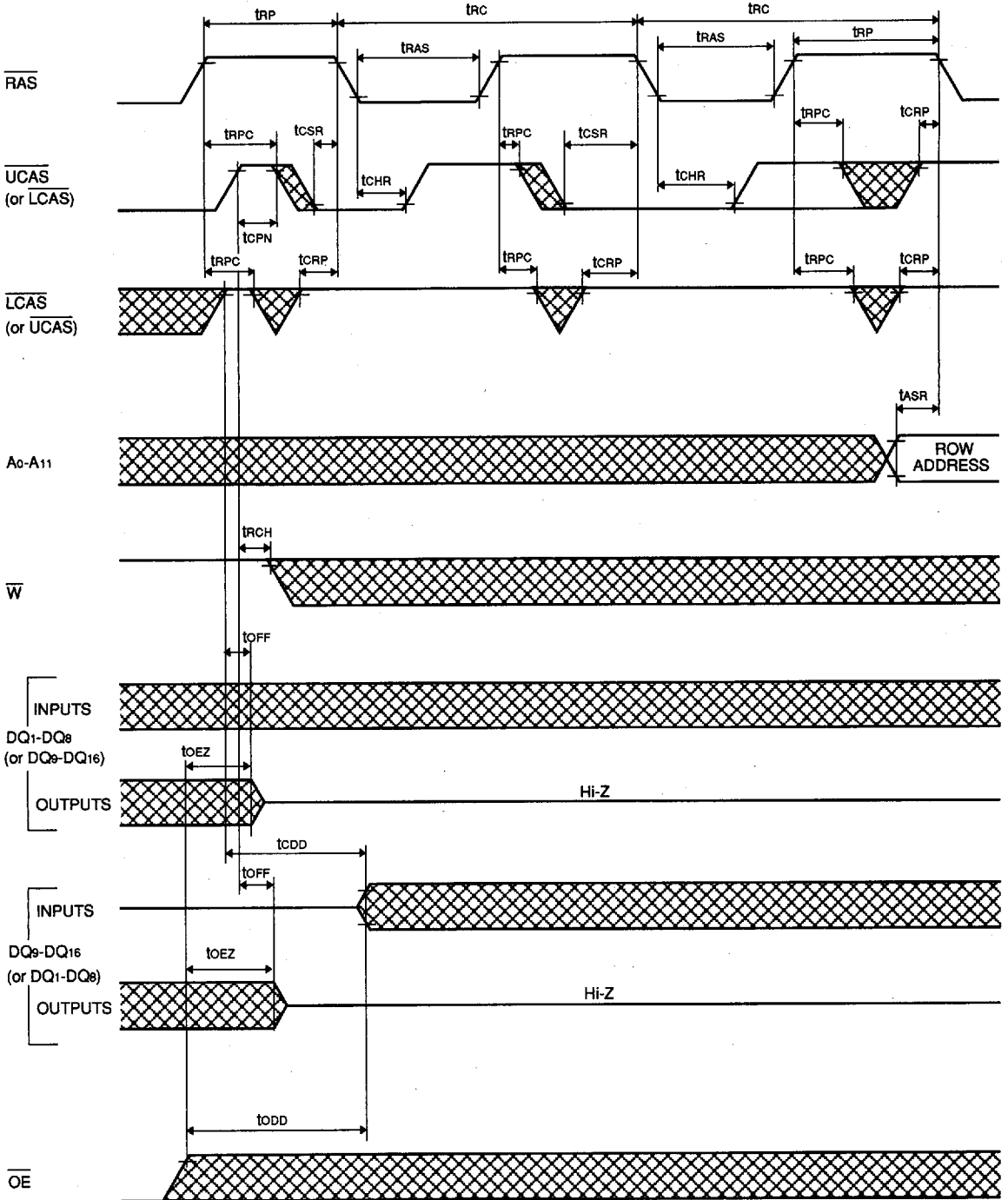


**CAS before RAS Refresh Cycle**





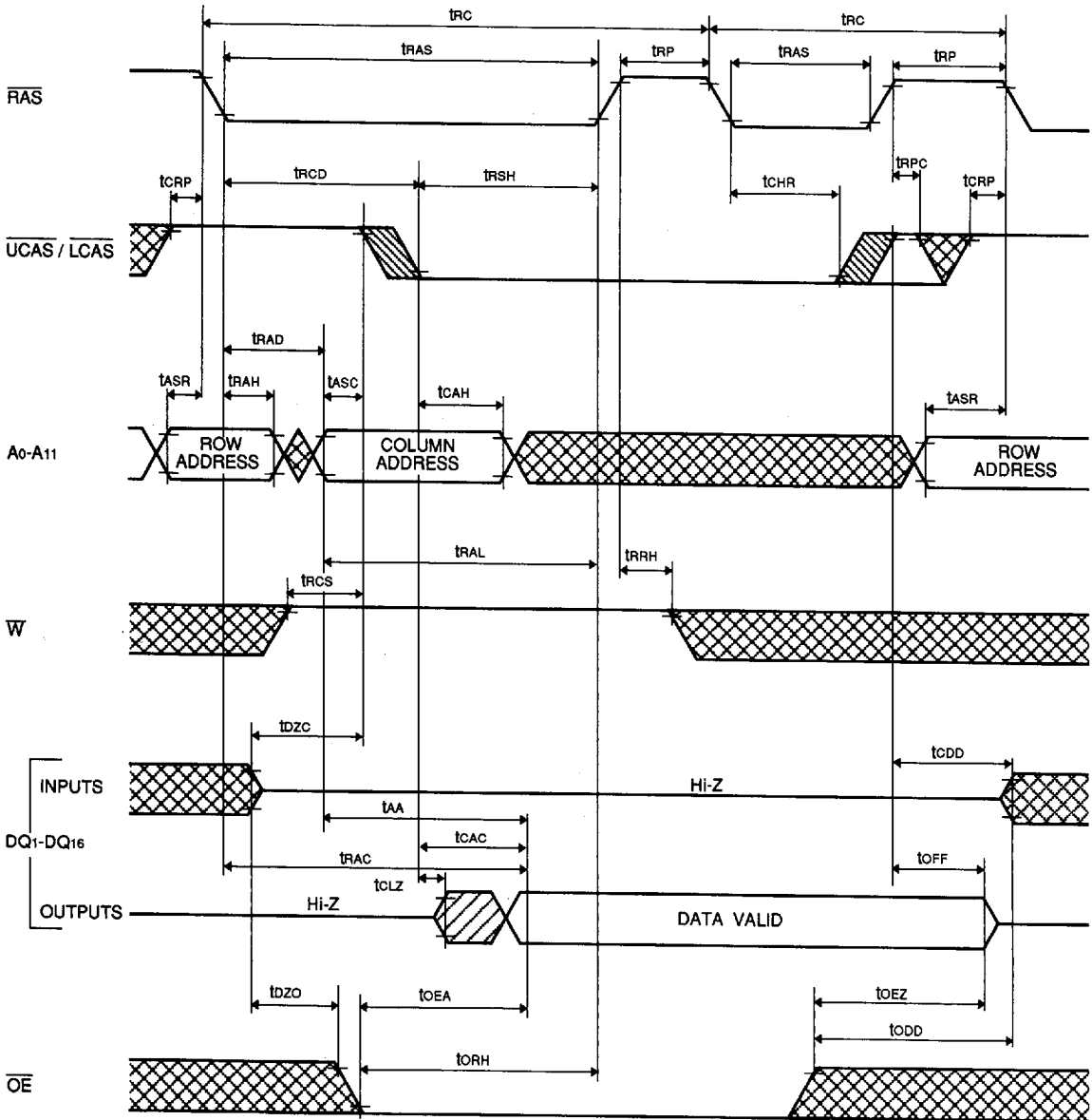
**Upper/(Lower) CAS before RAS Refresh Cycle**



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**FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

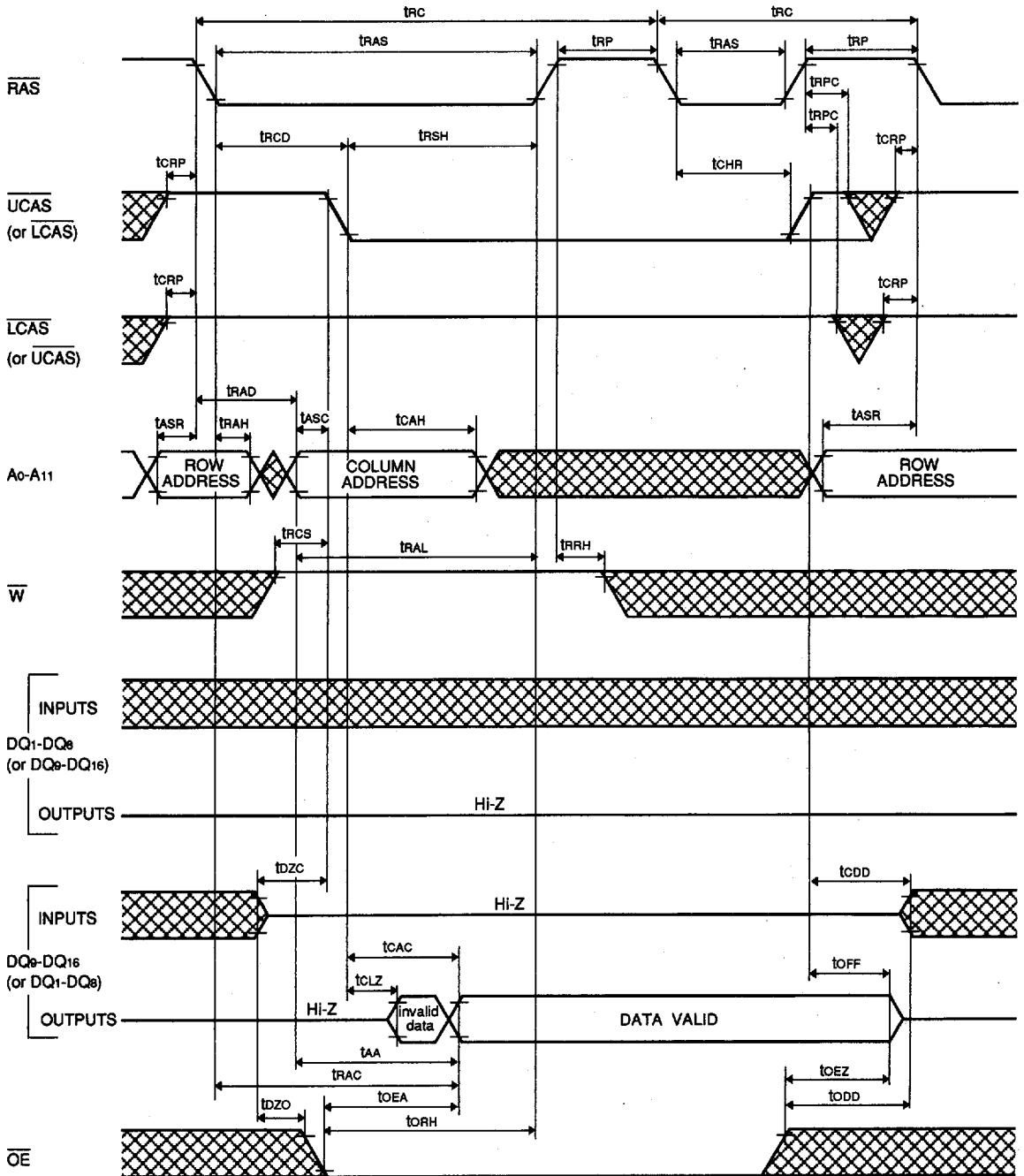
**Hidden Refresh Cycle (Read) (Note 29)**



Note 29: Early write, delayed write, read write or read modify write cycle is applicable as well as read cycle.  
 Timing requirements and output state are the same as that of each cycle shown above.

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Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 29)

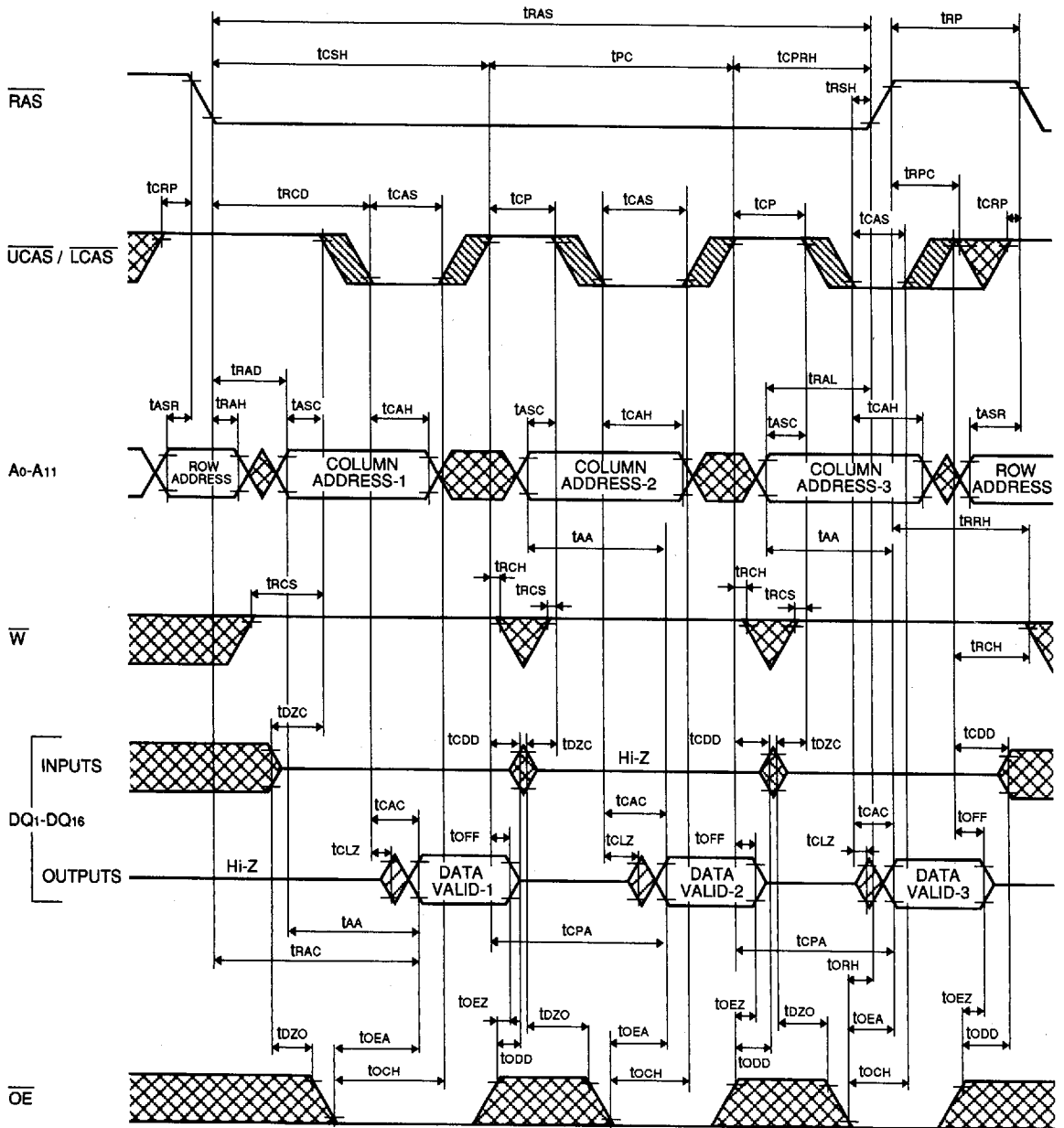


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M5M416160BJ, TP-6,-7,-6S,-7S

FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Fast Page Mode Read Cycle



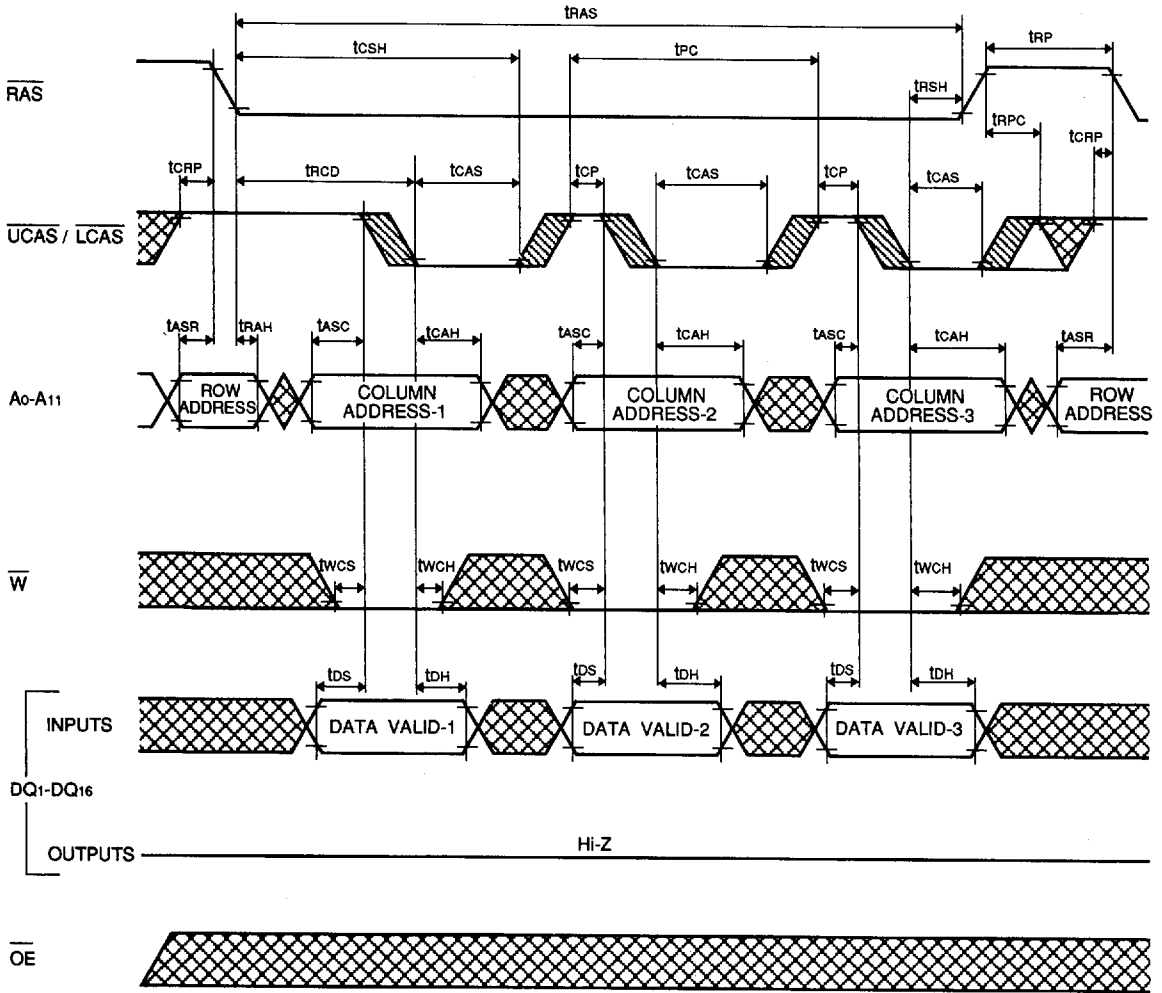
6249825 0028731 91T





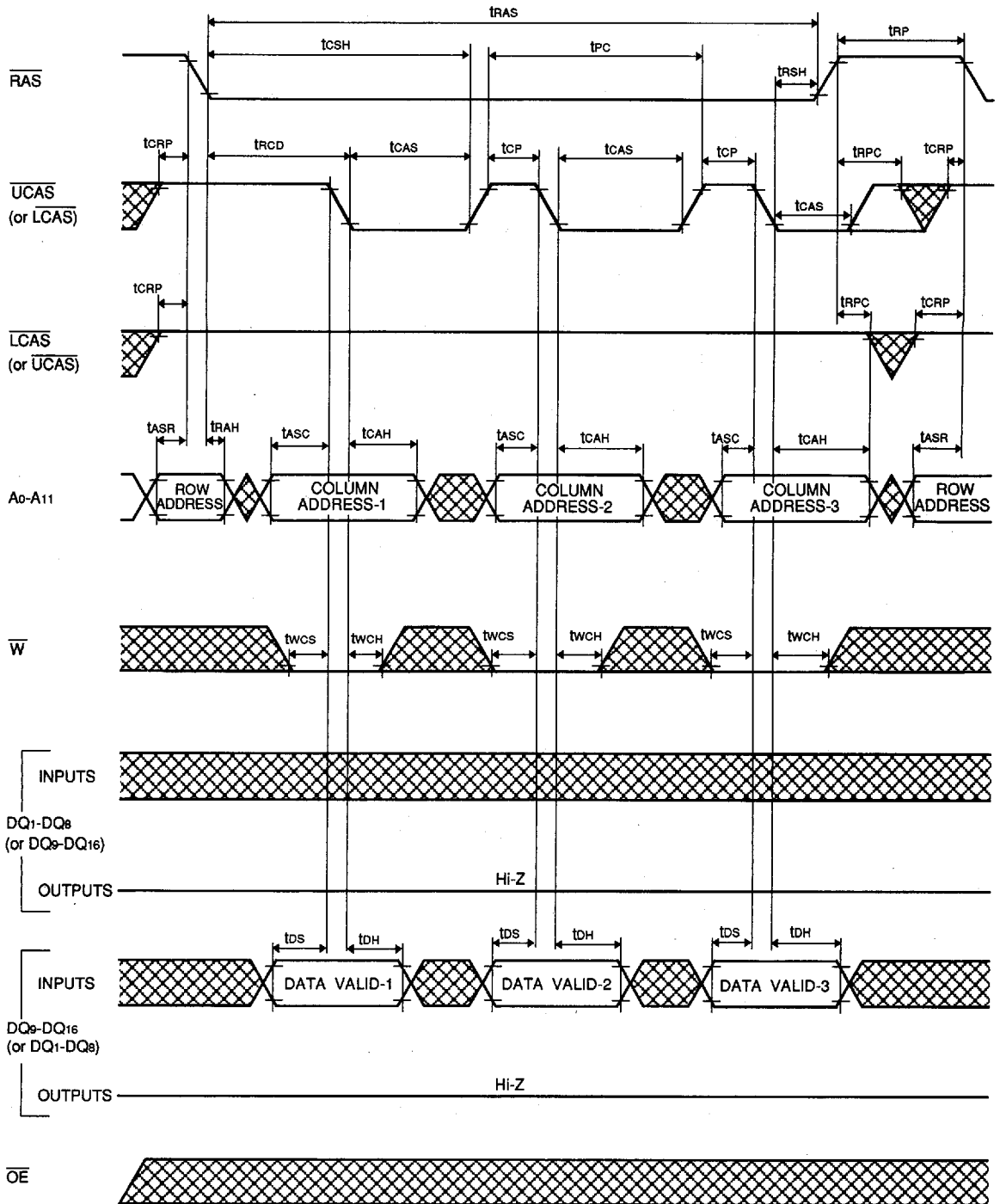
**FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Fast Page Mode Write Cycle ( Early Write )**



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**Fast Page Mode Upper/(Lower) Byte Write Cycle ( Early Write )**

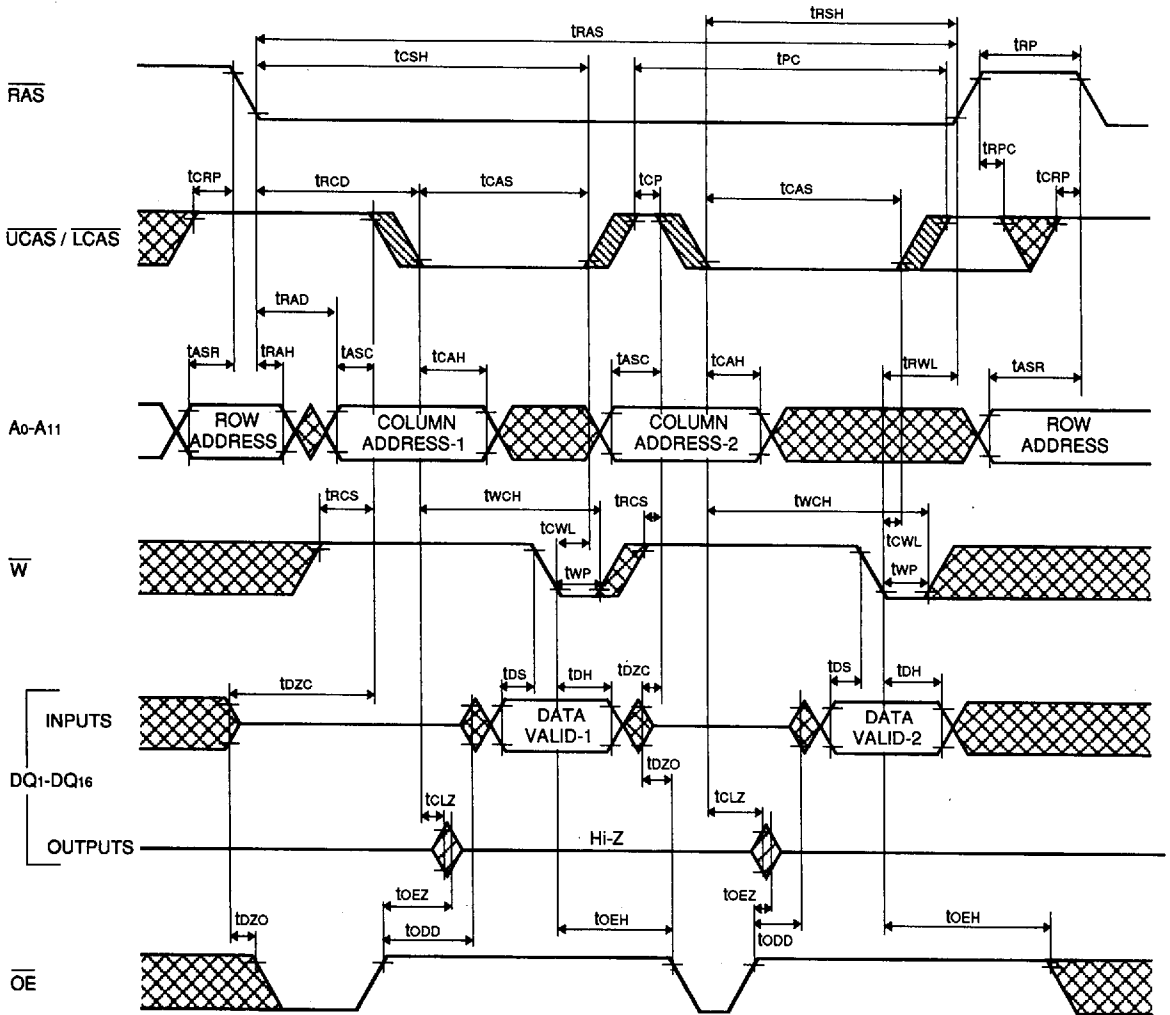


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MITSUBISHI LSIs  
**M5M416160BJ,TP-6,-7,-6S,-7S**

**FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Fast Page Mode Write Cycle ( Delayed Write )**



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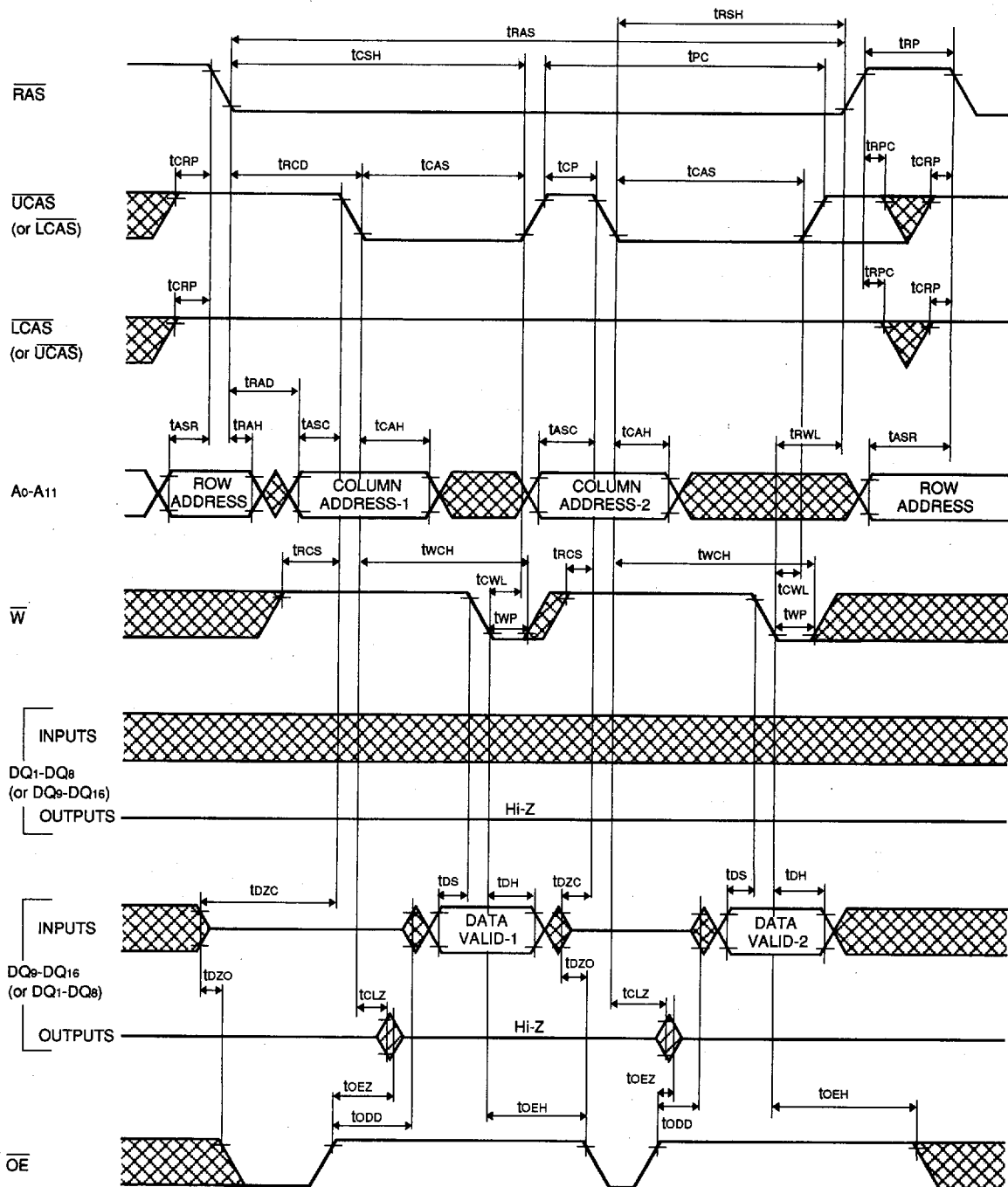




MITSUBISHI LSIs  
**M5M416160BJ,TP-6,-7,-6S,-7S**

**FAST PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM**

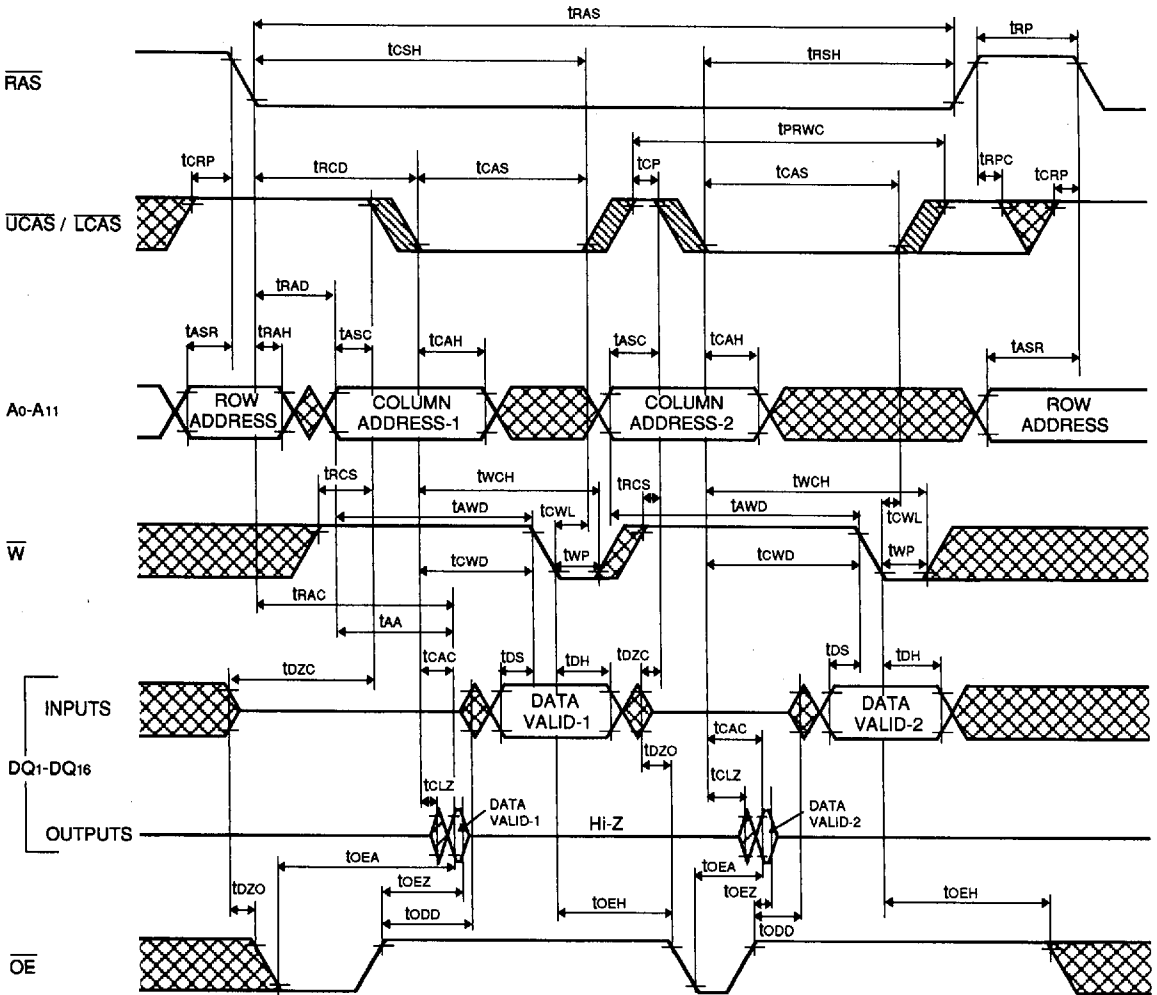
**Fast Page Mode Upper / (Lower) Byte Write ( Delayed Write )**



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**FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

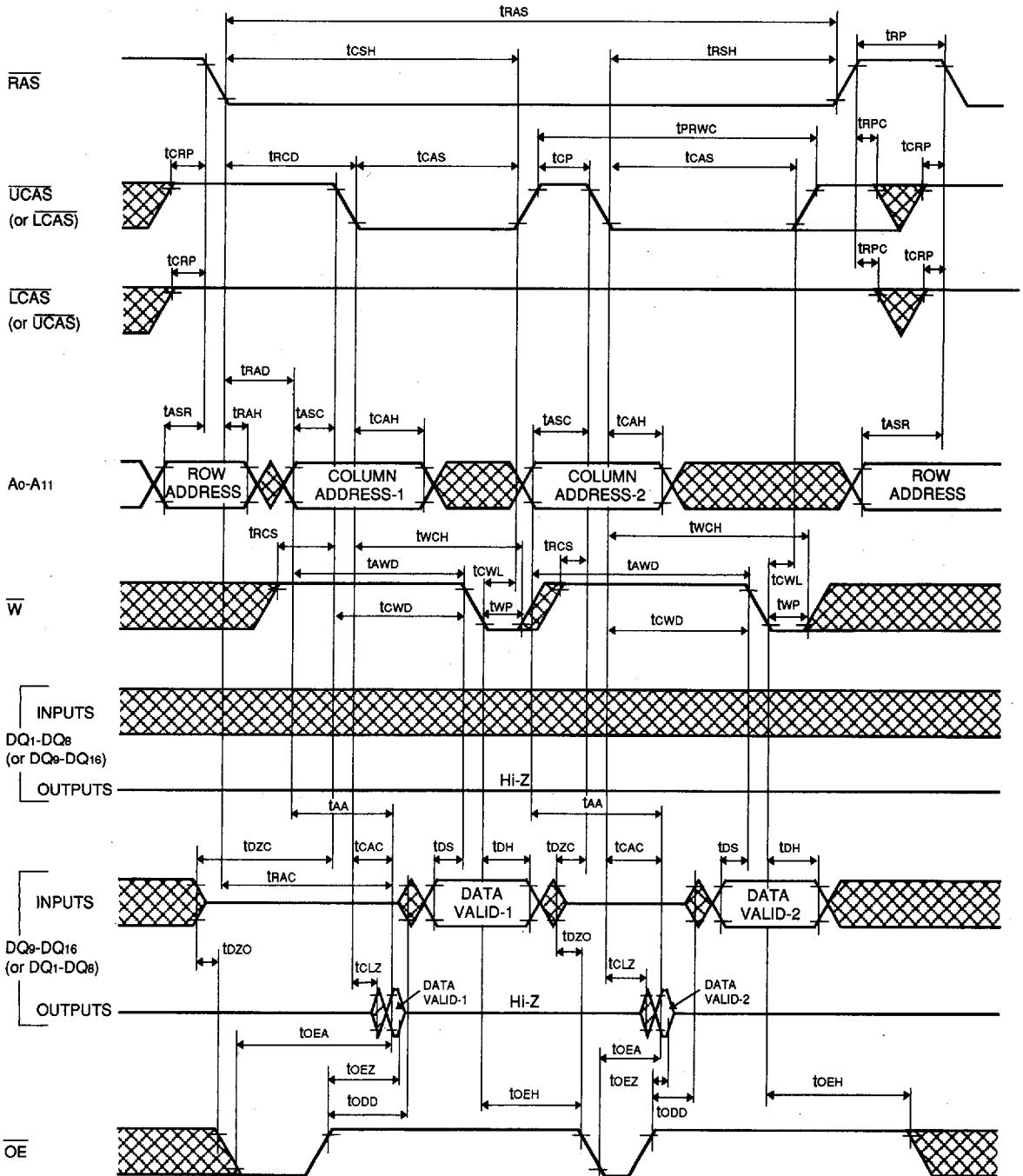
**Fast Page Mode Read-Write, Read-Modify-Write Cycle**



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**FAST PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM**

**Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle**



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**SELF REFRESH SPECIFICATIONS**

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

**ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>ccs</sub>	Supply current from Vcc Extended refresh cycle	M5M416160B -6S,-7S  RAS cycling CAS ≤ 0.2V or CAS before RAS refresh cycling W ≤ 0.2V or ≥ Vcc - 0.2V OE ≤ 0.2V or ≥ Vcc - 0.2V A0~A11 ≤ 0.2V or ≥ Vcc - 0.2V DQ = open tREF = 128ms tRAS = tRAS min ~ 1 μs			600	μA
I <sub>ccs</sub> (AV)	Average supply current from Vcc Self - Refresh cycle	M5M416160B -6S,-7S  RAS = CAS ≤ 0.2V			400	μA

**TIMING REQUIREMENTS** (Ta=0~70°C, Vcc=5V ±10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M416160B-6S		M5M416160B-7S		
		Min	Max	Min	Max	
t <sub>RAS</sub>	Self Refresh RAS low pulse width	100		100		μs
t <sub>RPS</sub>	Self Refresh RAS high precharge time	90		110		ns
t <sub>CHS</sub>	Self Refresh RAS hold time	- 50		- 50		ns

**SELF REFRESH ENTRY & EXIT CONDITIONS**

(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t<sub>ns</sub> / t<sub>sn</sub> before / after self refresh , on the condition of t<sub>ns</sub> ≤ 64 ms and t<sub>sn</sub> ≤ 64 ms.



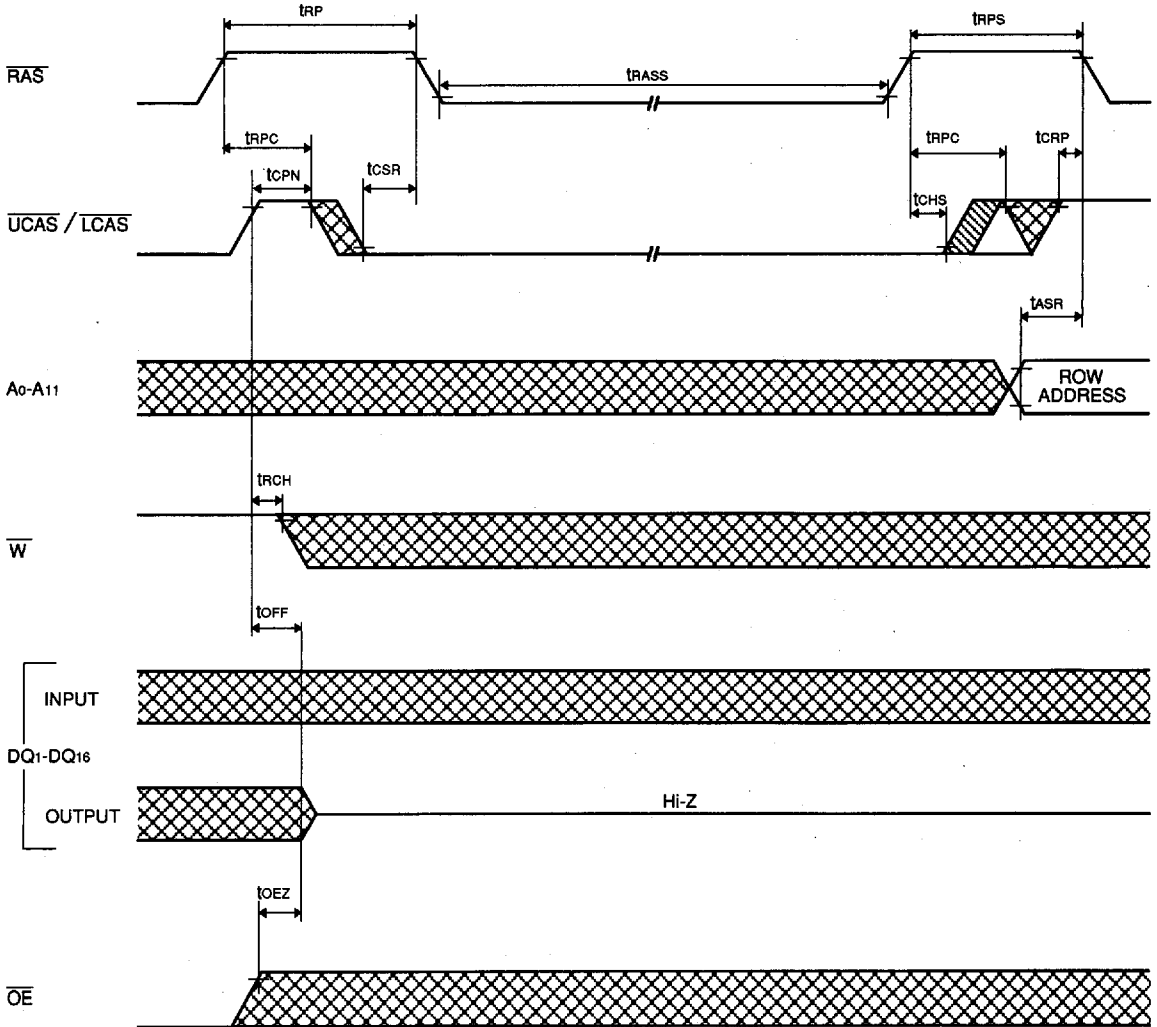
(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t<sub>ns</sub> / t<sub>sn</sub> before / after self refresh , on the condition of t<sub>ns</sub> + t<sub>sn</sub> ≤ 64 ms.



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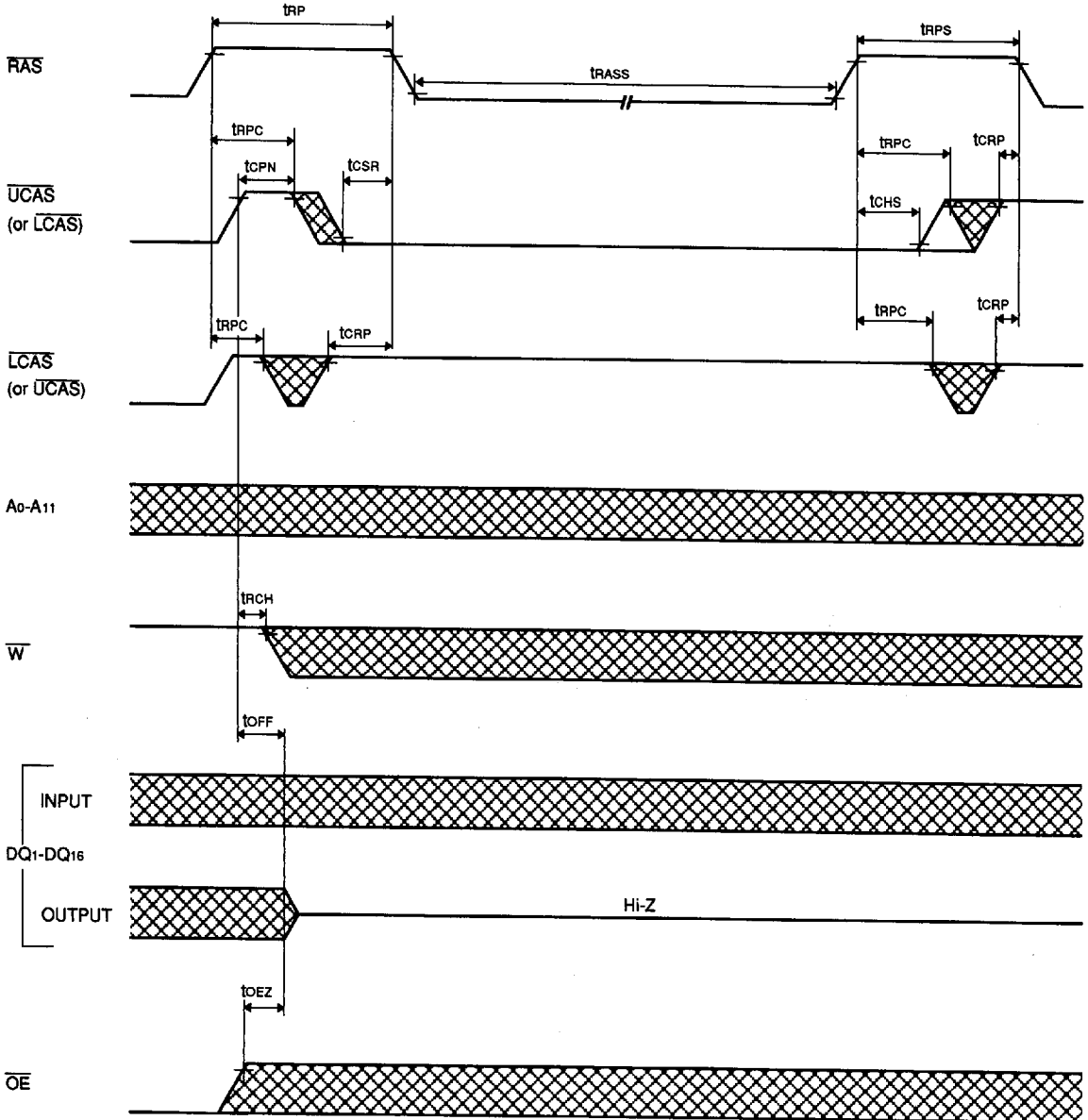
**Self Refresh Cycle**



MITSUBISHI LSIs  
**M5M416160BJ,TP-6,-7,-6S,-7S**

FAST PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Upper/(Lower) Self Refresh Cycle\*



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