Integrated Device Technology, Inc.

HIGH-SPEED 2K X 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT71V33S/L
IDT71V43S/L

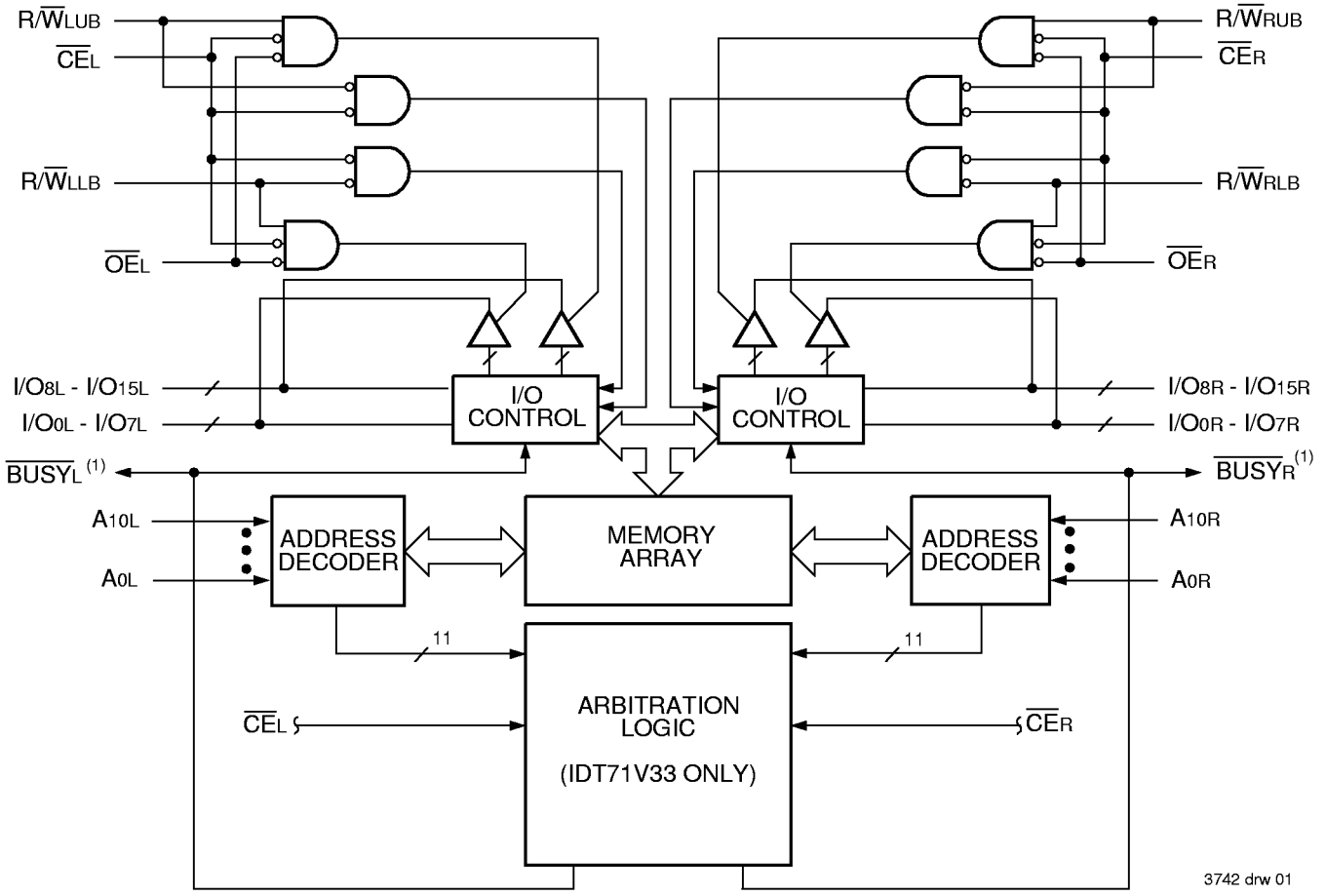
FEATURES:

- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT71V33/43S
    Active: 750 mW (typ.)
    Standby: 3.3mW (typ.)
  - — IDT71V33/43L
    Active: 750mW (typ.)
    Standby: 660µW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT71V33 easily expands data bus width to 32 bits or more using SLAVE IDT71V43
- On-chip port arbitration logic (IDT71V33 only)
- BUSY output flag on IDT71V33; BUSY input on IDT71V43
- Fully asynchronous operation from either port
- LVTTL-compatible; single 3.3V (±0.3V) power supply
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in a 68-pin PLCC, and 100-pin TQFP

DESCRIPTION:

The IDT71V33/71V43 are HIGH-speed 2K x 16 Dual-Port Static RAMs. The IDT71V33 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT71V43 "SLAVE" Dual-Port in

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. IDT71V33 (MASTER): BUSY is open drain output and requires pull-up resistor.
   IDT71V43 (SLAVE): BUSY is input.

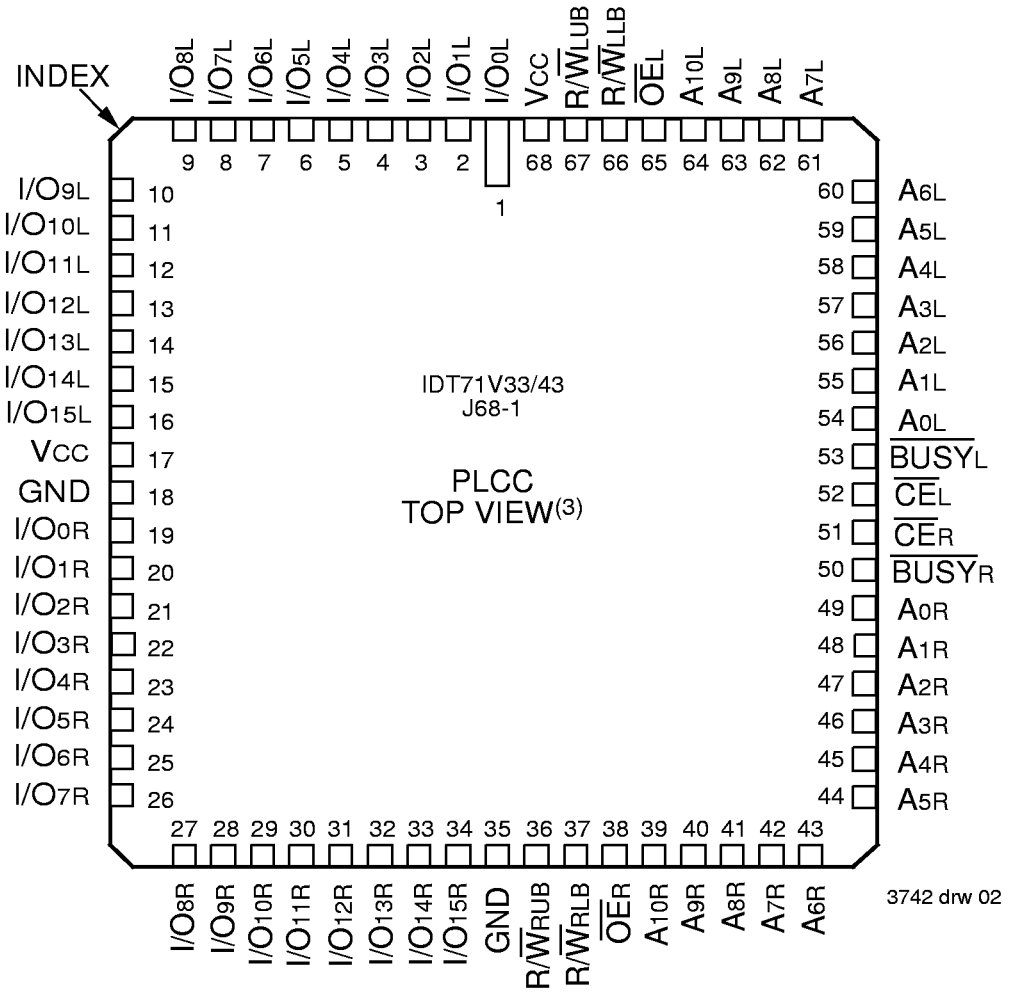
32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very LOW standby power mode.

Fabricated using IDT's CMOS HIGH-performance technology, these devices typically operate on only 750mW of power.

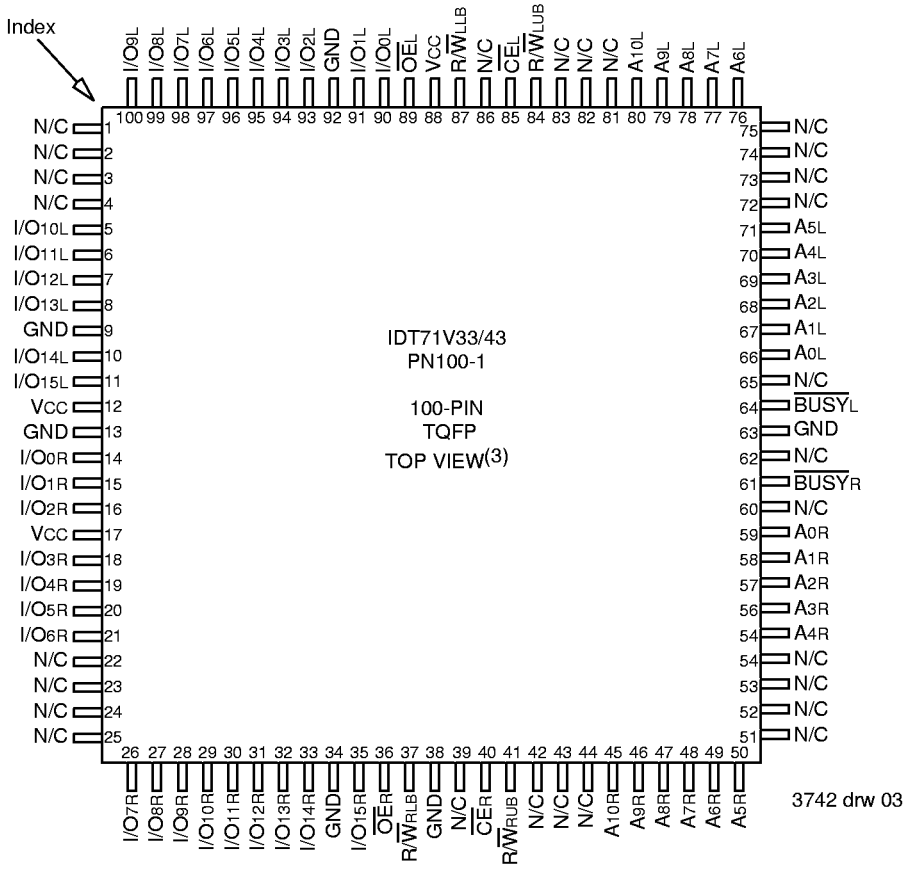
The IDT71V33/71V43 devices have identical pinouts. Each is packed in a 68-pin PLCC and a 100-pin TQFP.

PIN CONFIGURATIONS[1,2]



NOTES:
1. Both VCC pins must be connected to the supply to ensure reliable operation.
2. Both GND pins must be connected to the supply to ensure reliable operation.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS[1,2] (CON'T.)



NOTES:
1. Both VCC pins must be connected to the supply to ensure reliable operation.
2. Both GND pins must be connected to the supply to ensure reliable operation.
3. This text does not indicate orientation of the actual part-marking.

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enables
R/$\overline{W}_{LUB}$	R/$\overline{W}_{RUB}$	Upper Byte Read/Write Enable
R/$\overline{W}_{LLB}$	R/$\overline{W}_{RLB}$	Lower Byte Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{10L}	A_{0R} - A_{10R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground

3742 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3742 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V.

CAPACITANCE(1)

(T_A = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	11	pF

3742 tbl 03

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

MAXIMUM OPERATING TEMPERATURE AND SUPPLY VOLTAGE(1,2)

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

3742 tbl 04

NOTES:
1. This is the parameter T_A.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Volltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3(2)	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

3742 tbl 05

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 10ns
2. V_{TERM} must not exceed V_{CC} +0.3V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	71V33S 71V43S		71V33L 71V43L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3742 tbl 06

NOTE:
1. At Vcc ≤ 2.0V, input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2,6] (V_{CC} = 3.0V ± 0.3V)

Symbol	Parameter	Test Condition	Version		71V33X25 71V43X25 Typ.[1]	71V33X25 71V43X25 Max.	71V33X35 71V43X35 Typ.[1]	71V33X35 71V43X35 Max.	71V33X55 71V43X55 Typ.[1]	71V33X55 71V43X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open f = f_{MAX}[3]	COM'L	S	165	200	160	195	150	185	mA
				L	150	180	140	165	140	170	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} f = f_{MAX}[3]	COM'L	S	16	50	16	45	15	45	mA
				L	16	45	16	40	15	40	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f=f_{MAX}[3]	COM'L	S	90	130	80	120	80	120	mA
				L	65	110	65	105	65	105	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ > V_{CC} - 0.2V V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V, f = 0[4]	COM'L	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	3	0.2	3	0.2	3	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ < 0.2V and $\overline{CE}_{"B"}$ > V_{CC} - 0.2V[5] V_{IN} > V_{CC} - 0.2V or V_{IN} < 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L	S	90	125	80	110	80	110	mA
				L	80	110	65	100	65	100	
			IND	S	—	—	—	—	—	—	
				L	—	—	—	—	—	—	

3742 tbl 07

NOTES:
1. V_{CC} = 3.3V, T_A = +25°C for Typ., and are not production tested. I_{CCDC} = 120mA (typ.)
2. "X" in part numbers indicates power rating (S or L)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2 and 3

3742 tbl 09

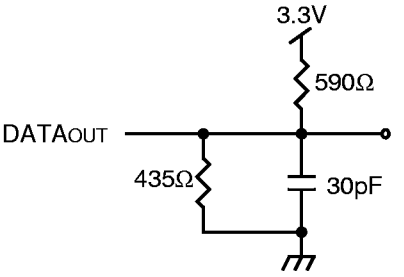


Figure 1. AC Output Test Load

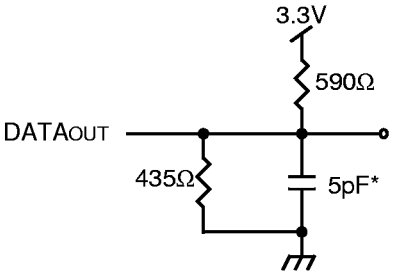


Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
*Including scope and jig

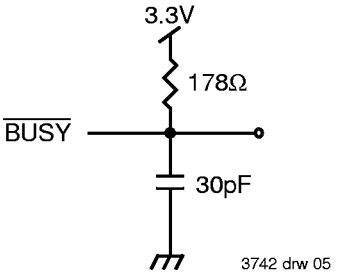


Figure 3. BUSY AC Output Load
(IDT71V33 only)

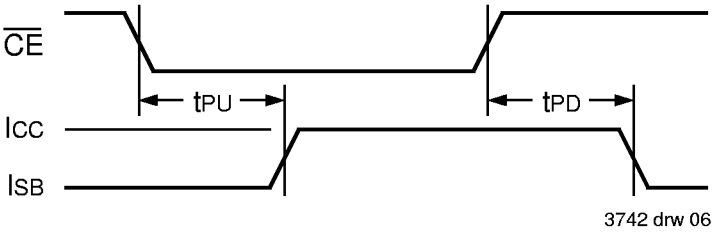
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[3,4]

Symbol	Parameter	71V33X25 71V43X25 Com'l Only		71V33X35 71V43X35 Com'l Only		71V33X55 71V43X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	ns
tLZ	Output Low-Z Time[1,2]	0	—	0	—	5	—	ns
tHZ	Output High-Z Time[1,2]	—	15	—	20	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns

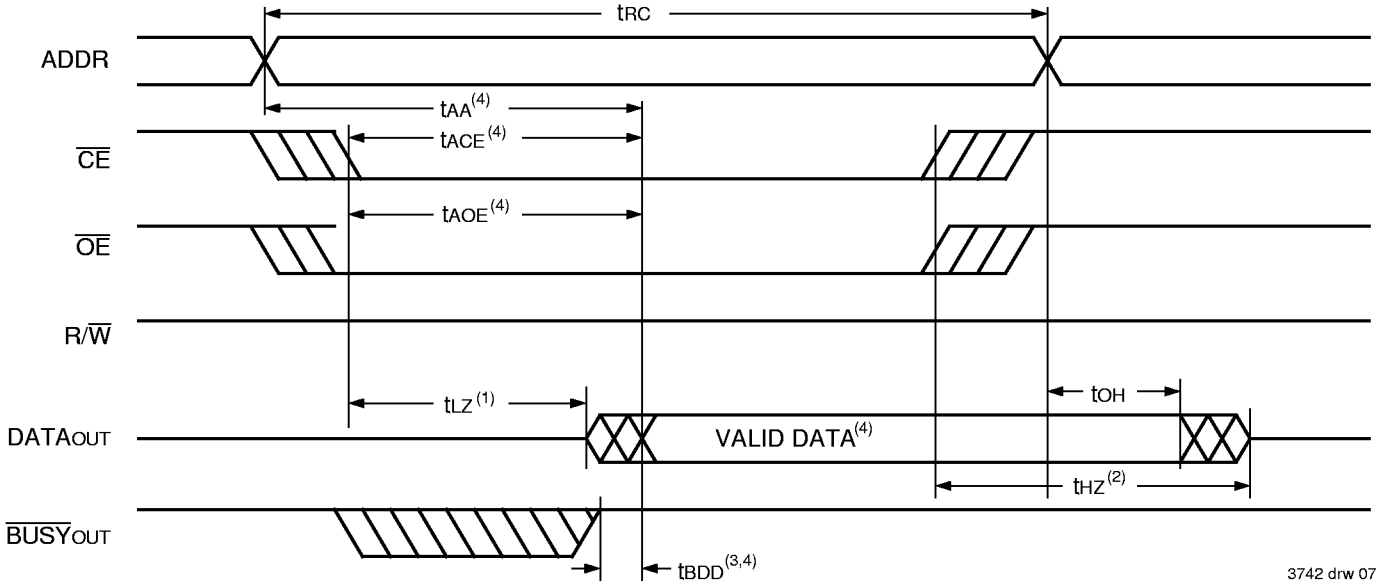
3742 tbl 10

NOTES:
1. Transition is measured ±200mV from Low or High-impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. "X" in part number indicates power rating (S or L).
4. Industrial temperature: for specific speeds, packages and powers contact your sales office.

TIMING OF POWER-UP POWER-DOWN



WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, OE or CE.
2. Timing depends on which signal is de-asserted first, OE or CE.
3. tBDD delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, BUSY has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, tAOE, tACE, tAA, or tBDD.
5. R/W = VIH, and the address is valid prior to or coincidental with CE transition LOW.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[10,11]

Symbol	Parameter	71V33X25 71V43X25 Com'l Only		71V33X35 71V43X35 Com'l Only		71V33X55 71V43X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time[3]	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	25	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	25	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	20	—	20	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	5	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	20	—	20	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	5	—	ns

3742 tbl 11

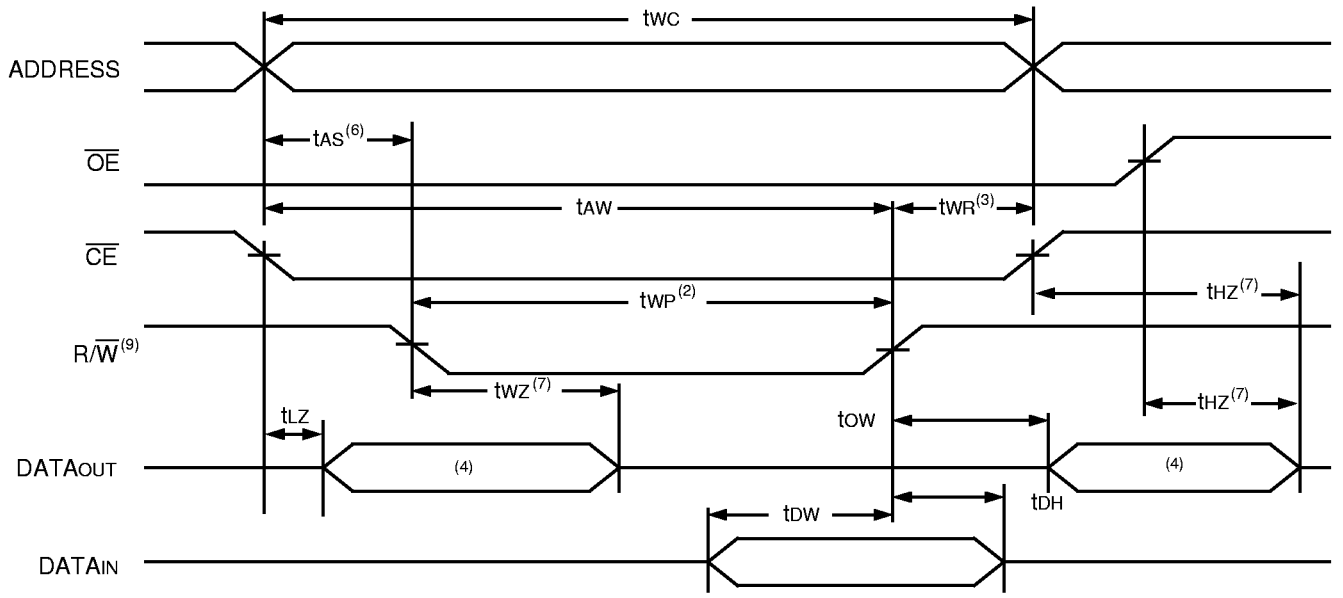
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[10,11]

Symbol	Parameter	71V33X25 71V43X25 Com'l Only		71V33X35 71V43X35 Com'l Only		71V33X55 71V43X55 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (For MASTER IDT 71V33)								
t_{BAA}	BUSY Access Time from Address	—	20	—	30	—	40	ns
t_{BDA}	BUSY Disable Time from Address	—	20	—	30	—	40	ns
t_{BAC}	BUSY Access Time from Chip Enable	—	20	—	25	—	35	ns
t_{BDC}	BUSY Disable Time from Chip Enable	—	20	—	25	—	30	ns
t_{WDD}	Write Pulse to Data Delay[5]		50		60		80	
t_{DDD}	Write Data Valid to Read Data Delay[5]		35		45		65	
t_{BDD}	BUSY Disable to Valid Data[6]	—	30	—	35	—	40	ns
t_{APS}	Arbitration Priority Set-up Time[7]	5	—	5	—	5	—	ns
t_{WH}	Write Hold After BUSY[9]	20	—	25	—	30	—	ns
BUSY INPUT TIMING (For SLAVE IDT 71V43)								
t_{WB}	BUSY Input to Write[8]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After BUSY[9]	20	—	25	—	30	—	ns
t_{WDD}	Write Pulse to Data Delay[5]	—	50	—	60	—	80	ns
t_{DDD}	Write Data Valid to Read Data Delay[5]	—	35	—	45	—	65	ns

3742 tbl 12

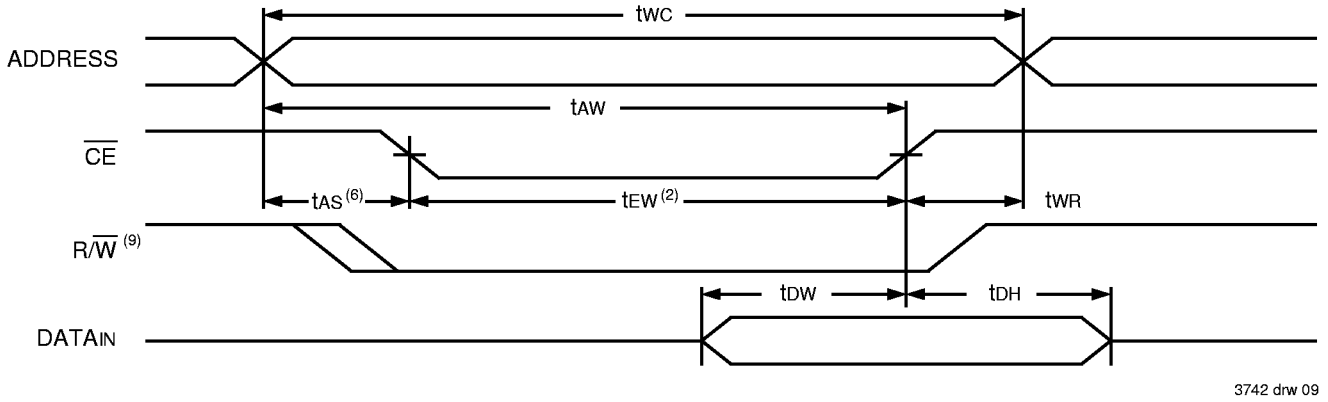
NOTES:
1. Transition is measured ±200mV from Low- or High-impedence voltage from the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$, since R/$\overline{W}$ = V_{IL} must occur after t_{BAA}.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will very over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
6. t_{BDD} is calculated parameter and is greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
7. To ensure that the earlier of the two ports wins.
8. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
9. To ensure that a write cycle is completed on port "B" after contention on port "A".
10. "X" in part number indicates power rating (S or L).
11. Industrial temperature: for specific speeds, packages and powers contact your sales office.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/W CONTROLLED TIMING)(1,5,8)



3742 drw 08

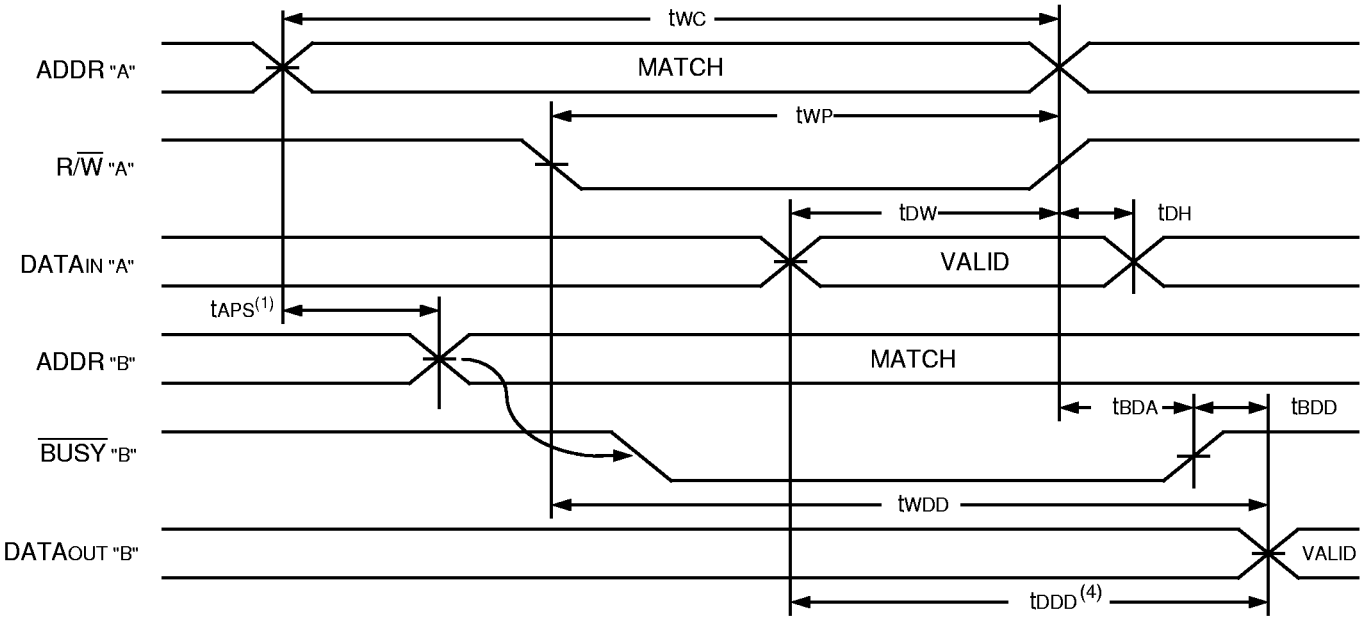
WRITE CYCLE NO. 2 (CE CONTROLLED TIMING)(1,5)



3742 drw 09

NOTES:
1. R/W or CE must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a CE = VIL and a R/W = VIL.
3. tWR is measured from the earlier of CE or R/W going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (CE or R/W) is asserted last.
7. Timing depends on which enable signal is de-asserted first, CE or OE.
8. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. R/W for either upper or lower byte.

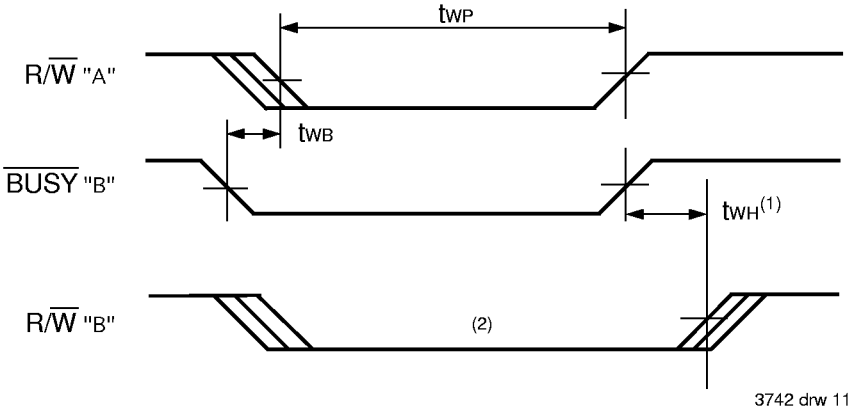
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND BUSY (2,3,4)



3742 drw 10

NOTES:
1. To ensure that the earlier of the two ports wins, tAPS is ignored for Slave (IDT7143).
2. CEL = CER = VIL
3. OE = VIL for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

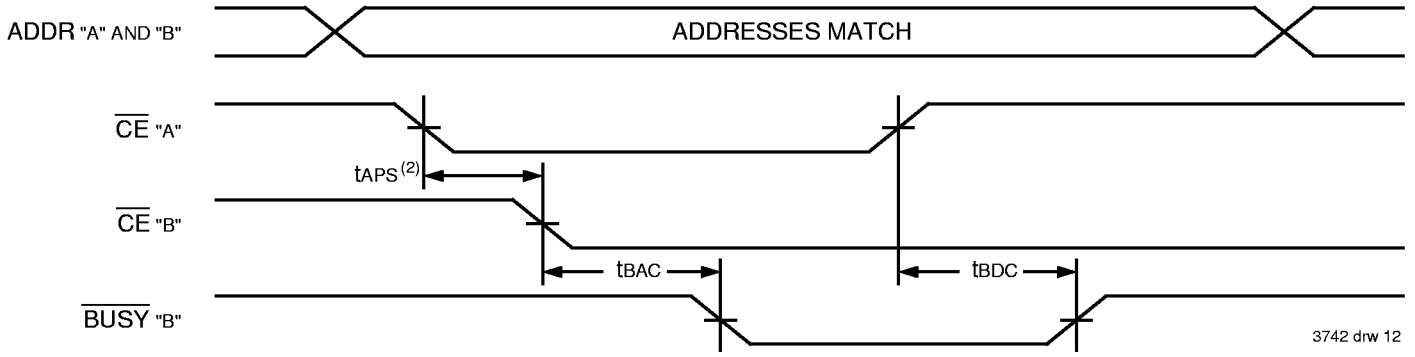
TIMING WAVEFORM OF WRITE WITH BUSY(3)



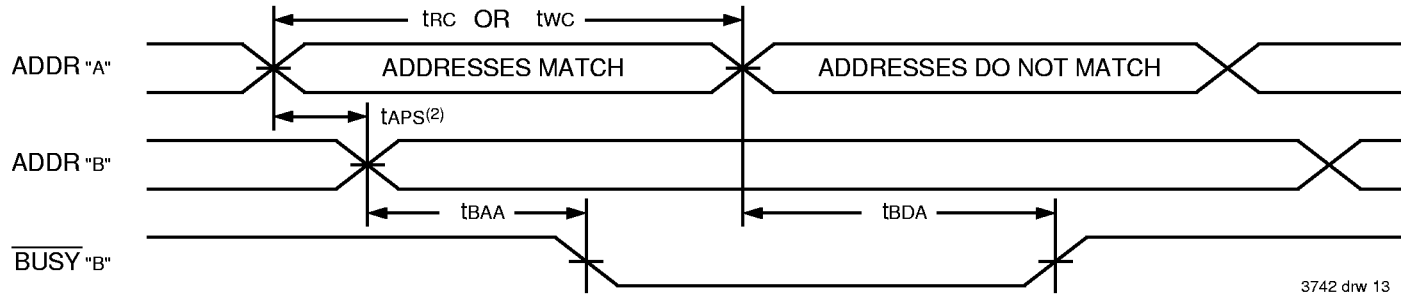
3742 drw 11

NOTES:
1. tWH must be met for both BUSY input (IDT71V43, SLAVE) and output (IDT71V33, MASTER).
2. BUSY is asserted on port "B" blocking R/W "B", until BUSY "B" goes HIGH.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY CE TIMING(1)



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESSES(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (IDT71V33 only).

FUNCTIONAL DESCRIPTION:

The IDT71V33/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V33/43 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table I.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by using the IDT71V43 (SLAVE). In the IDT71V43, the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW. The $\overline{BUSY}$ outputs on the IDT71V33 RAM are open drain and require pull-up resistors.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT71V33/43 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT71V33 RAM the $\overline{BUSY}$ pin is an output and on the IDT71V43 RAM, the $\overline{BUSY}$ pin is an input (see Figure 4).

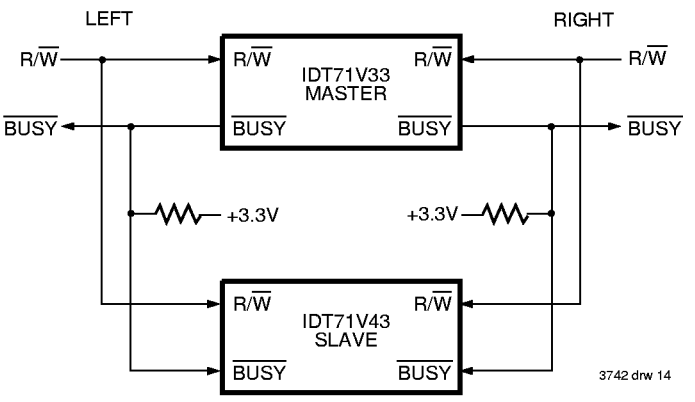


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT71V33 (MASTER) and the IDT71V43 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now $\overline{BUSY}$ and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLE I – NON-CONTENTION READ/WRITE CONTROL(4)

LEFT OR RIGHT PORT(1)						
R/$\overline{W}_{LB}$	R/$\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O0-7	I/O8-15	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH}, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	DATAIN	DATAIN	Data on Lower Byte and Upper Byte Written into Memory(2)
L	H	L	L	DATAIN	DATAOUT	Data on Lower Byte Written into Memory(2), Data in Memory Output on Upper Byte(3)
H	L	L	I	DATAOUT	DATAIN	Data in Memory Output on Lower Byte(3), Data on Upper Byte Written into Memory(2)
L	H	L	H	DATAIN	Z	Data on Lower Byte Written into Memory(2)
H	L	L	H	Z	DATAIN	Data on Upper Byte Written into Memory(2)
H	H	L	L	DATAOUT	DATAOUT	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

3742 tbl 13

NOTES:
1. A_{0L} - $A_{10L} \neq A_{0R}$ - A_{10R}
2. If $\overline{BUSY}$ = V_{IL}, data is not written.
3. If $\overline{BUSY}$ = V_{IL}, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care, "Z" = High Impedance, "LB" = Lower Byte, "UB" = Upper Byte

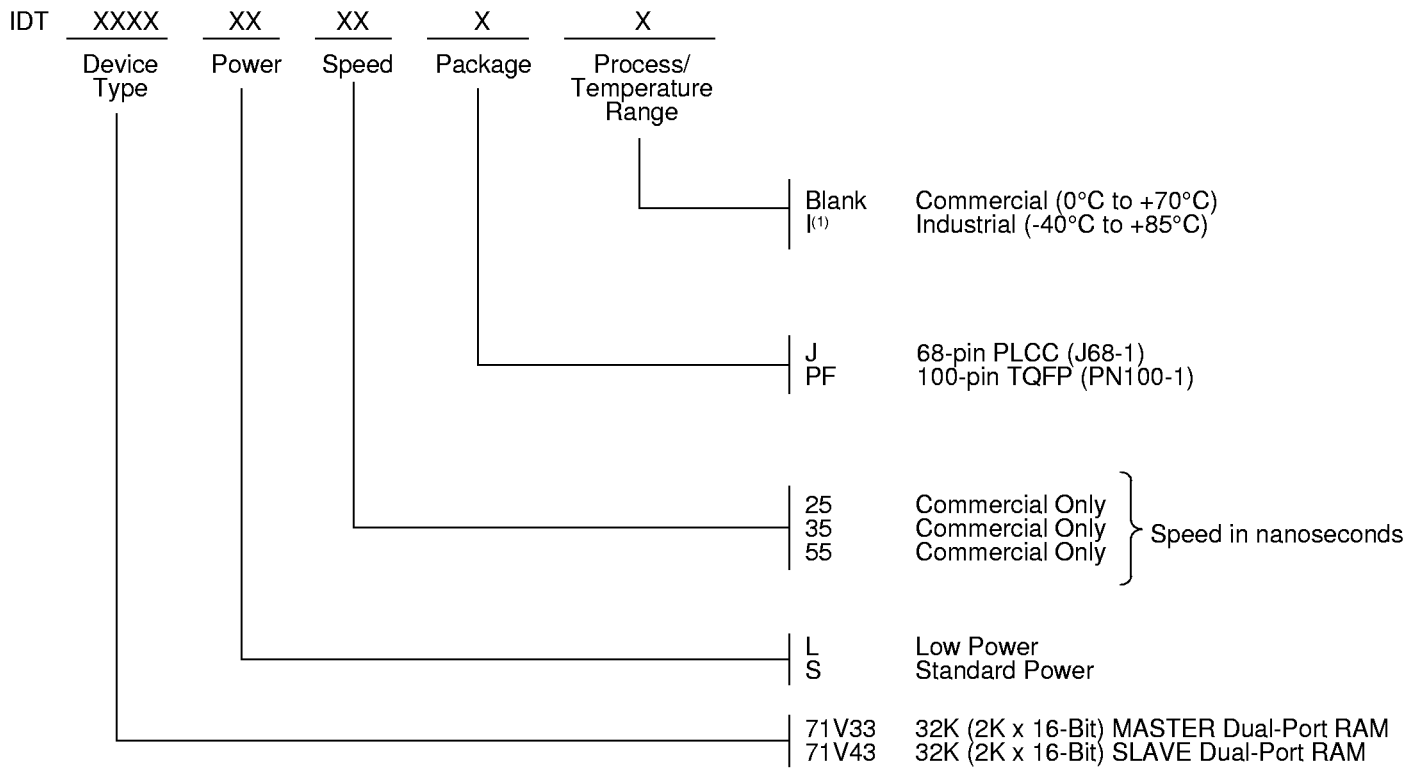
TRUTH TABLE I I — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{OL}-A_{10L} A_{OR}-A_{10R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3742 tbl 14

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs on the IDT71V33 (MASTER). Both are inputs on the IDT71V43 (SLAVE). On Slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

ORDERING INFORMATION

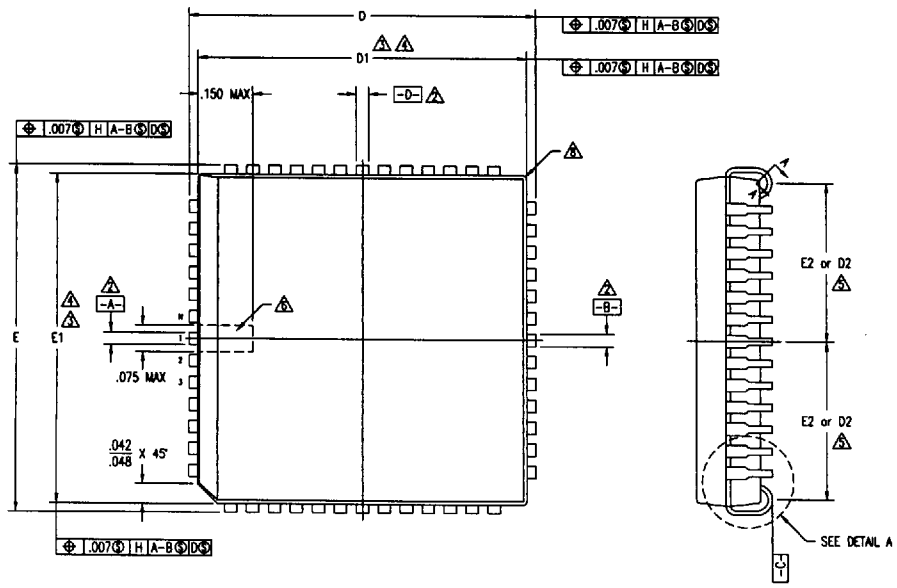


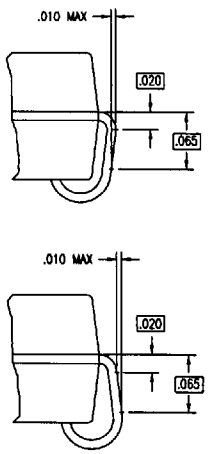
3742 drw 15

NOTE:
1. Industrial temperature range is available.
   For specific speeds, packages and powers contact your sales office.

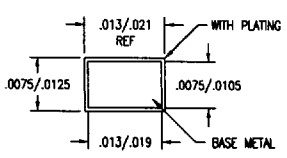
PLCC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	





DETAIL A ⚠



SECTION A-A ⚠

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL ANGULAR XX± ± XXX± XXXX±		
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/88	
CHECKED		SIZE C DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.165	.172	.180	
A1	.095	.105	.115	
A2	.062	–	.083	
D	.485	.490	.495	
D1	.450	.453	.456	3,4
D2	.195	.205	.215	5
E	.485	.490	.495	
E1	.450	.453	.456	3,4
E2	.191	.205	.219	5
N	28			

DWG #	J44-1			
JEDEC VARIATION AC				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.685	.690	.695		
.650	.653	.656	3,4	
.295	.305	.315	5	
.685	.690	.695		
.650	.653	.656	3,4	
.291	.305	.319	5	
44				

DWG #	J52-1			
JEDEC VARIATION AD				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.785	.790	.795		
.750	.753	.756	3,4	
.345	.355	.365	5	
.785	.790	.795		
.750	.753	.756	3,4	
.341	.355	.369	5	
52				

DWG #	J68-1			
JEDEC VARIATION AE				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.985	.990	.995		
.950	.953	.956	3,4	
.445	.455	.465	5	
.985	.990	.995		
.950	.953	.956	3,4	
.441	.455	.469	5	
68				

DWG #	J84-1			
JEDEC VARIATION AF				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.059	–	.080		
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.545	.555	.565	5	
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.541	.555	.569	5	
84				

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	06/15/95
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

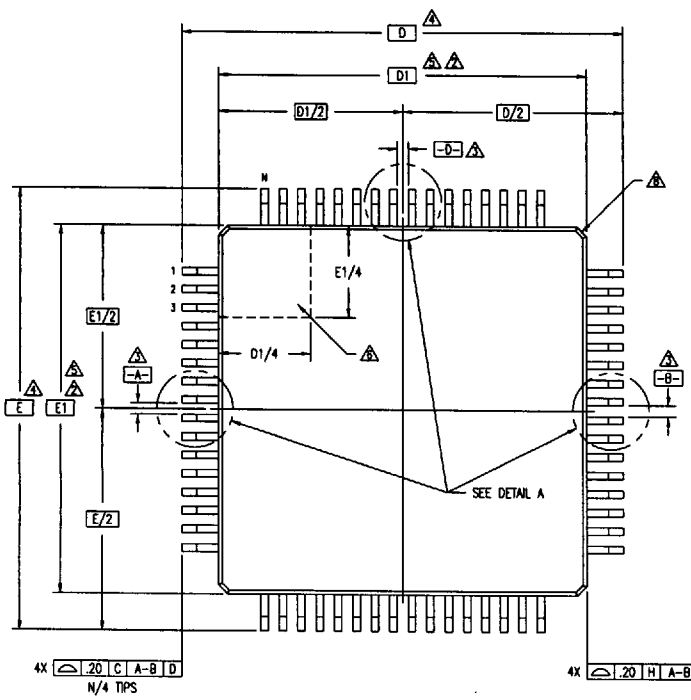
SIZE	DRAWING No.	REV
C	PSC-4008	06

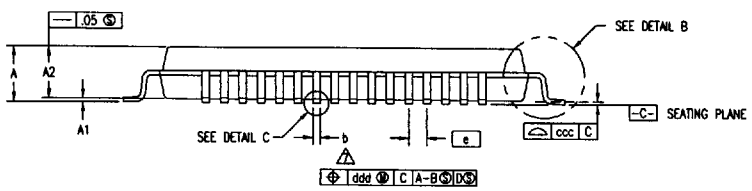
DO NOT SCALE DRAWING

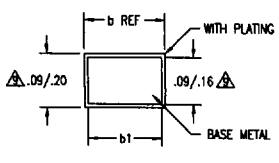
PACKAGE DIAGRAM OUTLINES

TQFP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	

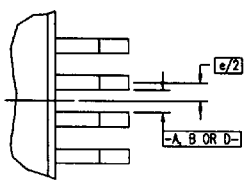




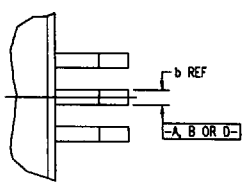


DETAIL C

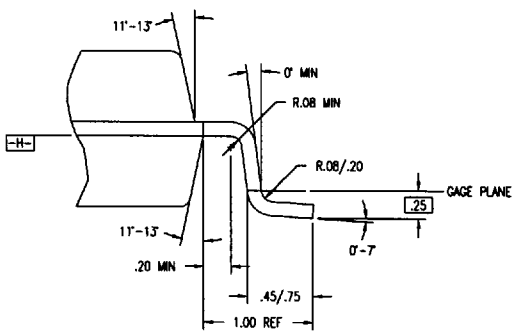
EVEN LEAD SIDES



ODD LEAD SIDES



DETAIL A



DETAIL B

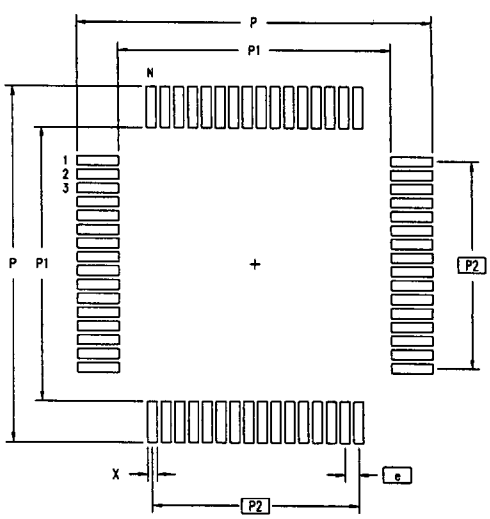
TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS / DRAWN AA 03/12/92 / CHECKED	TITLE: PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM	
	SIZE C	DRAWING No. PSC-4036 REV 03
	DO NOT SCALE DRAWING	

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	03/12/92
CHECKED	

TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE C | DRAWING No. PSC-4036 | REV 03

DO NOT SCALE DRAWING