MOTOROLA

MC2917A

QUAD THREE-STATE BUS TRANSCEIVER WITH INTERFACE LOGIC

The MC2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the Bus inputs) are one LS unit load. The three-state bus output can sink up to 48 mA at 0.5 V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is High, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_n data into this driver register on the Low-to-High transition.

Data from the A input is inverted at the Bus output. Likewise, the data at the Bus input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is Low, the latch is open and the receiver outputs will follow the bus inputs (Bus data inverted and $\overline{OE}$ Low). When the $\overline{RLE}$ input is High, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is High, the receiver outputs are in the high-impedance state.

The MC2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is Low (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is High, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated; and, if the driver is in the high-impedance state, the Bus parity is checked.

FEATURES

- Quad High speed LSI Bus Transceiver
- Three-state Bus Driver
- D-type Register on Driver
- Bus Driver Output Can Sink 48 MA at 0.5 V Max
- Internal Odd 4-bit Parity Checker/Generator
- Receiver Has Output Latch for Pipeline Operation
- Three-state Receiver Outputs Sink 12 mA
- Advanced Low-power Schottky Processing
- 100% Reliability Assurance Testing in Compliance With MIL-STD-883
- 3.5 V Minimum Output High Voltage for Direct Interface to MOS Microprocessors

TTL
QUAD THREE-STATE
BUS TRANSCEIVER
WITH INTERFACE LOGIC

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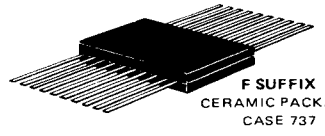
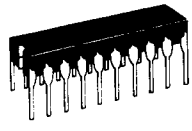
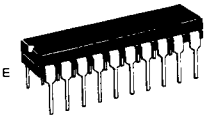


F SUFFIX
CERAMIC PACKAGE
CASE 737

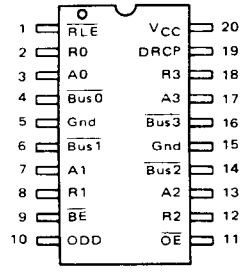


L SUFFIX
CERAMIC PACKAGE
CASE 732

P SUFFIX
PLASTIC PACKAGE
CASE 738



PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	MC2917APC
Hermetic DIP	0°C to +70°C	MC2917ALC
Hermetic DIP	-55°C to +125°C	MC2917ALM
Hermetic Flat Pack	-55°C to +125°C	MC2917AFM

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC}max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs (Except Bus)	30 mA
DC Output Current, into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

MC2917AXC — T_A = 0°C to +70°C, V_{CC} = 5.0 V ±5% (Commercial), Min = 4.75 V, Max = 5.25 V
MC2917AXM — T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10% (Military), Min = 4.5 V, Max = 5.5 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions (Note 1)		Min	Typ	Max	Unit
V_{OL}	Bus Output Low Voltage	V_{CC} = Min	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output High Voltage	V_{CC} = Min	Commercial, I_{OH} = −20 mA	2.4			Volts
			Military, I_{OH} = −15 mA	2.4			
I_O	Bus Leakage Current (High Impedance)	V_{CC} = Max, Bus Enable = 2.4 V	V_O = 0.4 V			−200	µA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{off}	Bus Leakage Current (Power off)	V_O = 4.5 V, V_{CC} = 0 V				100	µA
V_{IH}	Receiver Input High Threshold	Bus Enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input Low Threshold	Bus Enable = 2.4 V	Commercial			0.8	Volts
			Military			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = Max, V_O = 0 V		−50	−120	−225	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

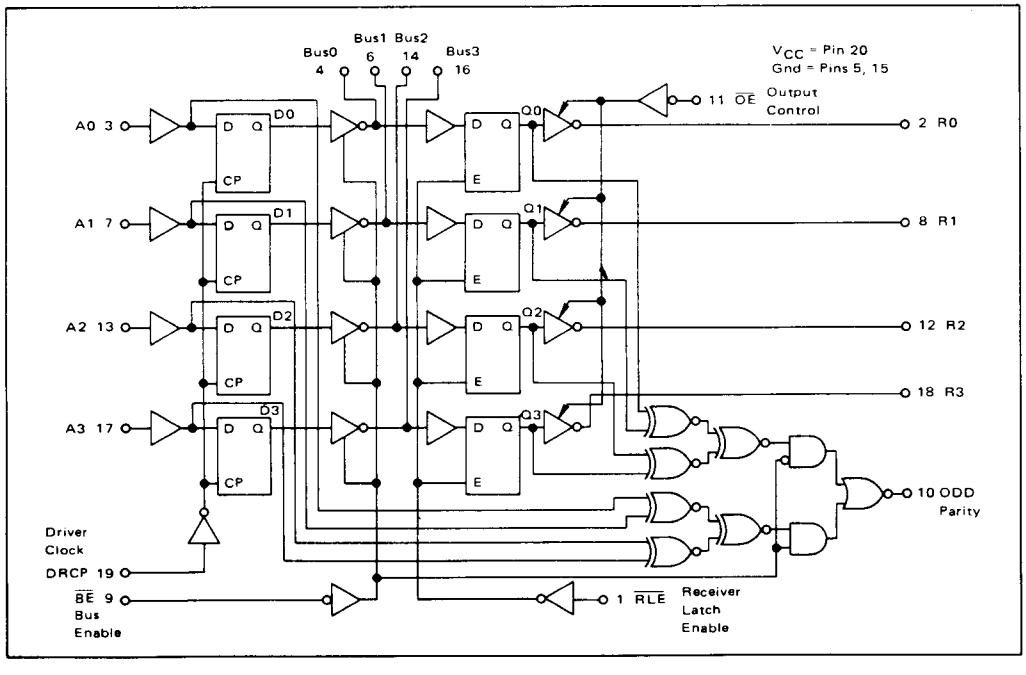
Parameter	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Unit
V_{OH}	Receiver Output High Voltage	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	Military, I_{OH} = −1.0 mA	2.4	3.4		Volts
			Commercial, I_{OH} = −2.6 mA	2.4	3.4		
		V_{CC} = 5.0 V, I_{OH} = −100 µA		3.5			
V_{OH}	Parity Output High Voltage	V_{CC} = Min, I_{OH} = −660 µA, V_{in} = V_{IH} or V_{IL}	Military	2.5	3.4		Volts
			Commercial	2.7	3.4		
V_{OL}	Output Low Voltage (Except Bus)	V_{CC} = Min, V_{in} = V_{IL} or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input High Level (Except Bus)	Guaranteed input logical High for all inputs		2.0			Volts
V_{IL}	Input Low Level (Except Bus)	Guaranteed input logical Low for all inputs	Military			0.7	Volts
			Commercial			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{in} = −18 mA				−1.2	Volts
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{in} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 2.7 V				20	µA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{in} = 7.0 V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = Max	Receiver	−30		−130	mA
			Parity	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = Max			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = Max	V_O = 2.4 V			50	µA
			V_O = 0.4 V			−50	

NOTES: 1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameter	Description	Test Conditions	MC2917AXM			MC2917AXC			Unit
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (Bus) = 50 pF	–	21	36	–	21	32	ns
t_{PLH}		R_L (Bus) = 130 Ω	–	21	36	–	21	32	
t_{ZH},t_{ZL}	Bus Enable ($\overline{BE}$) to Bus		–	13	26	–	13	23	ns
t_{HZ},t_{LZ}			–	13	21	–	13	18	
t_s	A Data Input	C_L = 15 pF	15	–	–	12	–	–	ns
t_h		R_L = 2.0 k	8.0	–	–	6.0	–	–	
t_{PW}	Clock Pulse Width (High)		20	–	–	17	–	–	ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)		–	18	33	–	18	30	ns
t_{PHL}			–	18	30	–	18	27	
t_{PLH}	Latch Enable to Receiver Output		–	21	33	–	21	30	ns
t_{PHL}			–	21	30	–	21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15	–	–	13	–	–	ns
t_h			6.0	–	–	4.0	–	–	
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)		–	32	46	–	32	42	ns
t_{PHL}			–	26	40	–	26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)		–	21	36	–	21	32	ns
t_{PHL}			–	21	36	–	21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output		–	21	36	–	21	32	ns
t_{PHL}			–	21	36	–	21	32	
t_{ZH},t_{ZL}	Output Control to Output		–	14	26	–	14	23	ns
t_{HZ},t_{LZ}		C_L = 5 pF, R_L = 2.0 k	–	14	26	–	14	23	

LOGIC DIAGRAM



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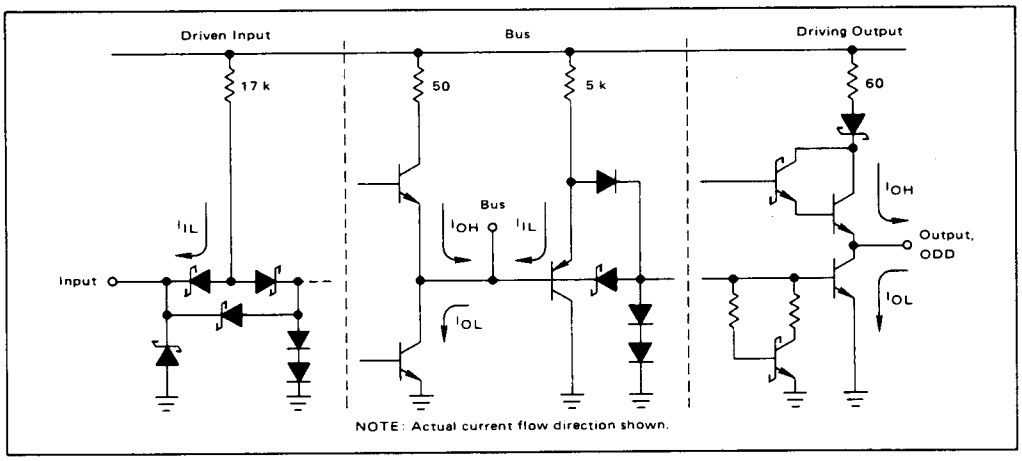
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



FUNCTION TABLE

		Inputs			Internal to Device		Bus	Output	
A_n	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_n	Q_n	Bus_n	R_n	Function
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = High Z = High impedance X = Don't care
L = Low NC = No change ↑ = Low-to-high transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	Odd Parity Output
L	ODD = A0 ⊕ A1 ⊕ A2 ⊕ A3
H	ODD = Q0 ⊕ Q1 ⊕ Q2 ⊕ Q3

DEFINITIONS OF FUNCTIONAL TERMS

DRCP — Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ — Bus Enable. When the Bus Enable is Low, the four drivers are in the high impedance state.

Bus0, Bus1, Bus2, Bus3 — The four driver outputs and receiver inputs (data is inverted).

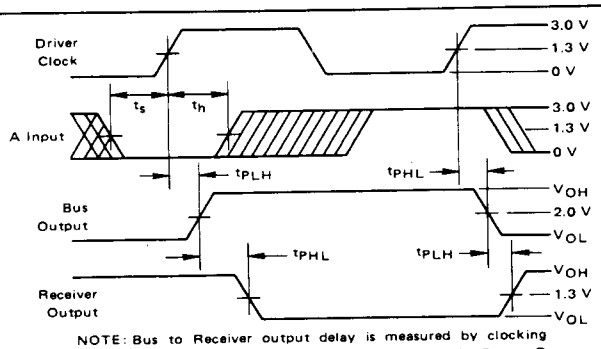
R0, R1, R2, R3 — The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ — Receiver Latch Enable. When $\overline{RLE}$ is Low, data on the Bus inputs is passed through the receiver latches. When $\overline{RLE}$ is High, the receiver latches are closed and will retain the data independent of all other inputs.

ODD — Odd parity output generates parity with the driver enabled. Checks parity with the driver in the high impedance state.

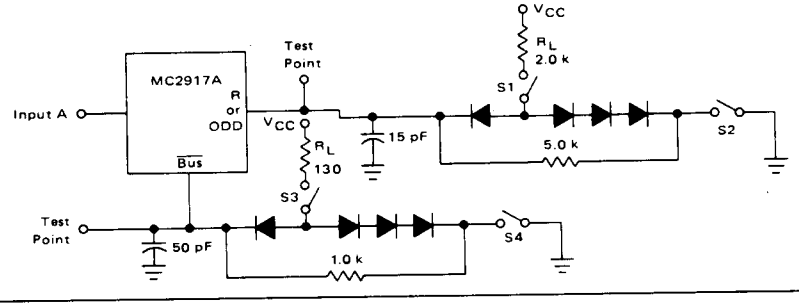
$\overline{OE}$ — Output Enable. When the $\overline{OE}$ input is High, the four three-state receiver outputs are in the high impedance state.

SWITCHING WAVEFORMS

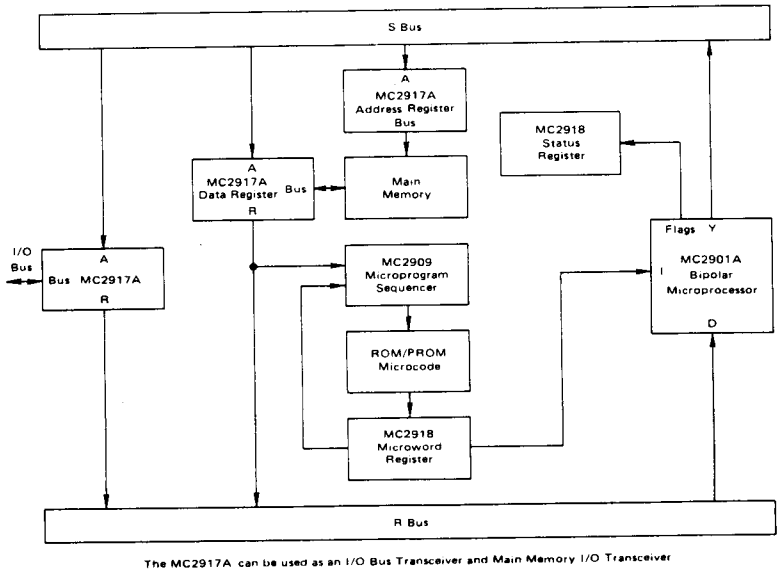


NOTE: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the Bus to R combinatorial delay.

SWITCHING TEST CIRCUIT



APPLICATIONS



The MC2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high speed microprocessor systems.

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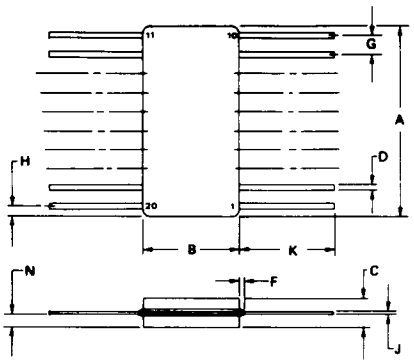
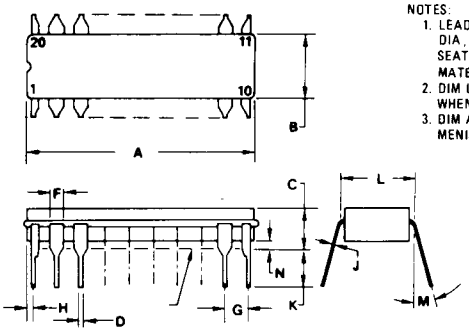
PACKAGE DIMENSIONS



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

CASE 737

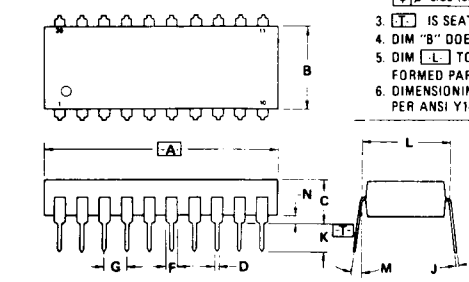
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	13.08	–	0.515
B	5.84	6.60	0.230	0.260
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

CASE 732

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030



NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOL FOR LEADS.
   ⌖ Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. [T] IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM [L] TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

CASE 738

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.19	0.155	0.165
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040