MOTOROLA

Military 54LS163A

4-Bit Binary Counter (with Synchronous Clear)

ELECTRICALLY TESTED PER:
MIL-M-38510/31512

The 'LS163A is a high-speed 4-bit synchronous counter. It is edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The 'LS163A can count modulo 16 (binary).

The 'LS163A has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

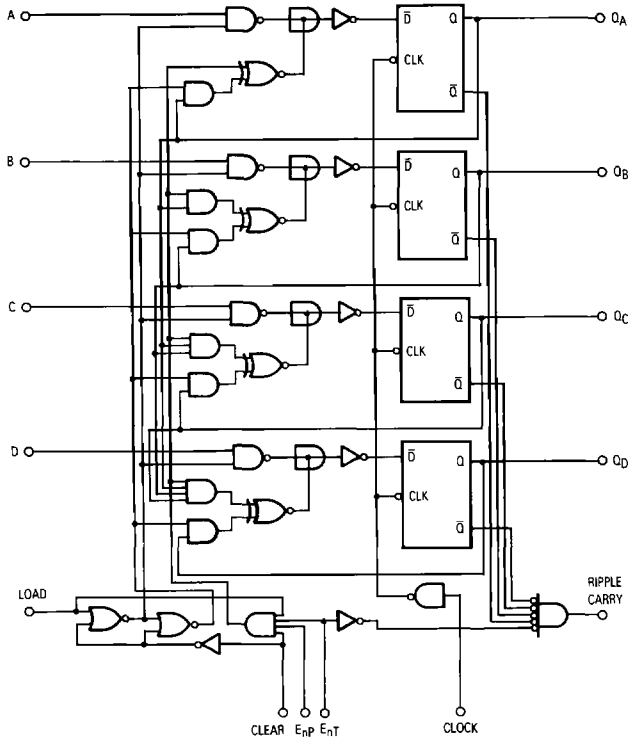
- Synchronous Counting and Loading
- Two Count Enable Inputs For High-Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Typical Count Rate of 35 MHz

AVAILABLE AS:

1) JAN: JM38510/31512BXA
2) SMD: 7603401
3) 883C: 54LS163A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
CR	1	1	2	GND
CP	2	2	3	V_{CC}
A	3	3	4	V_{CC}
B	4	4	5	V_{CC}
C	5	5	7	V_{CC}
D	6	6	8	V_{CC}
E_{nP}	7	7	9	V_{CC}
GND	8	8	10	GND
Ld	9	9	12	V_{CC}
E_{nT}	10	10	13	V_{CC}
Q_D	11	11	14	V_{CC}
Q_C	12	12	15	V_{CC}
Q_B	13	13	17	V_{CC}
Q_A	14	14	18	V_{CC}
RC	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

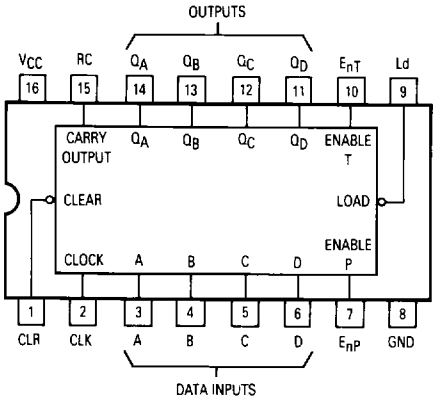
MODE SELECT TABLE

CR	Ld	E_{nT}	E_{nP}	Action on the Rising Clock Edge (_┌)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (D_n-Q_n)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

6

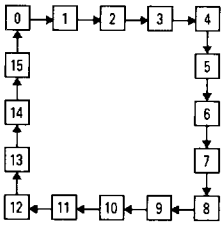
CONNECTION DIAGRAM



Pin Names		Loading (Note b)	
		HIGH	LOW
Load	Parallel Enable (Active LOW)	1.0 U.L.	0.5 U.L.
A–D	Parallel Inputs (Data Inputs)	0.5 U.L.	0.25 U.L.
E_{nP}	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
E_{nT}	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
CR	Master Reset (Active LOW) Input	1.0 U.L.	0.25 U.L.
Q_A–Q_D	Parallel Outputs (Note b)	10 U.L.	5(2.5) U.L.
RC	Terminal Count (Ripple Carry) Output (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. One TTL Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = $E_{nP} \cdot E_{nT} \cdot Ld$
RC for 'LS163A = $E_{nT} \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$
Preset = $\overline{Ld} \cdot CP$ + (rising clock edge)
Reset = $\overline{CR} \cdot CP$ + (rising clock edge)

FUNCTIONAL DESCRIPTION

The 'LS163A is a 4-bit synchronous counter with a synchronous Parallel Enable (Load) feature. The counter consists of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs, Parallel Enable (Ld), Count Enable Parallel (E_{nP}) and Count Enable Trickle (E_{nT}), select the mode of operation as shown in the table below. The Count Mode is enabled when the E_{nP}, E_{nT}, and $\overline{Ld}$ inputs are HIGH. When the $\overline{Ld}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the E_{nP} or E_{nT} can be used to inhibit the count sequence. With the $\overline{Ld}$ held HIGH, a LOW on either the E_{nP} or E_{nT} inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs ($E_{nP} \cdot E_{nT}$) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

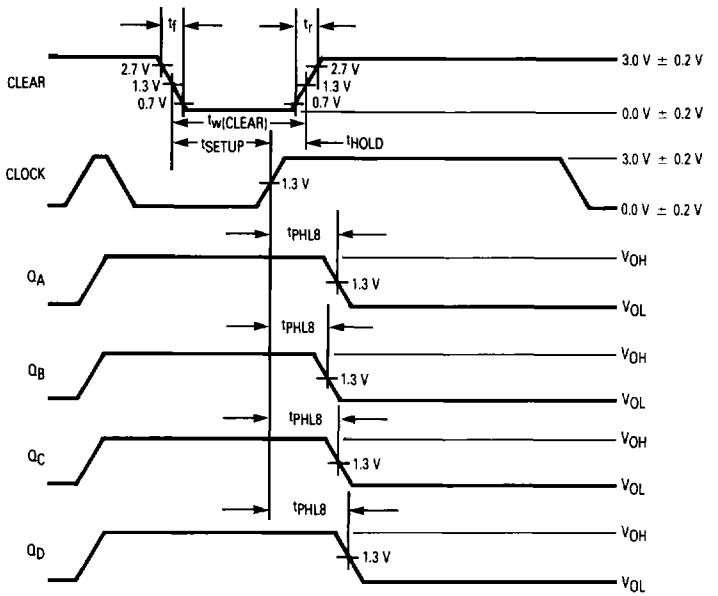
The Terminal Count (RC) output is HIGH when the Counter Enable Trickle (E_{nT}) input is HIGH while the counter is in its maximum count state (HLLH for BCD counters, HHHH for Binary counters). Note that RC is fully decoded and will, therefore, be HIGH only for one count state.

The 'LS163A counts modulo 16 following a binary sequence. It generates a RC when the E_{nT} input is HIGH while the counter is in the state 15 (HHHH). From this state they increment to state 0 (LLLL).

The active LOW Synchronous Reset ($\overline{CR}$) input of the 'LS163A acts as an edge-triggered control input, overriding E_{nT}, E_{nP} and $\overline{Ld}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

6

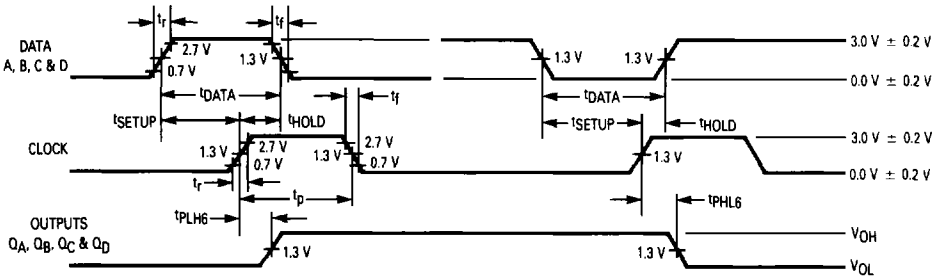
VOLTAGE WAVEFORM 1



NOTE:
The Clear pulse generator has the following characteristics:
V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, $t_{w(Clear)}$ = 25 ns,
t_{SETUP} = 25 ns, t_{HOLD} = 0 ns.

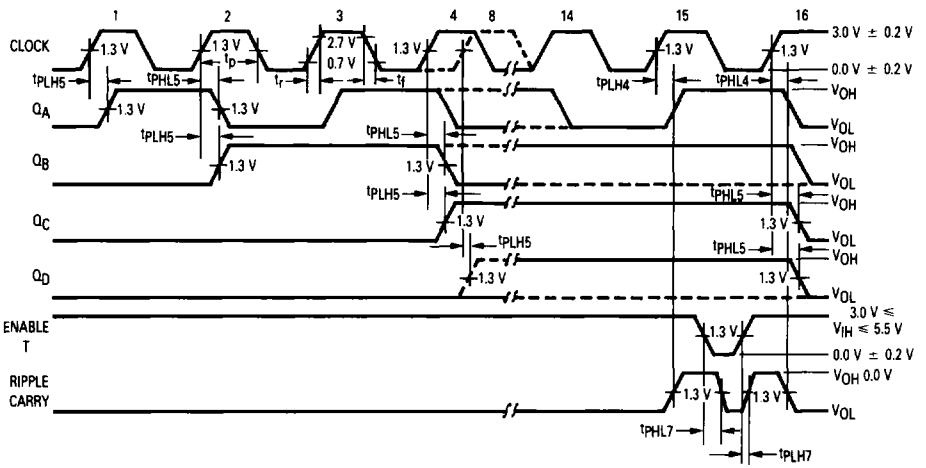
6

VOLTAGE WAVEFORM 2

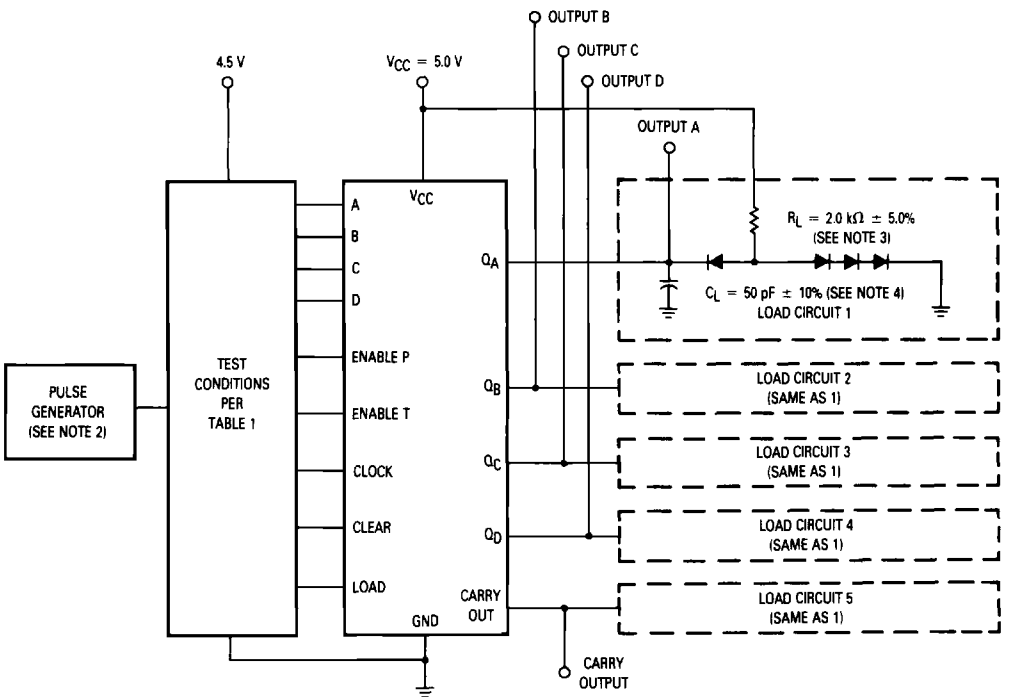


NOTE:
The data pulse generator has the following characteristics:
V_{gen} = 3.0 V, $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_{DATA} = 30 ns, t_{SETUP} = 20 ns,
t_{HOLD} = 10 ns.

VOLTAGE WAVEFORM 3



TEST CIRCUIT

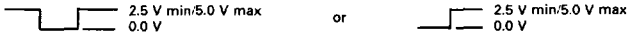


Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, CR = 4.5 V, E_{nP} = open, CP = (See Note 7), V_{IH} = 2.0 V, E_{nT} = 2.0 V, Ld = GND.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, Ld = GND, CP = (See Note 7), CR = 4.5 V, E_{nP} = open, E_{nT} = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, (other inputs are open).
I_{IH}	Logical "1" Input Current		40		40		40	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (other inputs are open).
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (other inputs are open), Ld & E_{nT} = GND or open.
I_{IHH}	Logical "1" Input Current		200		200		200	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (other inputs are open), Ld & $E_{nP/T}$ = GND or 5.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (other inputs are open), Ld = GND, V_{OUT} = GND, CP = (See Note 7), CR = 4.5 V, $E_{nT/P}$ = open.
I_{IL}	Logical "0" Input Current	−300	−760	−300	−760	−300	−760	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open), Ld & $E_{nP/T}$ = 4.5 V or 0.4 V.
I_{ILL}	Logical "0" Input Current	−120	−360	−120	−360	−120	−360	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open).
I_{IL}	Logical "0" Input Current	−160	−400	−160	−400	−160	−400	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V (other inputs are open), Ld = GND.
I_{ILL}	Logical "0" Input Current	−150	−380	−150	−380	−150	−380	μA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, Ld & E_{nT} = 4.5 V, other inputs are open.
I_{CCH}	Power Supply Current Off		31		31		31	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), Ld = 5.5 V or GND.
I_{CCL}	Power Supply Current Off		32		32		32	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CP = GND or 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

6

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL4} t_{PHL4}	Propagation Delay /Data-Output High-Low	3.0	40 35	3.0	56 44	3.0	56 44	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay /Data-Output Low-High	3.0	40 35	3.0	56 44	3.0	56 44	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output High-Low	3.0	32 27	3.0	45 34	3.0	45 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output Low-High	3.0	29 24	3.0	41 31	3.0	41 31	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL6} t_{PHL6}	Propagation Delay /Data-Output High-Low	3.0	32 14	3.0	48 18	3.0	48 18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH6} t_{PLH6}	Propagation Delay /Data-Output Low-High	3.0	29 14	3.0	42 18	3.0	42 18	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL7}	Propagation Delay /Data-Output High-Low	3.0	19	3.0	28	3.0	28	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PLH7}	Propagation Delay /Data-Output Low-High	3.0	19	3.0	28	3.0	28	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_{PHL8} t_{PHL8}	Propagation Delay /Data-Output High-Low	3.0	33 28	3.0	46 35	3.0	46 35	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX} f_{MAX}	Maximum Clock Frequency	22 25		22		22		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTES:
1. Voltage measurements are made with respect to ground terminal.
2. The pulse generator has the following characteristics:
   V_{GEN} = 3.0 V, t_r = 6.0 ns, t_f = 6.0 ns, t_p = 0.5 μs, PRR ≤ 1.0 MHz, Z_{OUT} ≈ 50 Ω.
3. All diodes are 1N3064 or equivalent.
4. C_L = 50 pF ± 10%, including scope probe and jig capacitance.
5. f_{MAX}: t_r = t_f ≤ 6.0 ns.
6. The limits specified for C_L = 15 pF are guaranteed but not tested.
7. Apply one pulse prior to measurement as follows:



6