Obsolete Device

TC911A/TC911B

Monolithic Auto-Zeroed Operational Amplifiers

Features

- First Monolithic Chopper-Stabilized Amplifier with On-Chip Nulling Capacitors
- Low Offset Voltage: 5µV
- Low Offset Voltage Drift: 0.05µV/°C
- Low Supply Current: 350µA
- High Common-Mode Rejection: 116dB
- Single Supply Operation: 4.5V to 16V
- High Slew Rate: 2.5V/µsec
- Wide Bandwidth: 1.5MHz
- High Open-Loop Voltage Gain: 120dB
- Low Input Noise Voltage: 0.65µV_{P-P} (0.1Hz to 1Hz)
- Pin Compatible With ICL7650
- Lower System Parts Count

Applications

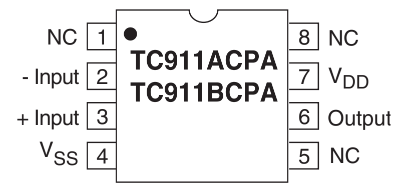
- Instrumentation
- Portable/Battery Powered
- Embedded Control
- Temperature Sensor Amplifier
- Strain Gage Amplifier

Device Selection Table

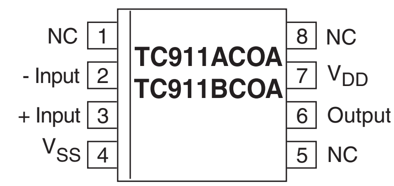
Part Number	Package	Temperature Range	Offset Voltage
TC911ACOA	8-Pin SOIC	0°C to +70°C	15µV
TC911ACPA	8-Pin PDIP	0°C to +70°C	15µV
TC911BCOA	8-Pin SOIC	0°C to +70°C	30µV
TC911BCPA	8-Pin PDIP	0°C to +70°C	30µV

Package Type

8-Pin PDIP



8-Pin SOIC



NC = No Internal Connection

General Description

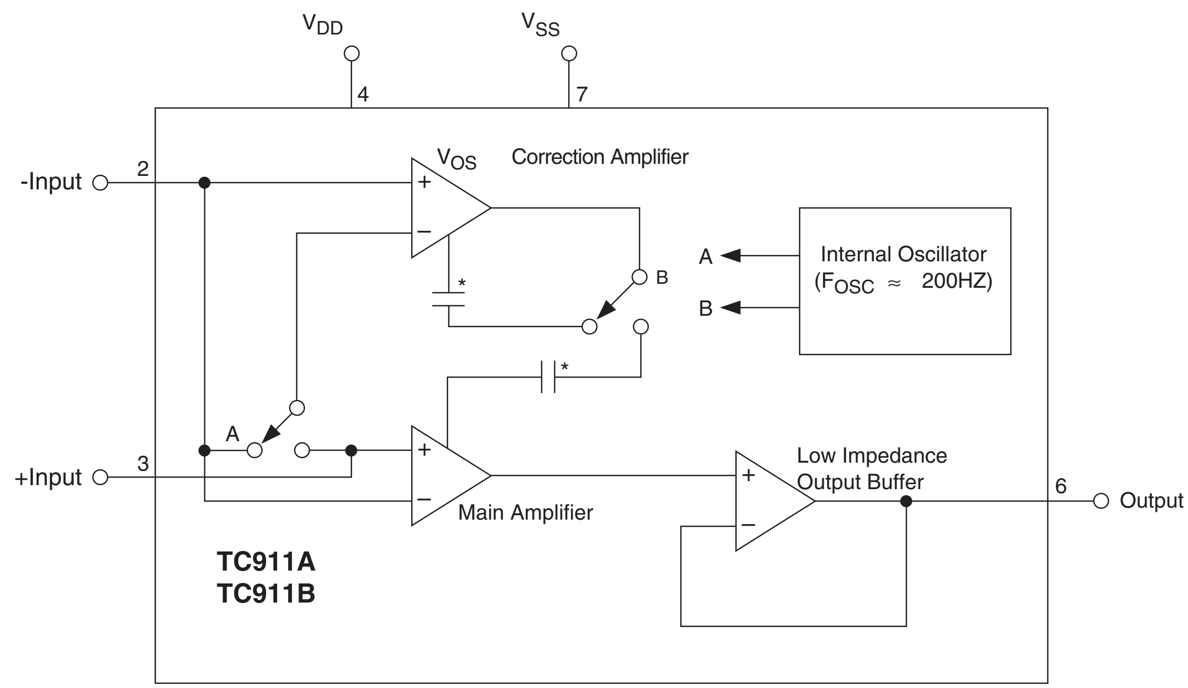
The TC911 CMOS auto-zeroed operational amplifier is the first complete monolithic chopper stabilized amplifier. Chopper operational amplifiers like the ICL7650/7652 and LTC1052 require user supplied, external offset compensation storage capacitors. **External capacitors are not required with the TC911.** Just as easy to use as the conventional OP07 type amplifier, the TC911 significantly reduces offset voltage errors. Pinout matches the OP07/741/7650 8-pin mini-DIP configuration.

Several system benefits arise by eliminating the external chopper capacitors: lower system parts count, reduced assembly time and cost, greater system reliability, reduced PC board layout effort and greater board area utilization. Space savings can be significant in multiple amplifier designs.

Electrical specifications include 15µV maximum offset voltage and 0.15µV/°C maximum offset voltage temperature co-efficient. Offset voltage error is five times lower than the premium OP07E bipolar device. The TC911 improves offset drift performance by eight times.

The TC911 operates from dual or single power supplies. Supply current is typically 350µA. Single 4.5V to 16V supply operation is possible, making single 9V battery operation possible. The TC911 is available in 2 package types: 8-pin plastic DIP and SOIC.

Functional Block Diagram



Note: Internal capacitors. No external capacitors required.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Total Supply Voltage (V_{DD} to V_{SS}) ....-18V
Input Voltage .... V_{DD} + 0.3V) to (V_{SS} – 0.3V)
Current Into Any Pin... 10mA
While Operating 100µA
Package Power Dissipation (T_A - 70°C)
Plastic DIP.. 730mW
Plastic SOIC... 470mW
Operating Temperature Range
C Device...................................... 0°C to +70°C
Storage Temperature Range.............. -65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC911A AND TC911B ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_S = ±5V, T_A = +25°C, unless otherwise indicated.									
			TC911A			**TC911B**			
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OS}	Input Offset Voltage	—	5	15	—	15	30	µV	T_A = +25°C
TCV_{OS}	Average Temp. Coefficient of Input Offset Voltage	— —	0.05 0.05	0.15 0.15	— —	0.1 0.1	0.25 0.25	µV/°C µV/°C	0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°C (**Note 1**)
I_B	Average Input Bias Current	— — —	— — —	70 3 4	— — —	— — —	120 4 6	pA nA nA	T_A = +25°C 0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°
I_{OS}	Average Input Offset Current	— —	5 —	20 1	— —	10 —	40 1	pA nA	T_A = +25°C T_A = +85°C
e_N	Input Voltage Noise	— —	0.65 11	— —	— —	0.65 11	— —	$µV_{P-P}$ $µV_{P-P}$	0.1 to 1Hz, R_S ≤ 100Ω 0.1 to 10Hz, R_S ≤ 100Ω
CMRR	Common Mode Rejection Ratio	110	116	—	105	110	—	dB	V_{SS} ≤ V_{CM} ≤ V_{DD} - 2.2
CMVR	Common Mode Voltage Range	V_{SS}	—	V_{DD} – 2	V_{SS}	—	V_{DD} – 2	V	
A_{OL}	Open-Loop Voltage Gain	115	120	—	110	120	—	dB	R_L = 10kΩ, V_{OUT} = ±4V
V_{OUT}	Output Voltage Swing	V_{SS} + 0.3	—	V_{DD} – 0.9	V_{SS} + 0.3	—	V_{DD} – 0.9	V	R_L = 10kΩ
BW	Closed Loop Bandwidth	—	1.5	—	—	1.5	—	MHz	Closed Loop Gain = +1
SR	Slew Rate	—	2.5	—	—	2.5	—	V/µsec	R_L = 10kΩ, C_L = 50pF
PSRR	Power Supply Rejection Ratio	112	—	—	105	—	—	dB	±3.3V to ±5.5V
V_S	Operating Supply Voltage Range	±3.3 6.5	— —	±8 16	±3.3 6.5	— —	±8 16	V V	Split Supply Single Supply
I_S	Quiescent Supply Current	—	350	600	—	—	800	µA	V_S = ±5V

Note 1: Characterized; not 100% tested.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in <Blue References>Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 5, 8	NC	No Internal Connection.
2	-INPUT	Inverting Input
3	+INPUT	Non-inverting Input
4	V_{SS}	Negative Power Supply
6	OUTPUT	Output
7	V_{DD}	Positive Power Supply

3.0 DETAILED DESCRIPTION

3.1 Pin Compatibility

The CMOS TC911 is pin compatible with the industry standard ICL7650 chopper stabilized amplifier. The ICL7650 must use external 0.1µF capacitors connected at pins 1 and 8. **With the TC911, external offset voltage error canceling capacitors are not required.** On the TC911 pins 1, 8 and 5 are not connected internally. The ICL7650 uses pin 5 as an optional output clamp connection. External chopper capacitors and clamp connections are not necessary with the TC911. External circuits connected to pins 1, 8 and 5 will have no effect. The TC911 can be quickly evaluated in existing ICL7650 designs. Since external capacitors are not required, system part count, assembly time and total system cost are reduced. Reliability is increased and PC board layout eased by having the error storage capacitors integrated on the TC911 chip.

The TC911 pinout matches many existing op amps: 741, LM101, LM108, OP05–OP08, OP-20, OP-21, ICL7650 and ICL7652. In many applications operating from +5V supplies, the TC911 offers superior electrical performance and can be a functional pin compatible replacement. Offset voltage correction potentiometers, compensation capacitors, and chopper stabilization capacitors can be removed when retro-fitting existing equipment designs.

3.2 Thermocouple Errors

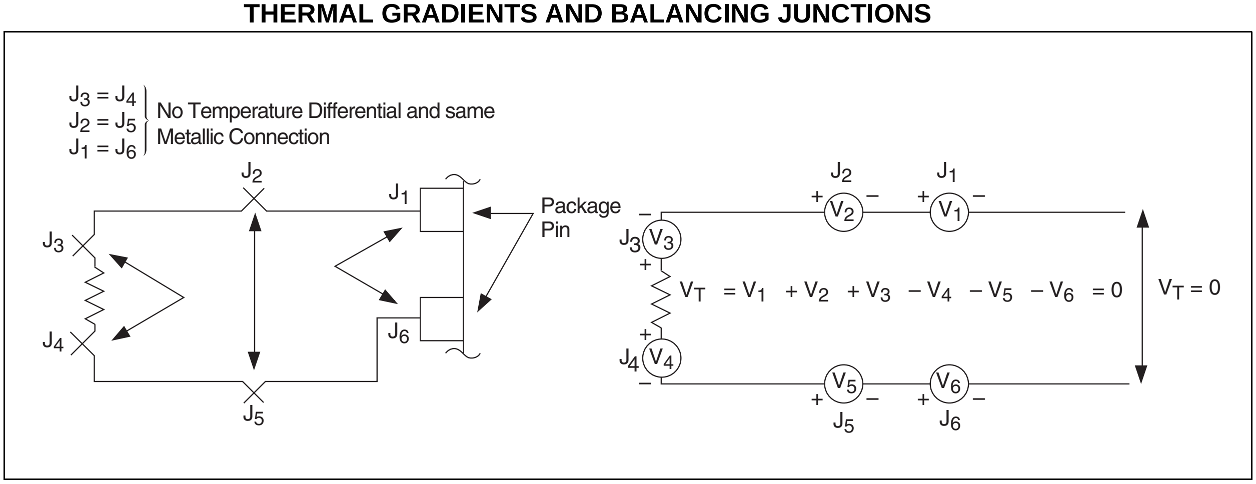
Heating one joint of a loop made from two different metallic wires causes current flow. This is known as the Seebeck effect. By breaking the loop, an open circuit voltage (Seebeck voltage) can be measured. Junction temperature and metal type determine the magnitude. Typical values are 0.1µV/°C to 10µV/°C. Thermal induced voltages can be many times larger than the TC911 offset voltage drift. Unless unwanted thermocouple potentials can be controlled, system performance will be less than optimum.

Unwanted thermocouple junctions are created when leads are soldered or sockets/connectors are used. Low thermo-electric coefficient solder can reduce errors. A 60% Sn/36% Pb solder has 1/10 the thermal voltage of common 64% Sn/36% Pb solder at a copper junction.

The number and type of dissimilar metallic junctions in the input circuit loop should be balanced. If the junctions are kept at the same temperature, their summation will add to zero-canceling errors (Figure 3-1).

Shielding precision analog circuits from air currents - especially those caused by power dissipating components and fans - will minimize temperature gradients and thermocouple induced errors.

FIGURE 3-1: UNWANTED THERMOCOUPLE ERRORS ELIMINATED BY REDUCING THERMAL GRADIENTS AND BALANCING JUNCTIONS



3.3 Avoiding Latchup

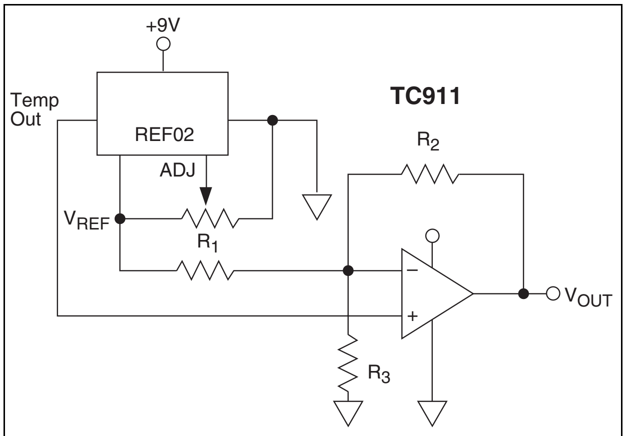
Junction isolated CMOS circuits inherently contain a parasitic p-n-p-n transistor circuit. Voltages exceeding the supplies by 0.3V should not be applied to the device pins. Larger voltages can turn the p-n-p-n device on, causing excessive device power supply current and excessive power dissipation. TC911 power supplies should be established at the same time or before input signals are applied. If this is not possible, input current should be limited to 0.1mA to avoid triggering the p-n-p-n structure.

3.4 Overload Recovery

The TC911 recovers quickly from the output saturation. Typical recovery time from positive output saturation is 20msec. Negative output saturation recovery time is typically 5msec.

4.0 TYPICAL APPLICATIONS

FIGURE 4-1: THERMOMETER CIRCUIT



$$V_{OUT} = V_{TEMP}\left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \times R_1}\right)\right] - \left[V_{REF}\,\frac{R_2}{R_1}\right]$$

$$\frac{d\,V_{OUT}}{dT} \approx \left[1 + R_2\left(\frac{R_3 + R_1}{R_3 \times R_1}\right)\right]\frac{d\,(V_{TEMP})}{dT} \approx K\ (2.1\ \text{mV/C})$$

$$K = 1 + \frac{R_2}{R_3 \times R_1}$$

FIGURE 4-2: 10-VOLT PRECISION REFERENCE

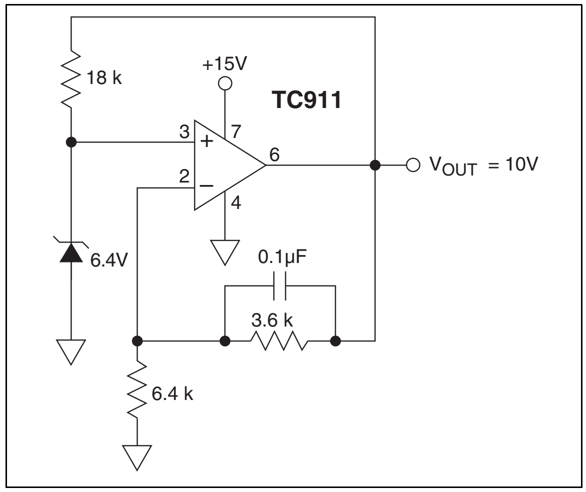
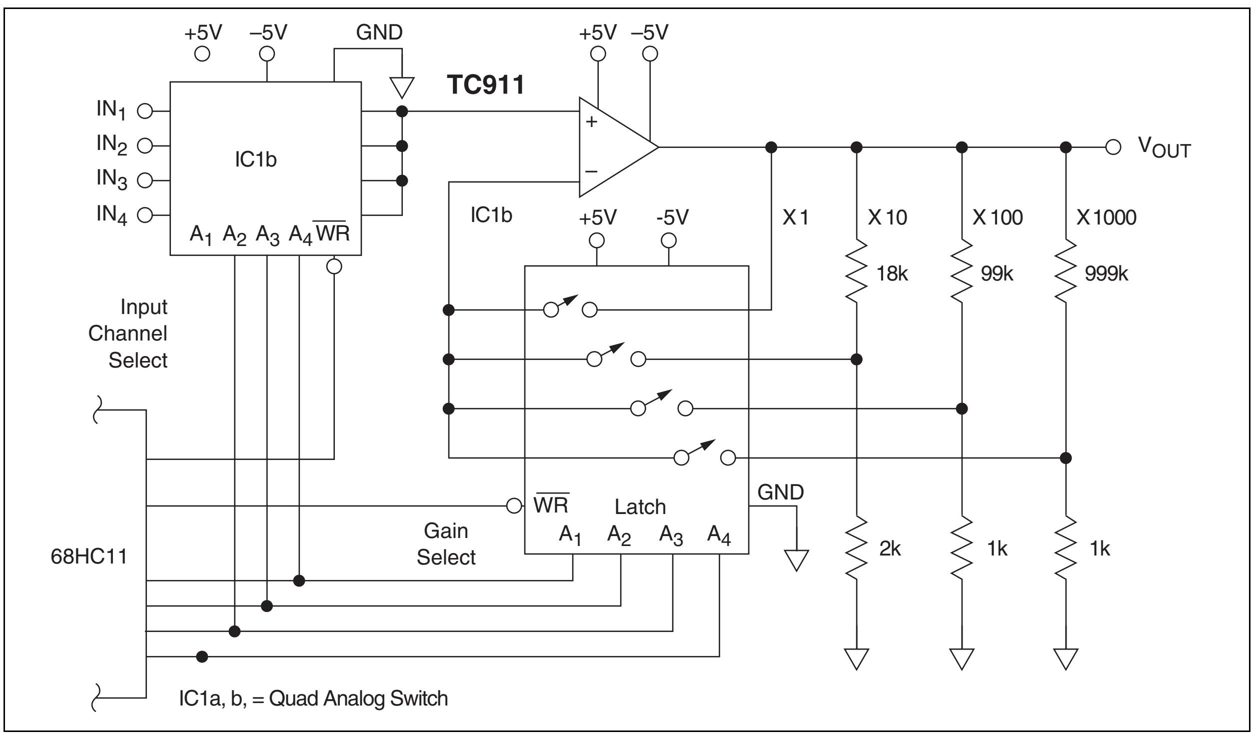


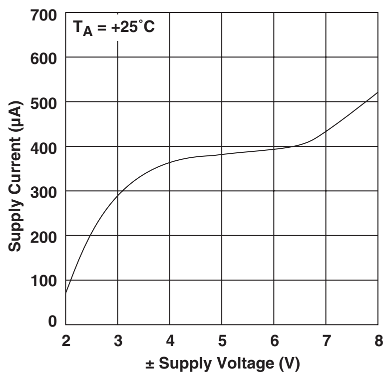
FIGURE 4-3: PROGRAMMABLE GAIN AMPLIFIER WITH INPUT MULTIPLEXER



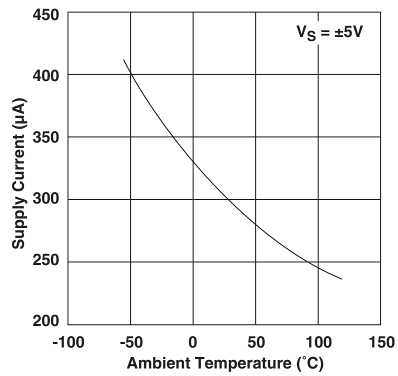
5.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

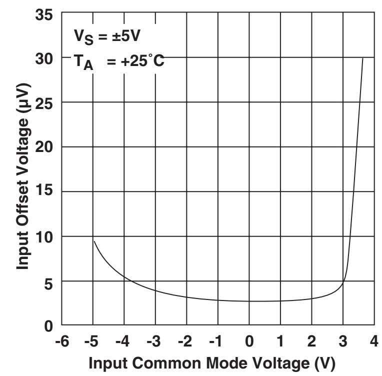
Supply Current vs. ± Supply Voltage



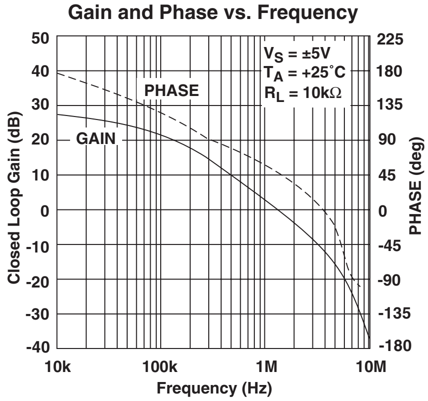
Supply Current vs. Temperature



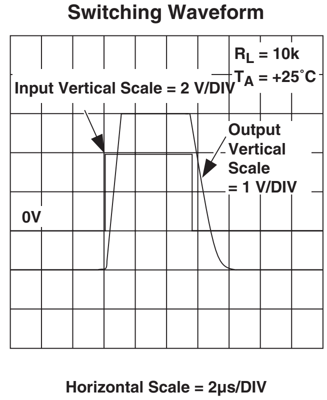
Input Offset Voltage vs. Common-Mode Voltage



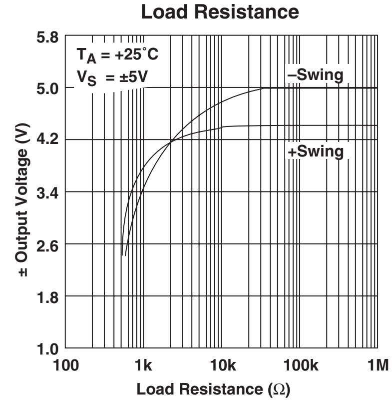
Gain and Phase vs. Frequency



Large Signal Output Switching Waveform



Output Voltage Swing vs. Load Resistance



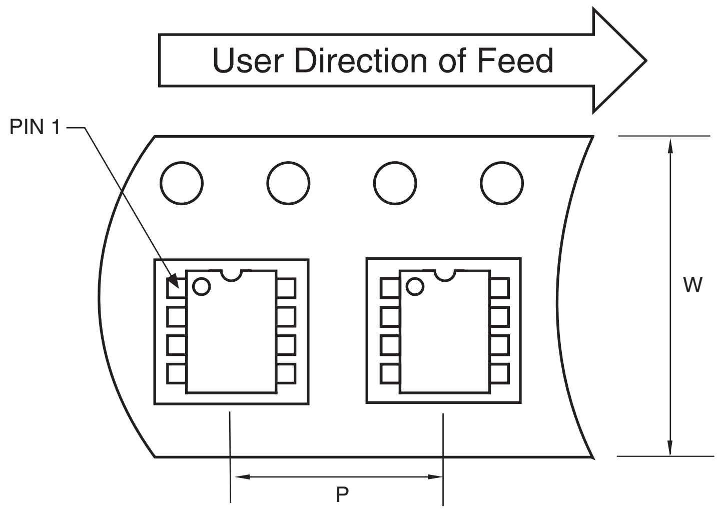
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

Package marking data not available at this time.

6.2 Taping Form

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



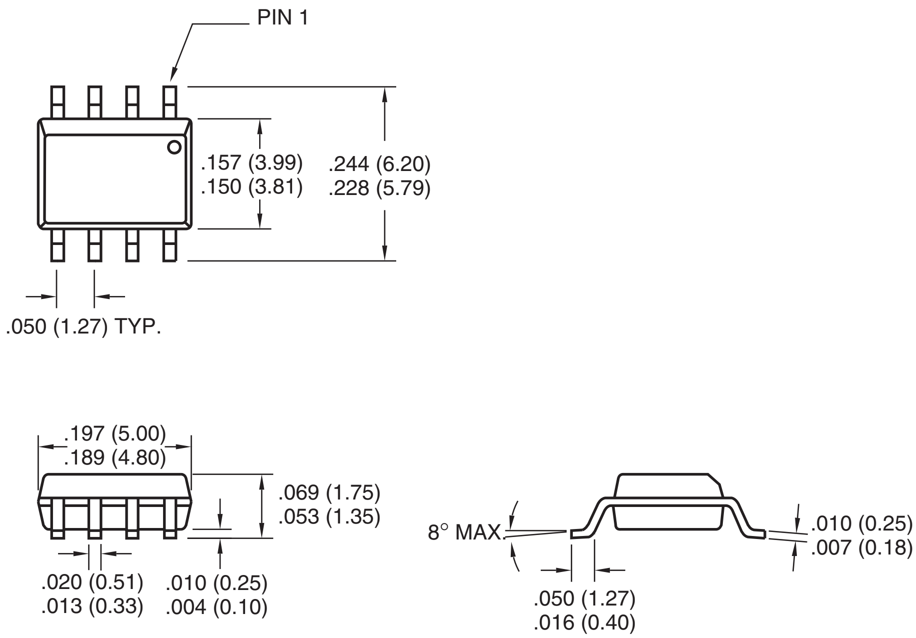
Standard Reel Component Orientation
for TR Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

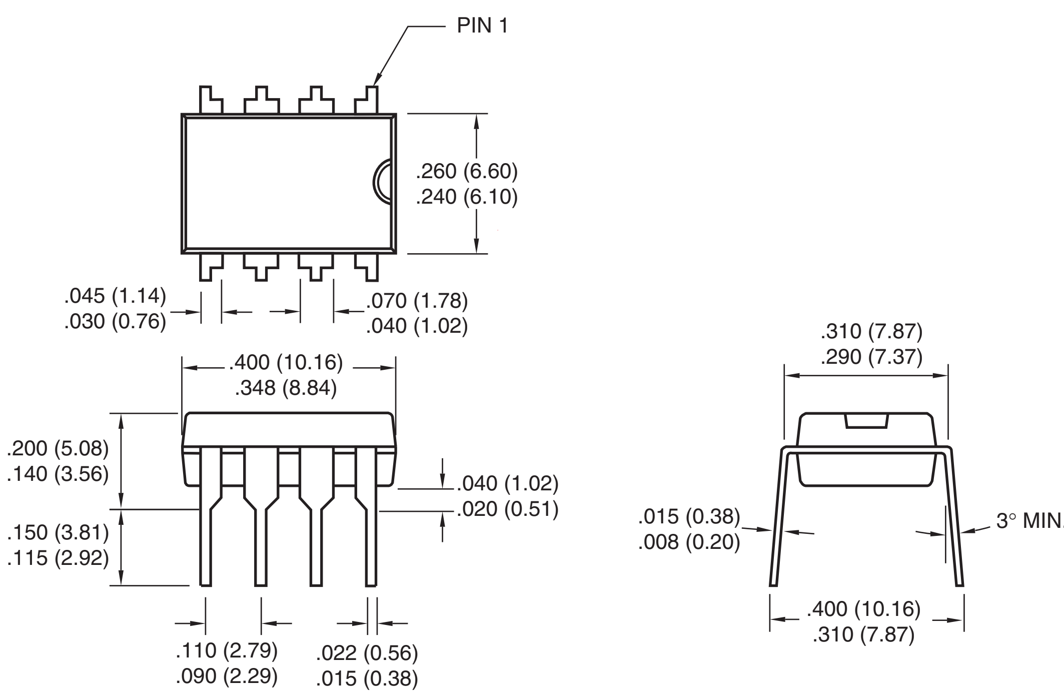
6.3 Package Dimensions

8-Pin SOIC



Dimensions: inches (mm)

8-Pin Plastic DIP



Dimensions: inches (mm)

NOTES:

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