Signetics

74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A Counters

'160, '162 BCD Decade Counter
'161, '163 4-Bit Binary Counter
Product Specification

Logic Products

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('160, '161)**
- **Synchronous reset ('162, '163)**
- **Hysteresis on Clock input (LS only)**

DESCRIPTION

Synchronous presettable decade (74160, 74LS160A, 74LS162A) and 4-bit (74161, 74LS161A, 74163, 74LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74160 – 74163	32MHz	61mA
74LS160A – 74LS163A	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74160N, N74LS160AN, N74161N, N74LS161AN N74LS162AN, N74163N, N74LS163AN
Plastic SO	N74LS161AD, N74S163AD

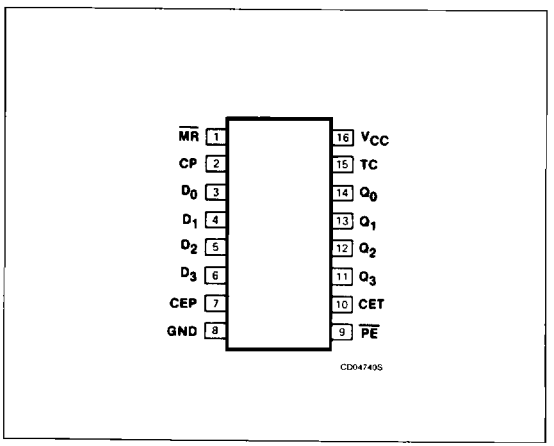
NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

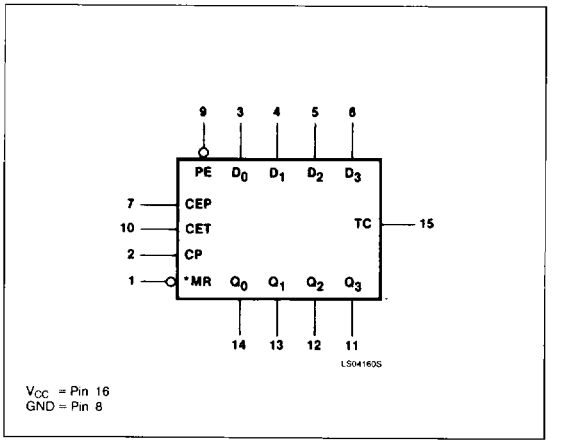
PINS	DESCRIPTION	74	74LS
CP, CET	Inputs	2ul	2LSul
D, CEP	Inputs	1ul	1LSul
$\overline{PE}$	Input	1ul	2LSul
All	Outputs	10ul	10LSul
$\overline{MR}$	Input ('160, '161)	1ul	1LSul
$\overline{MR}$	Input ('162, '163)	1ul	2LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

PIN CONFIGURATION



LOGIC SYMBOL



A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in '160, 'LS160A, '161, and 'LS161A to LOW levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'LS162A, '163, and LS163A, the clear function is synchronous. A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the set-up and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

For conventional operation of 74160, 74161 and 74163, the following transitions should be avoided.

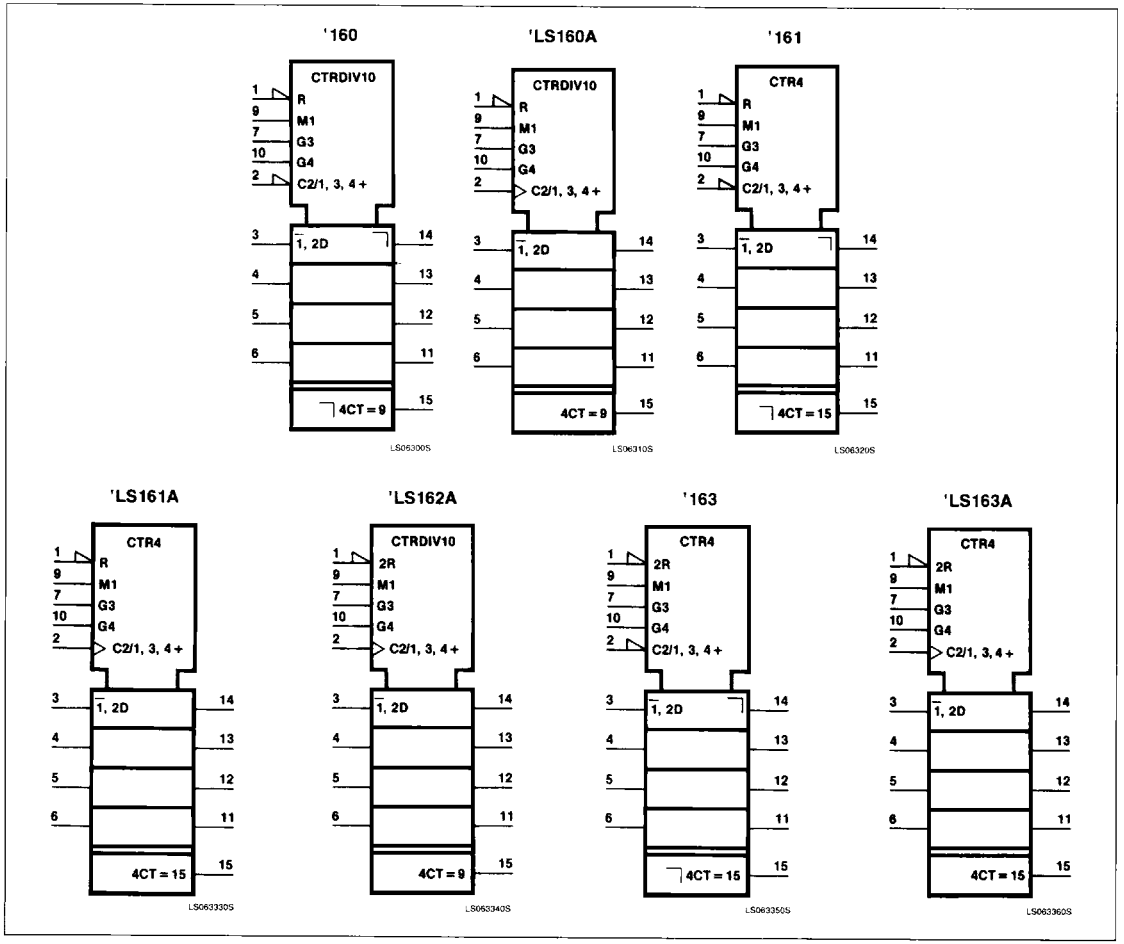
1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and $\overline{MR}$ are HIGH at or before the transition.

For 74163 there is an additional transition to be avoided.

3. LOW-to-HIGH transition on the $\overline{MR}$ input when clock is LOW, if the Enable and $\overline{PE}$ inputs are HIGH at or before the transition.

These restrictions are not applicable to 74LS160A, 74LS161A, 74LS162A and 74LS163A.

LOGIC SYMBOL (IEEE/IEC)



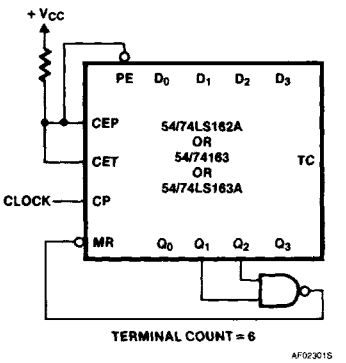


Figure 1

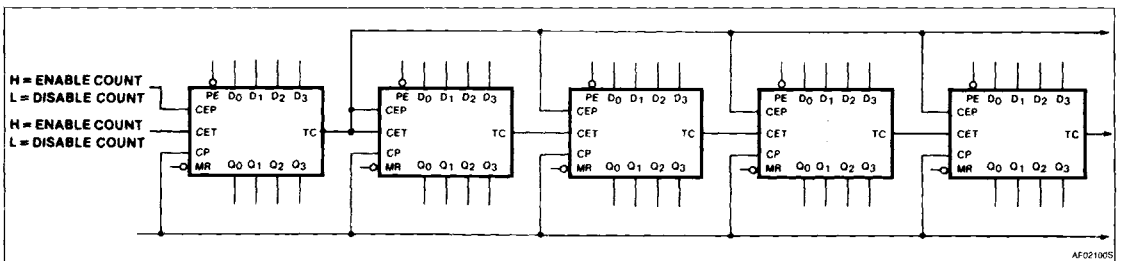
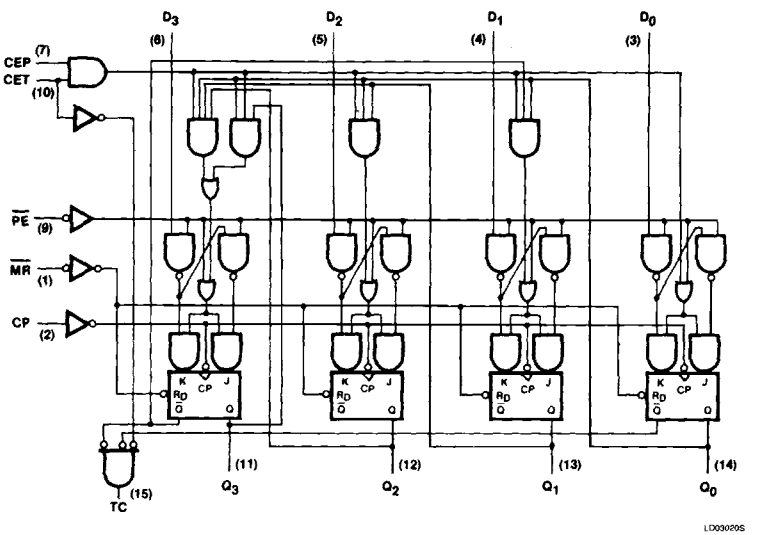


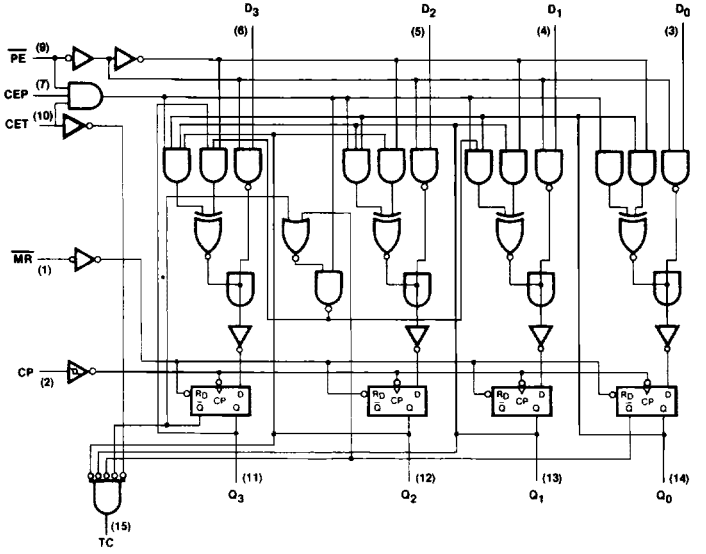
Figure 2. Synchronous Multistage Counting Scheme

LOGIC DIAGRAM, 74160

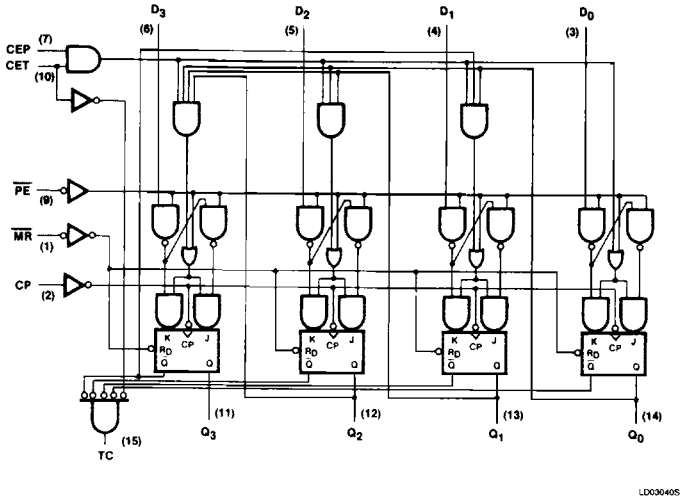


LOGIC DIAGRAMS

'LS160A



'161



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

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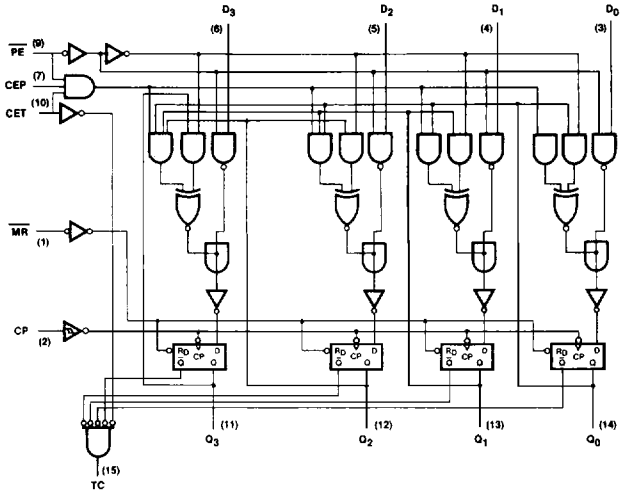
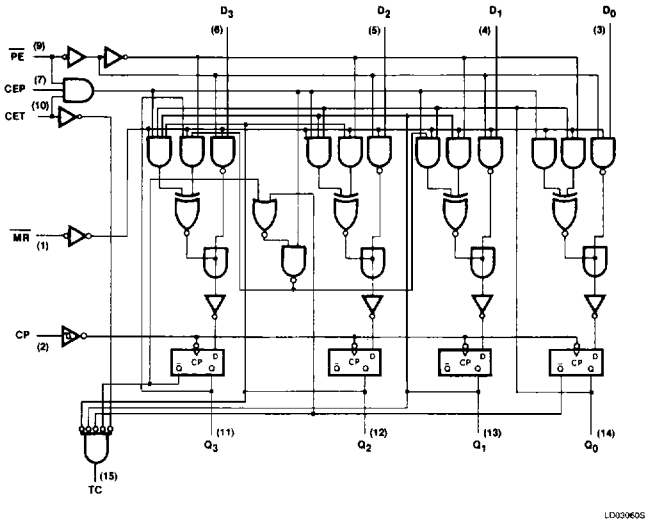
LOGIC DIAGRAMS

'LS161A



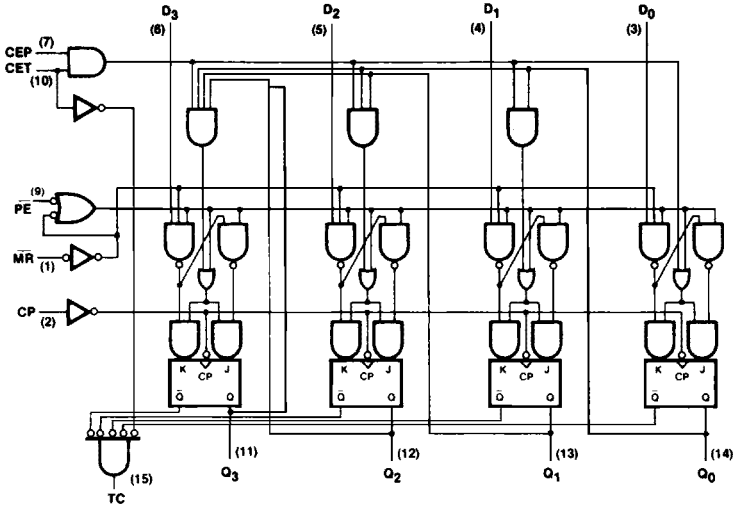
'LS162A



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

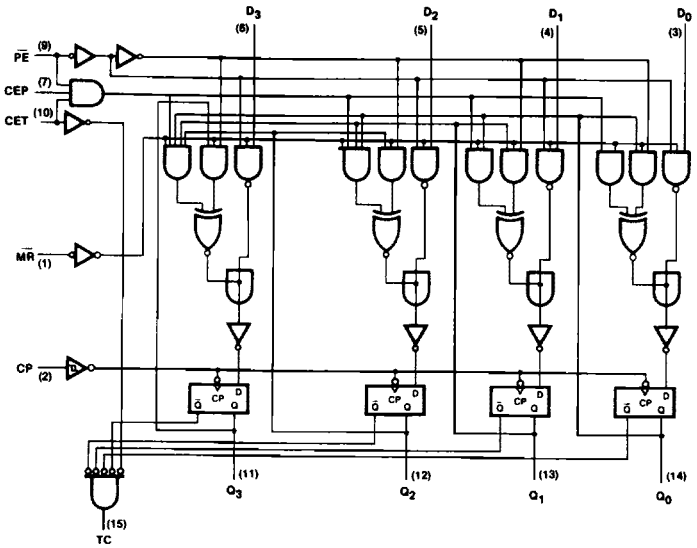
LOGIC DIAGRAMS

'163



LD03070S

'LS163A



LD03080S

V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

5

MODE SELECT — FUNCTION TABLE, '160, '161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h[c]	X	count	(a)
Hold (do nothing)	H	X	l[b]	X	h[c]	X	q_n	(a)
	H	X	X	l[b]	h[c]	X	q_n	L

MODE SELECT — FUNCTION TABLE, '162, '163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h[f]	↑	X	X	l	l	L	L
	h[f]	↑	X	X	l	h	H	(d)
Count	h[f]	↑	h	h	h[f]	X	count	(d)
Hold (do nothing)	h[f]	X	l[e]	X	h[f]	X	q_n	(d)
	h[f]	X	X	l[e]	h[f]	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES:

(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for '161 and HLLH for '160).
(b) The HIGH-to-LOW transition of CEP or CET on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{PE}$ on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.
(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for '162 and HHHH for '163).
(e) The HIGH-to-LOW transition of CEP or CET on the 74163 should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{PE}$ or $\overline{MR}$ on the 74163 should only occur while CP is HIGH for conventional operation.

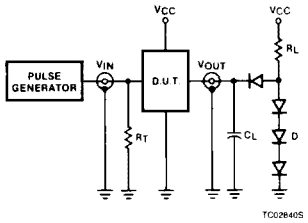
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

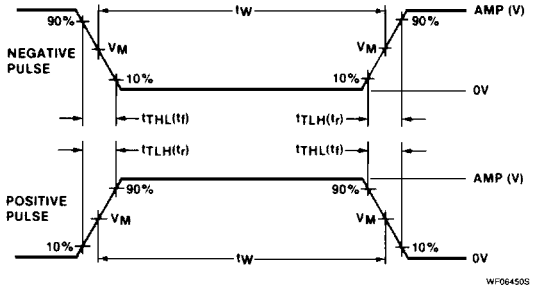
PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−800			−400	μA
I_{OL}	LOW-level output current			16			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74160, '161 '163			74LS160A, '161A '162A, '163A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX			0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)						0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	D, CEP						0.1	mA
				$\overline{PE}$, CP, CET						0.2	mA
				$\overline{MR}$, ('LS160A, 'LS161A)						0.1	mA
				$\overline{MR}$ ('LS162A, 'LS163A)						0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	CP, CET			80				μA
				Other inputs			40				μA
			V_I = 2.7V	D, CEP						20	μA
				$\overline{PE}$, CP, CET						40	μA
				$\overline{MR}$ ('LS160A, 'LS161A)						20	μA
				$\overline{MR}$ ('LS162A, 'LS163A)						40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	CP, CET			−3.2				mA
				Other inputs			−1.6				mA
			V_I = 0.4V	D, CEP						−0.4	mA
				$\overline{PE}$, CP, CET						−0.8	mA
				$\overline{MR}$ ('LS160A, 'LS161A)						−0.4	mA
				$\overline{MR}$ ('LS162A, 'LS163)						−0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−18		−57	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} All outputs HIGH			59	94		18	31	mA
			I_{CCL} All outputs LOW			63	101		19	32	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX+0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CCH} is measured with $\overline{PE}$ input HIGH, again with $\overline{PE}$ input LOW, all other inputs HIGH and outputs open. I_{CCL} is measured with Clock input HIGH, again with Clock input LOW, all other inputs low and outputs open.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		35 35		35 35	ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = HIGH		20 23		24 27	ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = LOW		25 29		24 27	ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		16 16		14 14	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('160, '161)	Waveform 3		38		28	ns

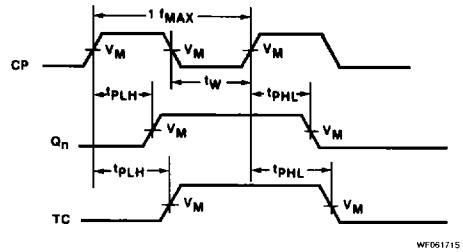
NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('160, '161)	Waveform 3	20		20		ns
t_W	Master Reset pulse width ('162, '163)	Waveform 6	20		20		ns
t_s	Set-up time, data to clock	Waveform 5	20		20		ns
t_h	Hold time, data to clock[1]	Waveform 5	3		3		ns
t_s	Set-up time, CEP or CET to clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s	Set-up time, $\overline{PE}$ to clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 5	0		0		ns
t_s	Set-up time, $\overline{MR}$ to clock ('162, '163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to clock ('162, '163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

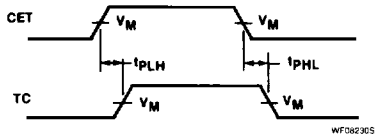
NOTE:
1. For 15ns rise time only, Hold time must be increased by 0.3ns for each nanosecond decrease in rise time.

AC WAVEFORMS



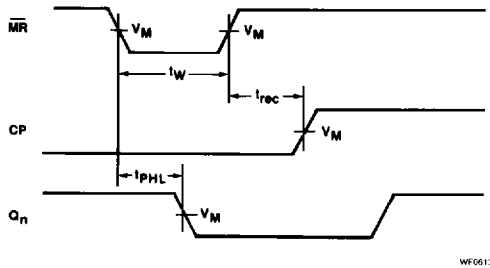
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 1. Clock To Output Delays, Maximum Frequency, And Clock Pulse Width



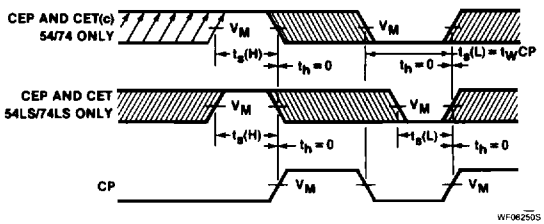
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 2. Propagation Delays CET Input To TC Output



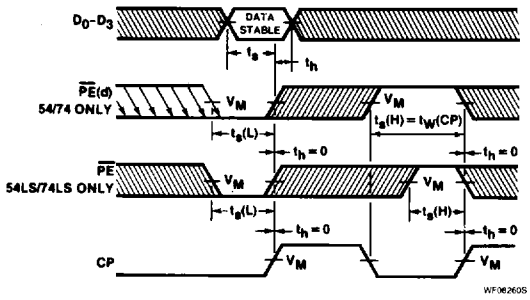
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.

Waveform 3. Master Reset Pulse Width, Master Reset To Output Delay and Master Reset To Clock Recovery Time ('160, '161)



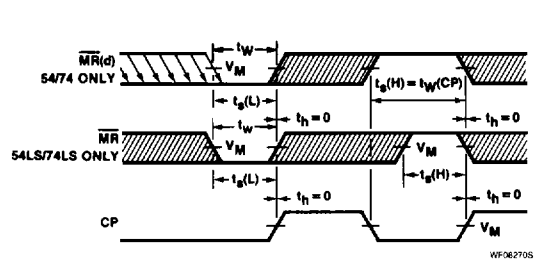
V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. CEP And CET Set-up And Hold Times



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5. Parallel Data And Parallel Enable Set-up And Hold Times



V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 6. Synchronous Reset Set-up, Pulse Width And Hold Times ('162, '163)