Pentium® and Pentium Pro® Motherboard Clock Generator

Features

- Four-skew controlled CPU clock outputs (PCLK0-PCLK3) 66, 60, and 50 MHz selectable
- Six-skew controlled synchronous PCI clock outputs (BCLK0 BCLK5) at one-half of the CPU clock frequency and synchronous
- One fixed clock output at 48 MHz
- Three 14.318 MHz reference clock outputs: (REF2-REF0)
- Supports 3.3V operation
- Controlled output buffer rise/fall time
- Built in crystal oscillator circuit
- On-chip PLL loop filters
- Low power CMOS design
- Test mode support
- Packages available:
  - 28-pin 209-mil wide SSOP (H28)
  - 28-pin 300-mil wide SOIC (S28)

CPU and PCI Bus Clock Outputs

Four selectable CPU clock outputs (PCLK0-3) and six PCI clock outputs (BCLK0-5) are provided. Output frequency of the CPU and PCI clock outputs are selected with input pins SEL0 and SEL1 as shown in Table 1.

Table 1. Output Frequency Selection

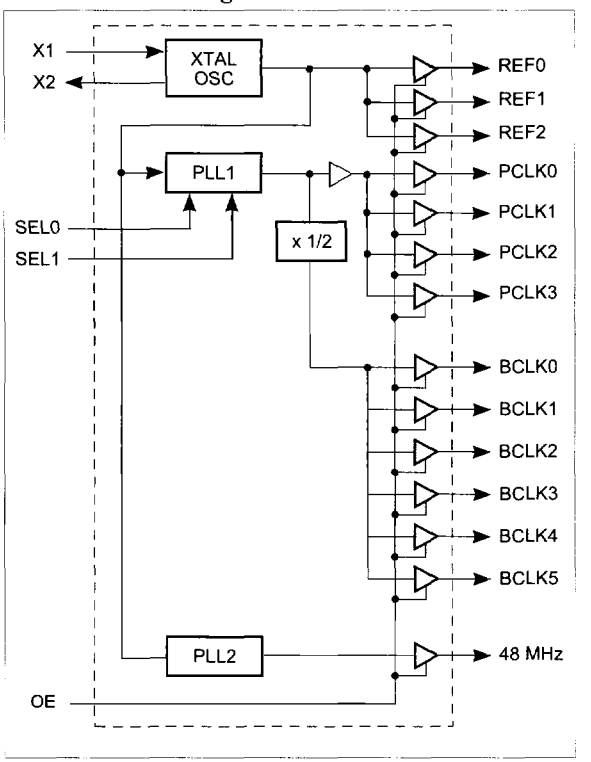
Select Address SEL1	Select Address SEL0	CPU Clock: PCLK0-3 (MHz)	PCI Clock BCLK0-5 (MHz)
0	0	50	25
0	1	66.6	33.3
1	0	60	30
1	1	Test Mode	Test Mode

Description

Pericom Semiconductor's PI6C series of clock generators are produced in the Company's advanced 0.8 micron CMOS process.

The PI6C980 clock generator provides a complete system clock solution for Intel Pentium and Pentium Pro motherboards with PCI buses. It is designed to fully meet Intel Pentium, Pentium Pro, and Intel Triton 2 chipsets.

Function Block Diagram



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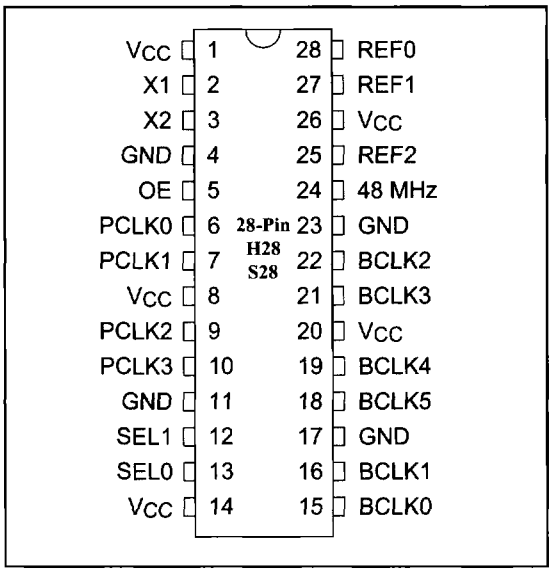
Product Pin Configuration



Test Mode

The PI6C980 also includes a special test mode which can be used in production system verification (Table 1). When using the test mode, X1 is driven with an external clock (Reference Frequency) and the following output clock frequencies result:

Reference Frequency

Device Pin	Output Frequency
REF0/1	Reference Frequency
48 MHz	Reference Frequency/2
BLK0-5	Reference Frequency/4
PCLK0-3	Reference Frequency/2

Pin Descriptions

Pin Name	I/O	Description
REF2	O	Fixed 14.318 MHz output for various motherboard functions
48 MHz	O	Fixed 48 MHz output for floppy drive or Super I/O applications
BCLK0	O	Selectable frequency output for PCI bus clock applications
BCLK1	O	Selectable frequency output for PCI bus clock applications
BCLK2	O	Selectable frequency output for PCI bus clock applications
BCLK3	O	Selectable frequency output for PCI bus clock applications
BCLK4	O	Selectable frequency output for PCI bus clock applications
BCLK5	O	Selectable frequency output for PCI bus clock applications
GND	—	Ground connection
OE	I	Output Enable, puts all outputs in high impedance state when low. This input has internal pull-up device.
PCLK0	O	Selectable frequency output for CPU clock applications
PCKL1	O	Selectable frequency output for CPU clock applications
PCLK2	O	Selectable frequency output for CPU clock applications
PCLK3	O	Selectable frequency output for CPU clock applications
REF0	O	Fixed 14.318 MHz output for various motherboard functions
REF1	O	Fixed 14.318 MHz output for various motherboard functions
SEL0	I	Frequency Selection input. This input has internal pull-up device.
SEL1	I	Frequency Selection input. This input has internal pull-up device.
VCC	—	Power supply connection, 3.3V
X1	I	Crystal connection or external reference frequency input
X2	—	Crystal connection, leave unconnected when using external reference

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	0°C to +70°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics at 3.3V (Operating Range, V_{CC} = +3.3V ±10%, Temperature 0°C to +70°C)

Parameters	Description	Test Conditions	Min.	Max.	Units
I_{IL}	Input LOW Current, except X1	V_{IN}=0V	-5.0	5.0	µA
I_{IH}	Input HIGH Current, except X1	V_{IN}=V_{CC}	-5.0	5.0	µA
I_{OL}	Output LOW Current	V_{OL}=0.8V; for PCLKS & BCLKS, V_{CC}=Min.	30.0		mA
I_{OH}	Output HIGH Current	V_{OL}=2.0V; for PCLKS & BCLKS, V_{CC}=Min.		-31.0	mA
I_{OL}	Output LOW Current	V_{OL}=0.8V; for fixed CLKs, V_{CC}=Min.	25.0		mA
I_{OH}	Output HIGH Current	V_{OL}=2.0V; for fixed CLKs, V_{CC}=Min.		-30.0	mA
V_{OL}	Output LOW Voltage	I_{OL}=15mA; for PCLKS & BCLKS, V_{CC}=Min.		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH}=20mA; for PCLKS & BCLKS, V_{CC}=Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL}=12.5mA; for fixed CLKS, V_{CC}=Min.		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH}=20mA; for fixed CLKS, V_{CC}=Min.	2.4		V
I_{CC}	Supply Current	@66.66MHz; all outputs unloaded		110	mA

AC Electrical Characteristics[1] (Operating Range, VCC = 3.3V ±10%, Temperature 0°C to 70°C)

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
Processor Clock Outputs, PCLK0-3:						
T_{jab}	Output Clock Jitter, Absolute				±250	ps
t_{SK}	Output Clock Skew	Between any two outputs			250	ps
t_P	Period Time (50 MHz)		20.0			ns
$t_{H/L}$	High/Low Time (50 MHz)	Above 2.4V, Below 0.4V	4.0			ns
t_P	Period Time (60 MHz)		16.7			ns
$t_{H/L}$	High/Low Time (60 MHz)	Above 2.4V, Below 0.4V	4.0			ns
t_P	Period Time (66 MHz)		15.0			ns
$t_{H/L}$	High/Low Time (66 MHz)	Above 2.4V, Below 0.4V	4.0			ns
Bus Clock Outputs, BCLK0-5:						
T_{jab}	Output Clock Jitter, Absolute				±350	ps
t_{SK}	Output Clock Skew	Between any two outputs			500	ps
t_P	Period Time (25 MHz)		40.0			ns
$t_{H/L}$	High/Low Time (25 MHz)	Above 2.4V, Below 0.4V	16.0			ns
t_P	Period Time (30 MHz)		33.3			ns
$t_{H/L}$	High/Low Time (30 MHz)	Above 2.4V, Below 0.4V	13.0			ns
t_P	Period Time (33 MHz)		30.0			ns
$t_{H/L}$	High/Low Time (33 MHz)	Above 2.4V, Below 0.4V	12.0			ns
T_{SK}	Skew from PCLKx to BCLKx[2]		1.0		5.0	ns
Regarding All Clock Outputs:						
dt	Output Duty Cycle		45	50	55	%
tr	Output Rise Time	From 0.4V to 2.4V	1.0		4.0	ns
tf	Output Fall Time	From 2.4V to 0.4V	1.0		24.0	ns
T_{PU}	Stabilization Time from Power-Up	Within 0.1% of Final Freq.			3.0	ms
f_D	Long-Term Output Frequency Stability[3]	Over Vcc and T_A Range			0.1	%

Notes:

1. All AC tests are performed with the following load conditions: PCLK0-3 = 20 pF, BCLK0-5 = 30 pF, 48 MHz = 20 pF, REF0 = 30 pF, REF1 = 15 pF and REF2 = 20 pF. Threshold voltage for timing measurements is 1.5V.
2. PCLK outputs lead BCLK outputs.
3. Output Frequency Stability is solely determined by crystal oscillator frequency shift.