T-46-23-12

MATRA M H S

September 1990

**DATA SHEET**

# HM 65728

## 2 k x 8
## HIGH SPEED CMOS SRAM

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## FEATURES

- **FAST ACCESS TIME**
  **MILITARY : 35/45/55 ns (max)**
  **COMMERCIAL : 20/25/35/45/55 ns (max)**
- **LOW POWER CONSUMPTION**
  **ACTIVE : 310 mW (typ)**
  **STANDBY : 55 mW (typ)**
- **WIDE TEMPERATURE RANGE :**
  **– 55°C TO + 125°C**
- **300 AND 600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

## DESCRIPTION

The HM 65728 is a high speed CMOSstatic RAM organized as 2048 x 8 bits. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 20 ns are available with maximum power consumption of only 600 mW.
The HM 65728 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 80 % when the circuit is deselected.

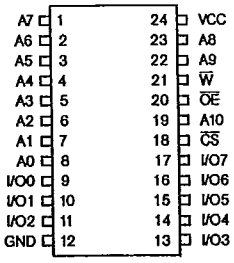
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65728 are TTL compatible and operate from single 5V supply thus simplifying system design.
The HM 65728 is processed following the test methods of MIL STD 883C.

## PACKAGES

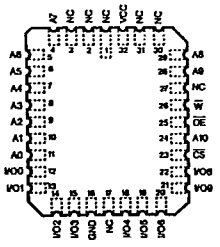
Plastic 300 & 600 mils, 24 pins, DIL
SO 300 mils, 24 pins
Tape and Reel Service

Ceramic 300 mils, 24 pins, DIL
LCC, 32 pins

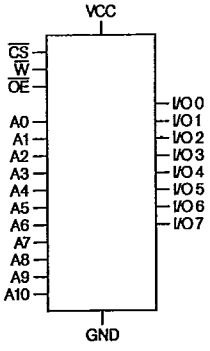
**Pinout DIL 24 pins (top view)**




**Pinout LCC 32 pins (top view)**



## LOGIC SYMBOL



## BLOCK DIAGRAM

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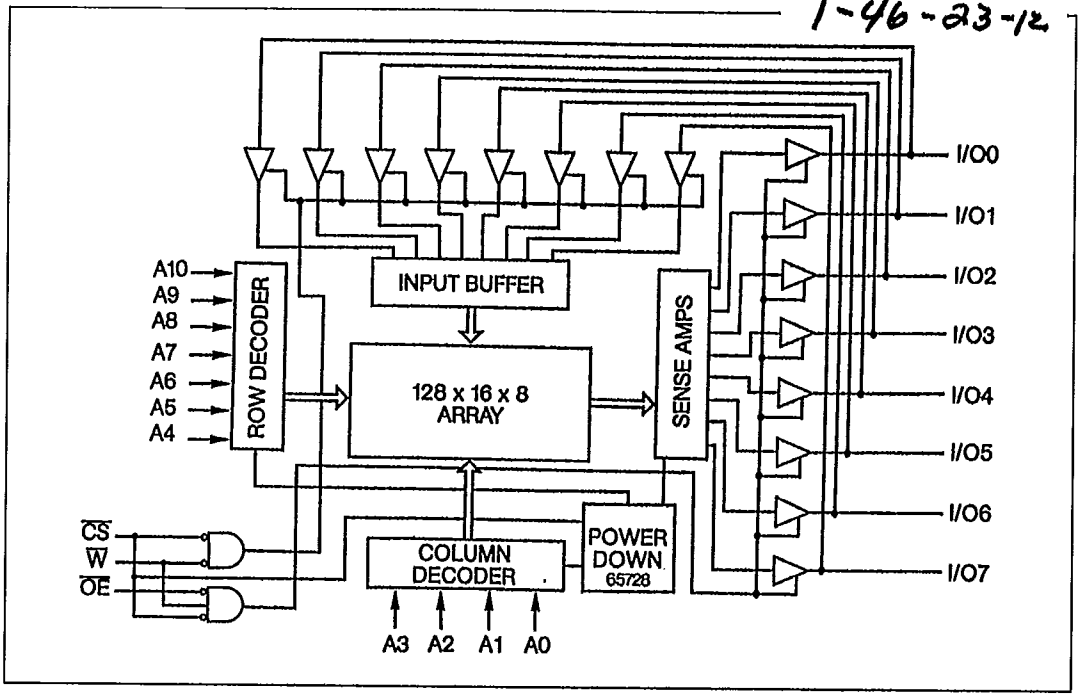


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### PIN NAMES

| | | | |
|---|---|---|---|
| A0-A10 | : Address inputs | $\overline{CS}$ | : Chip Select |
| I/O0–I/O7 | : Input/Output | $\overline{OE}$ | : Output Enable |
| Vcc | : Power | $\overline{W}$ | : Write enable |
| Gnd | : Ground | | |

### TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{W}$ | DATA-IN | DATA-OUT | MODE |
|---|---|---|---|---|---|
| H | X | X | Z | Z | Deselect |
| L | L | H | Z | Valid | Read |
| L | H | L | Valid | Z | Write |
| L | L | L | Valid | Z | Write |

## ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

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## OPERATING RANGE

| | | OPERATING VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|---|
| Military | (– 2) | 5 V ± 10 % | – 55°C to + 125°C |
| Commercial | (– 5) | 5 V ± 10 % | 0°C to + 70°C |

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Vcc | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| Gnd | Ground | 0.0 | 0.0 | 0.0 | V |
| VIL | Input low voltage | – 3.0 | 0.0 | 0.8 | V |
| VIH | Input high voltage | 2.0 | – | 5.5 | V |

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## CAPACITANCE

| PARAMETER | | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| Cin | (1) | Input capacitance | – | – | 5 | pF |
| Cout | (1) | Output capacitance | – | – | 7 | pF |

**Note :** 1. TA = 25C, f = 1MHz, Vcc = 5.0V, these parameters are not tested.

## AC TEST LOADS WAVEFORMS

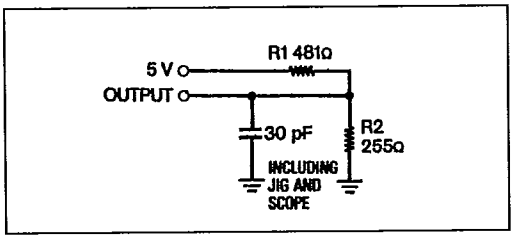



Fig. 1a.

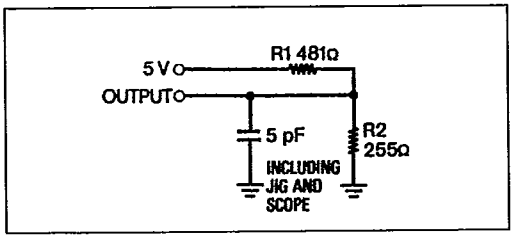
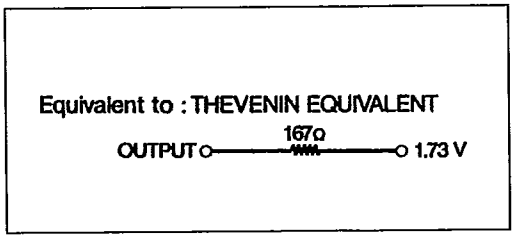



Fig. 1b.



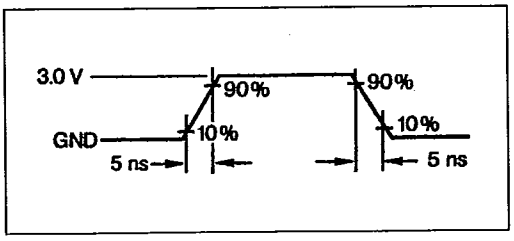




**Figure 2 :** All Input Pulses.

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## ELECTRICAL CHARACTERISTICS DC PARAMETER

| PARAMETER | DESCRIPTION | MINIMUM | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| IIX (2) | Input leakage current | −10.0 | – | 10.0 | µA |
| IOZ (3) | Output leakage current | −40.0 | – | 40.0 | µA |
| IOS (3) | Output short circuit current | – | – | −300.0 | mA |
| VOL (4) | Output low voltage | – | – | 0.4 | V |
| VOH (4) | Output high voltage | 2.4 | – | – | V |

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
4. Vcc min, IOL = 8.0 mA.
5. Vcc min, IOH = - 4.0 mA.

### Consumption for Commercial specification :

| SYMBOL | PARAMETER | 65728 F-5 | 65728 H-5 | 65728 K-5 | 65728 M-5 | 65728 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| ICCSB (6) | Standby supply current | 40 | 20 | 20 | 20 | 30 | mA | max |
| ICCOP (7) | Dynamic Operating current | 100 | 100 | 100 | 100 | 100 | mA | max |

### Consumption for Military specification :

| SYMBOL | PARAMETER | 65728 H-2* | 65728 K-2 | 65728 M-2 | 65728 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| ICCSB (6) | Standby supply current | 40 | 30 | 30 | 30 | mA | max |
| ICCOP (7) | Dynamic Operating current | 120 | 120 | 120 | 120 | mA | max |

Notes : 6. $\overline{CS} \geq VIH$, a pull up resistor to Vcc on the CS input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary specification.

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## ELECTRICAL CHARACTERISTICS AC PARAMETERS

### AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns

Input timing reference levels : 1.5 V
Output loading IOL/IOH (*see figure 1a and 1b*) : + 30 pF

### WRITE CYCLE : Commercial Specification

| SYMBOL | PARAMETER | 65728 F-5 | 65728 H-5 | 65728 K-5 | 65728 M-5 | 65728 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Write cycle time | 20 | 25 | 35 | 45 | 55 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 20 | 20 | 30 | 40 | 50 | ns | min |
| TDVWH | Data set-up time | 15 | 15 | 15 | 20 | 25 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 20 | 20 | 30 | 40 | 50 | ns | min |
| TWLQZ (8) | Write low to high Z | 10 | 10 | 15 | 15 | 20 | ns | max |
| TWLWH | Write pulse width | 15 | 20 | 20 | 20 | 30 | ns | min |
| TWHAX | Address hold to end of write | 0 | 2 | 2 | 2 | 2 | ns | min |
| TWHDX | Data hold time | 0 | 0 | 0 | 0 | 5 | ns | min |
| TWHQX (8, 9) | Write high to low Z | 3 | 3 | 0 | 0 | 0 | ns | min |
| TEHAX | Address hold end $\overline{CS}$ | 3 | 3 | 3 | 3 | 3 | ns | min |

**Notes :** 8. The data input set up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. At any given temperature and voltage condition, TWHQX is less than TWLQZ for all devices. These parameters are sampled and not 100 % tested.
* Preliminary specification.

### WRITE CYCLE : Military specification

| SYMBOL | PARAMETER | 65728 H-2* | 65728 K-2 | 65728 M-2 | 65728 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Write Cycle time | 25 | 35 | 45 | 55 | ns | min |
| TAVWL | Address set-up time | 0 | 0 | 0 | 0 | ns | min |
| TAVWH | Address valid to end of write | 20 | 30 | 40 | 50 | ns | min |
| TDVWH | Data set-up time | 10 | 15 | 20 | 25 | ns | min |
| TELWH | $\overline{CS}$ low to write end | 20 | 30 | 40 | 50 | ns | min |
| TWLQZ (8) | Write low to high Z | 10 | 15 | 15 | 20 | ns | max |
| TWLWH | Write pulse width | 20 | 20 | 25 | 30 | ns | min |
| TWHAX | Address hold to end of write | 2 | 2 | 2 | 2 | ns | min |
| TWHDX | Data hold time | 5 | 5 | 5 | 5 | ns | min |
| TEHAX | Address hold end $\overline{CS}$ | 3 | 3 | 3 | 3 | ns | min |

* Preliminary specification

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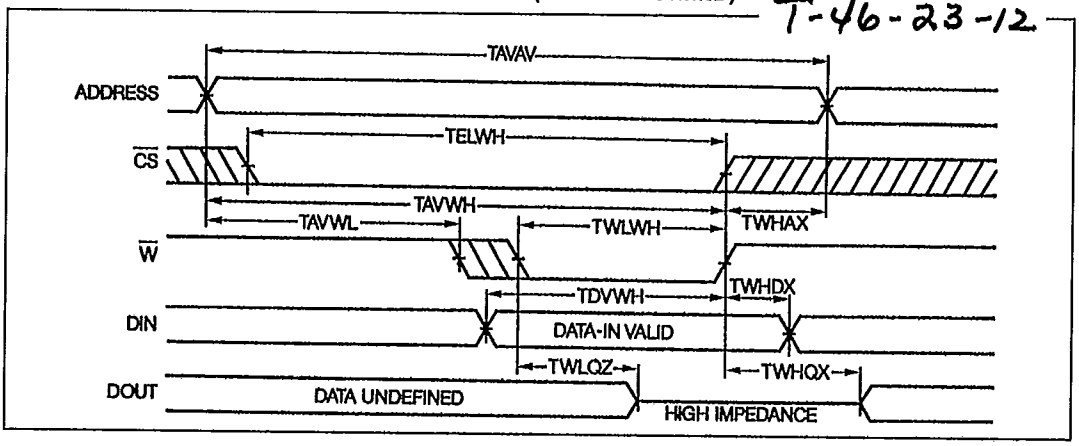
## WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)

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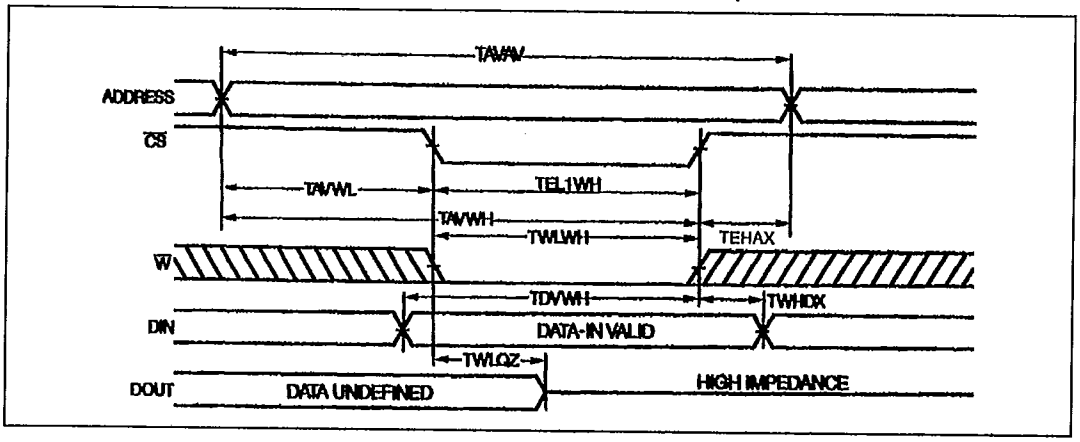
## WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



**READ CYCLE : Commercial specification**

| SYMBOL | PARAMETER | 65728 F-5 | 65728 H-5 | 65728 K-5 | 65728 M-5 | 65728 N-5 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 20 | 25 | 35 | 45 | 55 | ns | min |
| TAVQV | Address access time | 20 | 25 | 35 | 45 | 55 | ns | max |
| TAVQX | Address valid to low Z | 3 | 3 | 5 | 5 | 5 | ns | min |
| TELQV | Chip-select access time | 20 | 25 | 35 | 45 | 55 | ns | max |
| TELQX | $\overline{CS}$ low to low Z | 3 | 3 | 5 | 5 | 5 | ns | min |
| TEHQZ | $\overline{CS}$ high to high Z | 12 | 12 | 15 | 20 | 20 | ns | max |
| TELIC | $\overline{CS}$ low to power up | 0 | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | $\overline{CS}$ high to power down | 15 | 15 | 20 | 25 | 25 | ns | max |
| TGLQV | Output enable access time | 10 | 15 | 15 | 20 | 25 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 2 | 2 | 0 | 0 | 0 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 10 | 10 | 15 | 15 | 20 | ns | max |

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**READ CYCLE : Military specification**

| SYMBOL | PARAMETER | 65728 H-2* | 65728 K-2 | 65728 M-2 | 65728 N-2 | UNIT | VALUE |
|---|---|---|---|---|---|---|---|
| TAVAV | Read cycle time | 25 | 35 | 45 | 55 | ns | min |
| TAVQV | Address access time | 25 | 35 | 45 | 55 | ns | max |
| TAVQX | Address valid to low Z | 3 | 5 | 5 | 5 | ns | min |
| TELQV | Chip-select access time | 25 | 35 | 45 | 55 | ns | max |
| TELQX | $\overline{CS}$ low to low Z | 3 | 5 | 5 | 5 | ns | min |
| TEHQZ | $\overline{CS}$ high to high Z | 12 | 15 | 20 | 20 | ns | max |
| TELIC | $\overline{CS}$ low to power up | 0 | 0 | 0 | 0 | ns | min |
| TEHICL | $\overline{CS}$ high to power down | 20 | 20 | 25 | 25 | ns | max |
| TGLQV | Output enable access time | 12 | 15 | 20 | 25 | ns | max |
| TGLQX | $\overline{OE}$ low to low Z | 0 | 0 | 0 | 0 | ns | min |
| TGHQZ | $\overline{OE}$ high to high Z | 12 | 15 | 15 | 20 | ns | max |

* Preliminary specification

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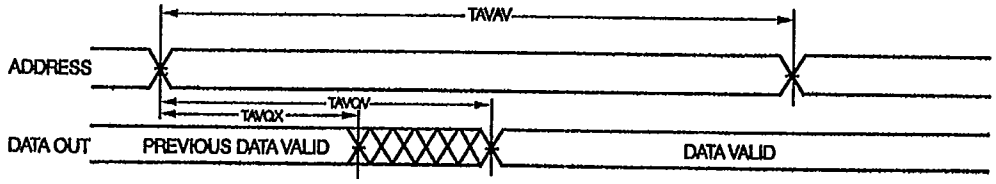
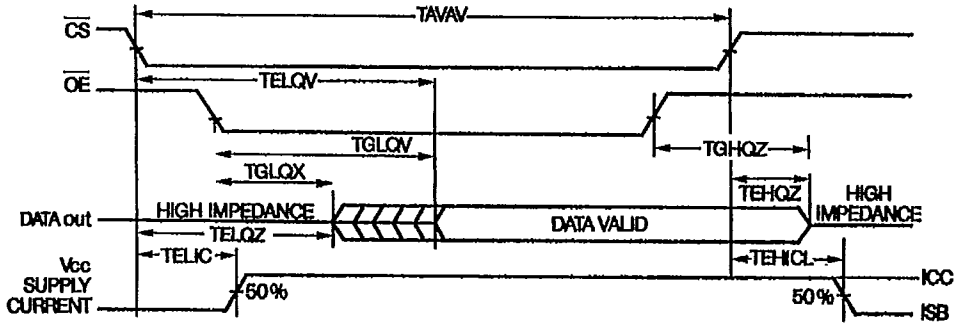
## READ CYCLE nb 1




## READ CYCLE nb 2

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## ORDERING INFORMATION

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| Package | Device type | Grade | Level |
|---|---|---|---|
| HM1 | 65728 (A) | H | – 5 : R |

- Package:
  - 0 - Chip form
  - 1 - Ceramic 24 pins
  - 3 - Plastic 24 pins 300 mils
  - 3E - Plastic 24 pins 600 mils
  - 4 - LCC 32 pins
  - T - SOIC 24 pins
- Device type: 2 k x 8 high speed static RAM
- Grade:
  - F = 20 ns
  - H = 25 ns
  - K = 35 ns
  - M = 45 ns
  - N = 55 ns
- Level:
  - – 5 : Commercial
  - – 2 : Military
  - – 8 : Military with B.I.

  (B.I. = Burn-In)
- : R — Tape and Reel Service

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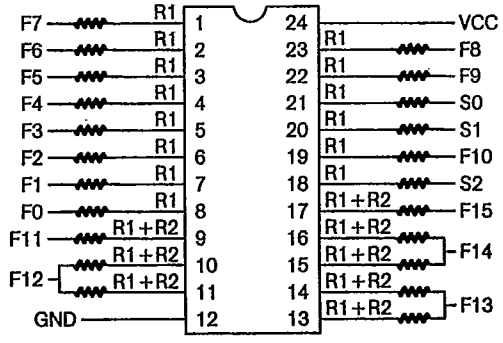
## PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

The reference are : Plastic DIL, 300 mils, 24 pins
Plastic DIL, 600 mils, 24 pins
SOIC DIL, 300 mils, 24 pins
Ceramic, 300 mils, 24 pins
LCC rectangular, 32 pins

## BURN-IN SCHEMATICS




R1 = 220 Ω per row

R2 = 2.2 K Ω per driver

FO = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write/read cycles

VCC = 5.5 V