

# SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379

## OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

SDLS167 – OCTOBER 1976 – REVISED MARCH 1988

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

### description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input  $\bar{G}$  is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the  $\bar{G}$  input.

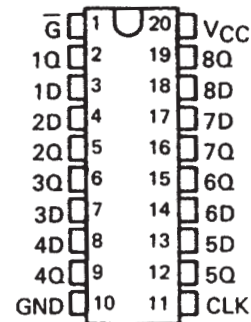
These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

**FUNCTION TABLE**  
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\bar{G}$	CLOCK	DATA	Q	$\bar{Q}$
H	X	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

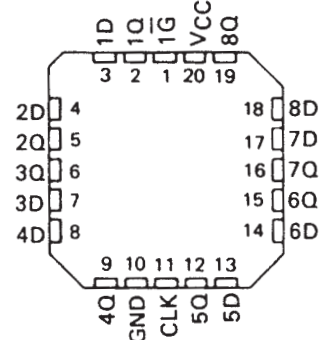
**SN54LS377 . . . J PACKAGE**  
**SN74LS377 . . . DW OR N PACKAGE**

(TOP VIEW)



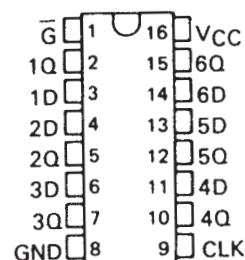
**SN54LS377 . . . FK PACKAGE**

(TOP VIEW)



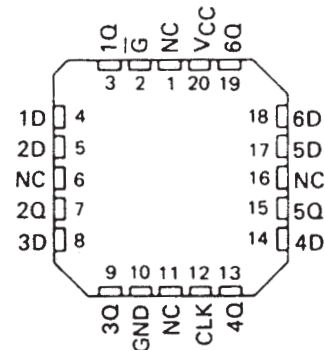
**SN54LS378 . . . J OR W PACKAGE**  
**SN74LS378 . . . D OR N PACKAGE**

(TOP VIEW)



**SN54LS378 . . . FK PACKAGE**

(TOP VIEW)



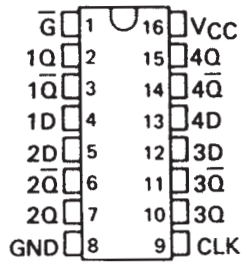
NC – No internal connection

# SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

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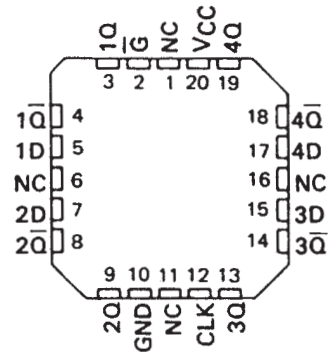
SN54LS379 . . . J OR W PACKAGE  
SN74LS379 . . . D OR N PACKAGE

(TOP VIEW)



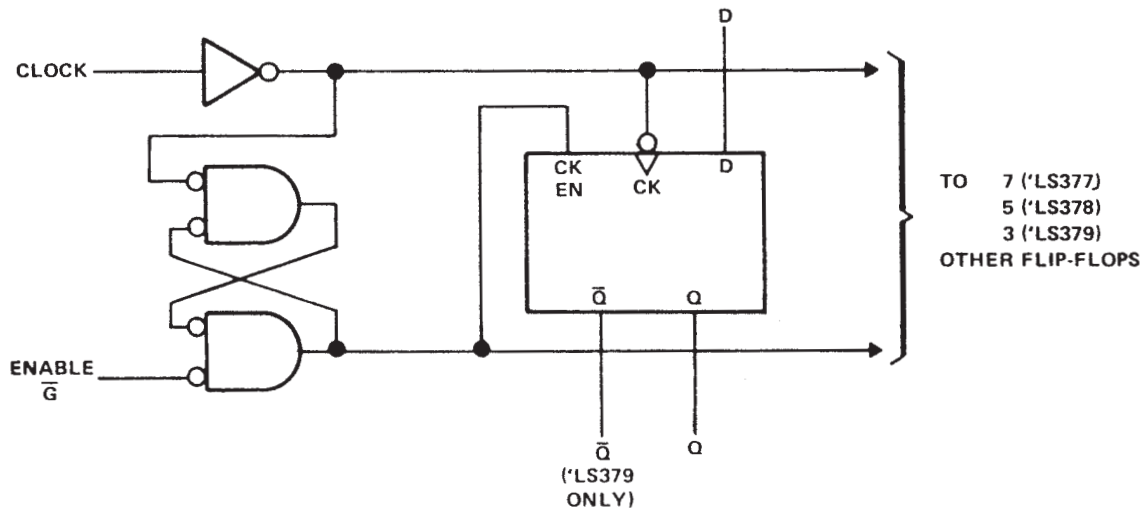
SN54LS379 . . . FK PACKAGE

(TOP VIEW)

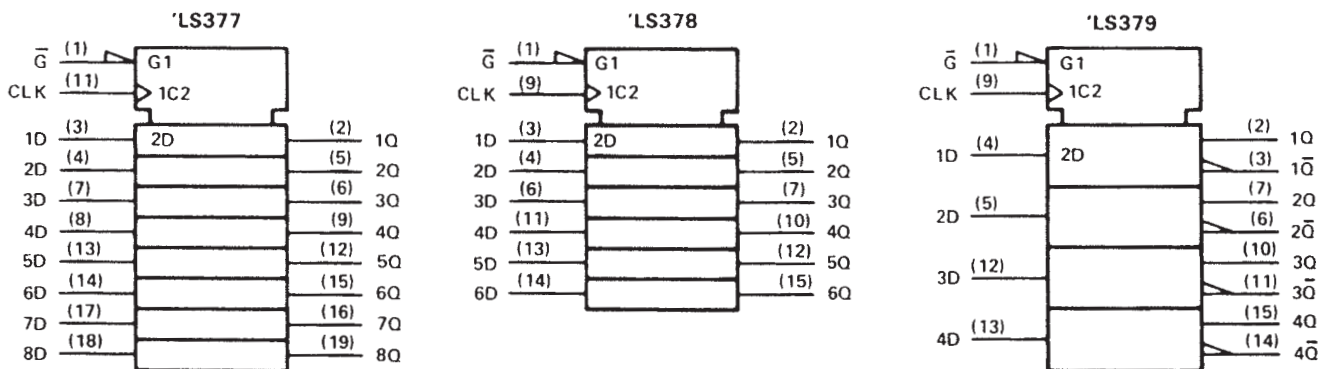


NC – No internal connection

logic diagram (positive logic)



logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, and N packages.

SN54LS377, SN54LS378, SN54LS379,  
SN74LS377, SN74LS378, SN74LS379  
OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

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schematics of inputs and outputs



**absolute maximum rating over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN54LS377, SN54LS378, SN54LS379, SN74LS377, SN74LS378, SN74LS379 OCTAL, HEX, AND QUAD D-TYPE FLIP-FLOPS WITH ENABLE

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## recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Clock frequency, $f_{clock}$	0		30	0		30	MHz
Width of clock pulse, $t_W$	20			20			ns
Setup time, $t_{su}$	Data input	20†		20†			ns
	Enable active-state	25†		25†			
	Enable inactive-state	10†		10†			
Hold time, $t_h$	Data and enable	5†		5†			ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

† The arrow indicates that the rising edge of the clock pulse is used for reference.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage				0.7			0.8	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$			0.25	0.4		0.25	0.4	V
	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$						0.35	0.5	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu$ A	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA	
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS377	17	28	17	28		mA	
		'LS378	13	22	13	22		mA	
		'LS379	9	15	9	15		mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and ground applied to all data and enable inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF},$	30	40		MHz
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock	$R_L = 2 \text{ k}\Omega$		17	27	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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## SN54LS377, Octal D-type Flip-Flops With Enable

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS377	SN74LS377
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	8	8
Static Current		28
th (ns)		5
tpd max (ns)		27
tsu (ns)		20

### FEATURES

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### DESCRIPTION

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- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
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- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
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- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

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ORDERABLE DEVICE	STATUS	PACKAGE TYPE   PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY   SUS	STD PACK QTY	IN STOCK	IN PROGRESS QTY   DATE	LEAD TIME	DISTRIBUTOR COMPANY   REGION	IN STOCK	PURCHASE
JM38510/32504B2A	ACTIVE	LCCC (FK)   20	-55 TO 125		<a href="#">View Contents</a>	1KU   8.37	1	23*	3712   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		
									> 10k   27 May				
JM38510/32504BRA	ACTIVE	CDIP (J)   20	-55 TO 125		<a href="#">View Contents</a>	1KU   3.00	1	615*	26   06 May	6 WKS	<a href="#">Avnet</a>   Americas	323	<a href="#">BUY NOW</a>
									> 10k   20 May				
JM38510/32504BSA	ACTIVE	CFP (W)   20	-55 TO 125		<a href="#">View Contents</a>	1KU   7.87	1	90*	> 10k   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		
SN54LS377J	ACTIVE	CDIP (J)   20	-55 TO 125		<a href="#">View Contents</a>	1KU   1.70	1	2139*	903   06 May	6 WKS	<a href="#">EBV Elektronik</a>   Europe	900	<a href="#">BUY NOW</a>
									> 10k   20 May		<a href="#">Avnet</a>   Americas	133	<a href="#">BUY NOW</a>
SNJ54LS377FK	ACTIVE	LCCC (FK)   20	-55 TO 125		<a href="#">View Contents</a>	1KU   7.87	1	271*	3580   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		

									> 10k   27 May				
SNJ54LS377J	ACTIVE	<a href="#">CDIP (J)</a>   20	-55 TO 125		<a href="#">View Contents</a>	1KU   2.00	1	<b>88*</b>	> 10k   20 May	6 WKS	<a href="#">Avnet</a>   Americas	82	<b>BUY NOW</b>
											<a href="#">Avnet-SILICA</a>   Europe	81	<b>BUY NOW</b>
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SNJ54LS377W	ACTIVE	<a href="#">CFP (W)</a>   20	-55 TO 125		<a href="#">View Contents</a>	1KU   7.87	1	<b>68*</b>	> 10k   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		

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## SN54LS378, Hex D-type Flip-Flops With Enable

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LS378	SN74LS378
Voltage Nodes (V)	5	5
Vcc range (V)	4.5 to 5.5	4.75 to 5.25
Input Level	TTL	TTL
Output Level	TTL	TTL
Output Drive (mA)		-0.4/8
Output	2S	2S
No. of Bits	6	6
Static Current		22
th (ns)		5
tpd max (ns)		27
tsu (ns)		20

### FEATURES

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- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
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5962-8992501EA	ACTIVE	CDIP (J)   16	-55 TO 125		<a href="#">View Contents</a>	1KU   2.00	1	41*	>10k   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		
SN54LS378J	ACTIVE	CDIP (J)   16	-55 TO 125		<a href="#">View Contents</a>	1KU   1.49	1	26*	>10k   20 May	6 WKS	<a href="#">EBV Elektronik</a>   Europe	150	<b>BUY NOW</b>
											<a href="#">Avnet</a>   Americas	17	<b>BUY NOW</b>
SNJ54LS378FK	OBSOLETE	LCCC (FK)   20	-55 TO 125		<a href="#">View Contents</a>	1KU		0*		Call**	None Reported <a href="#">View Distributors</a>		
SNJ54LS378J	ACTIVE	CDIP (J)   16	-55 TO 125	5962-8992501EA	<a href="#">View Contents</a>	1KU   2.00	1	196*	>10k   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		
SNJ54LS378W	ACTIVE	CFP (W)   16	-55 TO 125	5962-8992501FA	<a href="#">View Contents</a>	1KU   7.15	1	0*	>10k   20 May	6 WKS	None Reported <a href="#">View Distributors</a>		

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