

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74VHCT74AF, TC74VHCT74AFT

### Dual D-Type Flip-Flop with Preset and Clear

The TC74VHCT74 is an advanced high speed CMOS D-TYPE FLIP –FLOP fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.

The input voltage are compatible with TTL output voltage.

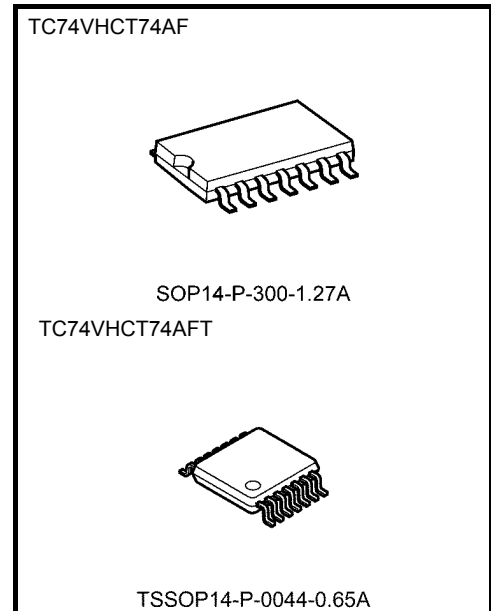
This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output <sup>(Note)</sup> pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

Note:  $V_{CC} = 0 V$

### Features

- High speed:  $f_{max} = 160 \text{ MHz (typ.)}$  at  $V_{CC} = 5 V$
- Low power dissipation:  $I_{CC} = 2 \mu A \text{ (max)}$  at  $T_a = 25^\circ C$
- Compatible with TTL inputs:  $V_{IL} = 0.8 V \text{ (max)}$   
 $V_{IH} = 2.0 V \text{ (min)}$
- Power down protection is provided on all inputs and outputs
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 74 type.



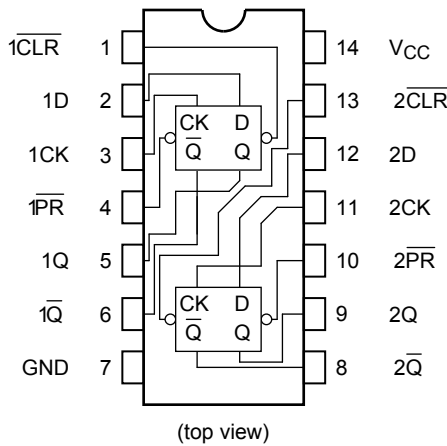
Weight

SOP14-P-300-1.27A: 0.18 g (typ.)

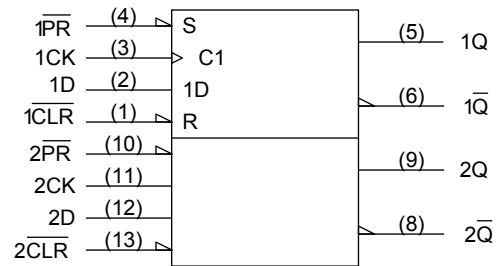
TSSOP14-P-0044-0.65A: 0.06 g (typ.)

Start of commercial production  
1995-12

**Pin Assignment**



**IEC Logic Symbol**



**Truth Table**

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↓	H	L	—
H	H	X	↔	Q <sub>n</sub>	Q̄ <sub>n</sub>	No Change

X: Don't care

**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5 to 7.0 (Note 2)	V
		-0.5 to V <sub>CC</sub> + 0.5 (Note 3)	
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20 (Note 4)	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: V<sub>CC</sub> = 0 V

Note 3: High or low state. I<sub>OUT</sub> absolute maximum rating must be observed.

Note 4: V<sub>OUT</sub> < GND, V<sub>OUT</sub> > V<sub>CC</sub>

## Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to 5.5 (Note 2)	V
		0 to $V_{CC}$ (Note 3)	
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 20	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 2:  $V_{CC} = 0$  V

Note 3: High or low state

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit		
			$V_{CC}$ (V)	Min	Typ.	Max	Min		Max	
High-level input voltage	$V_{IH}$	—	4.5 to 5.5	2.0	—	—	2.0	—	V	
Low-level input voltage	$V_{IL}$	—	4.5 to 5.5	—	—	0.8	—	0.8	V	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$	4.5	4.40	4.50	—	4.40	—	V
			$I_{OH} = -8 \text{ mA}$	4.5	3.94	—	—	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 8 \text{ mA}$	4.5	—	—	0.36	—	0.44	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	$\mu\text{A}$	
	$I_{CCT}$	Per input: $V_{IN} = 3.4 \text{ V}$ Other input: $V_{CC}$ or GND	5.5	—	—	1.35	—	1.50	mA	
Output leakage current	$I_{OPD}$	$V_{OUT} = 5.5 \text{ V}$	0	—	—	0.5	—	5.0	$\mu\text{A}$	

### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit	
			V <sub>CC</sub> (V)	Limit		
Minimum pulse width (CK)	$t_w$ (L) $t_w$ (H)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_w$ (L)	—	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time	$t_s$	—	5.0 ± 0.5	5.0	5.0	ns
Minimum hold time	$t_h$	—	5.0 ± 0.5	0.0	0.0	ns
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	$t_{\text{rem}}$	—	5.0 ± 0.5	3.5	3.5	ns

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (CK-Q, $\overline{\text{Q}}$ )	$t_{\text{pLH}}$	—	5.0 ± 0.5	15	—	5.8	7.8	1.0	9.0	ns
	$t_{\text{pHL}}$			50	—	6.3	8.8	1.0	10.0	
Propagation delay time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ -Q, $\overline{\text{Q}}$ )	$t_{\text{pLH}}$	—	5.0 ± 0.5	15	—	7.6	10.4	1.0	12.0	ns
	$t_{\text{pHL}}$			50	—	8.1	11.4	1.0	13.0	
Maximum clock frequency	$f_{\text{max}}$	—	5.0 ± 0.5	15	100	160	—	80	—	MHz
				50	80	140	—	65	—	
Input capacitance	C <sub>IN</sub>	—		—	4	10	—	10	pF	
Power dissipation capacitance	C <sub>PD</sub>	(Note)		—	24	—	—	—	pF	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

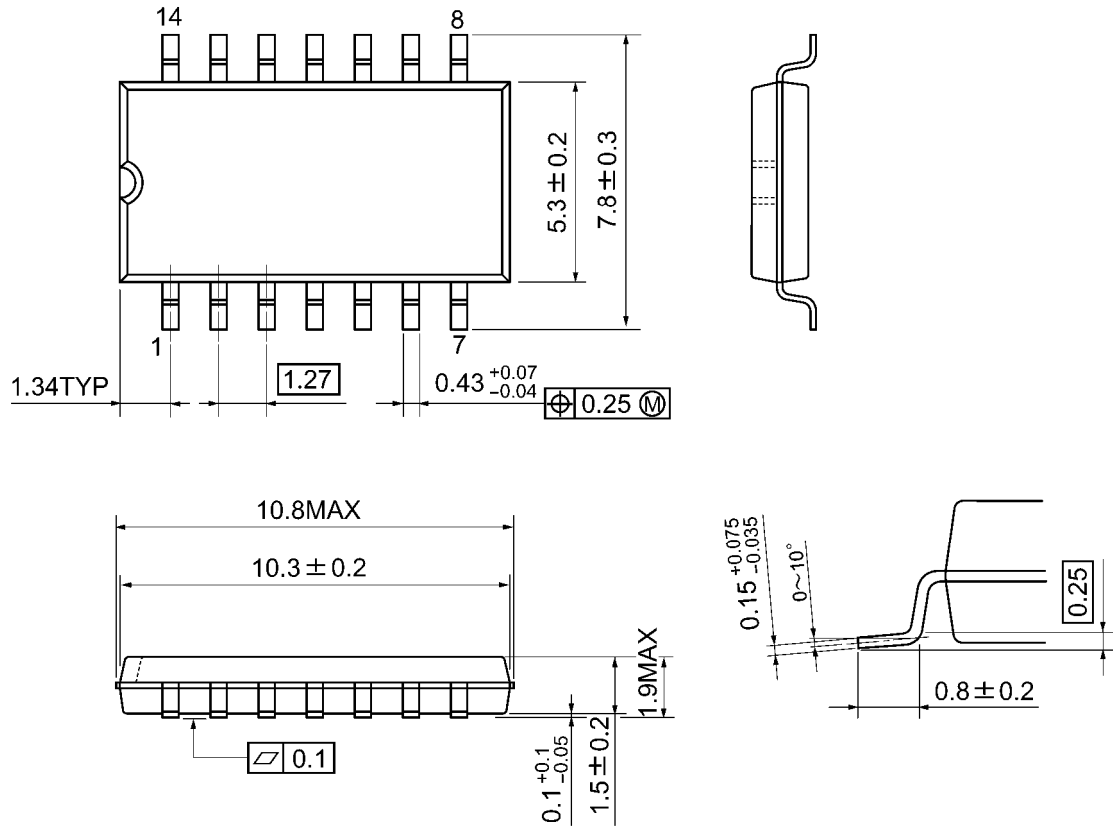
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/2 \text{ (per F/F)}$$

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm

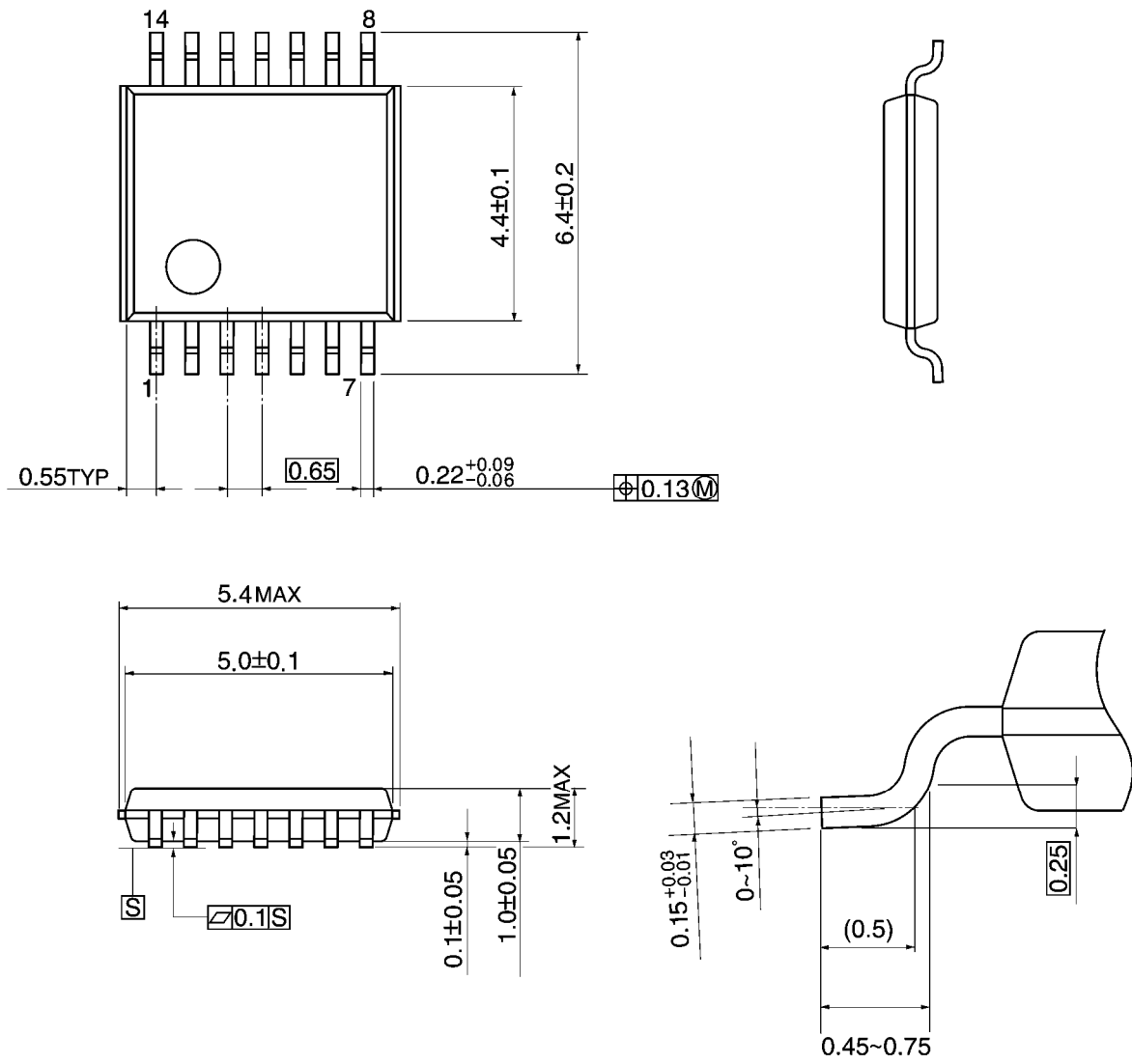


Weight: 0.18 g (typ.)

**Package Dimensions**

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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