

Low Frequency Timing-Safe™ Peak EMI reduction IC

General Features

- Low Frequency Clock distribution with Timing-Safe™ Peak EMI Reduction
- Input frequency range: 4MHz - 20MHz.
- Zero input - output propagation delay
- Low-skew outputs
 - Output-output skew less than 250pS
 - Device-device skew less than 700pS
- Less than 200pS cycle-to-cycle jitter
- Available in 8pin, 150 mil SOIC, 4.4mm TSSOP Package
- 3.3V Operation
- Industrial temperature range
- Advanced CMOS technology
- The First True Drop-in Solution

eight-pin version and accepts one reference input and drives out one low-skew clock.

All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad, internal to the device.

Multiple ASM3P622S01B/J devices can accept the same input clock and distribute it. In this case, the skew between the outputs of the two devices is guaranteed to be less than 700pS.

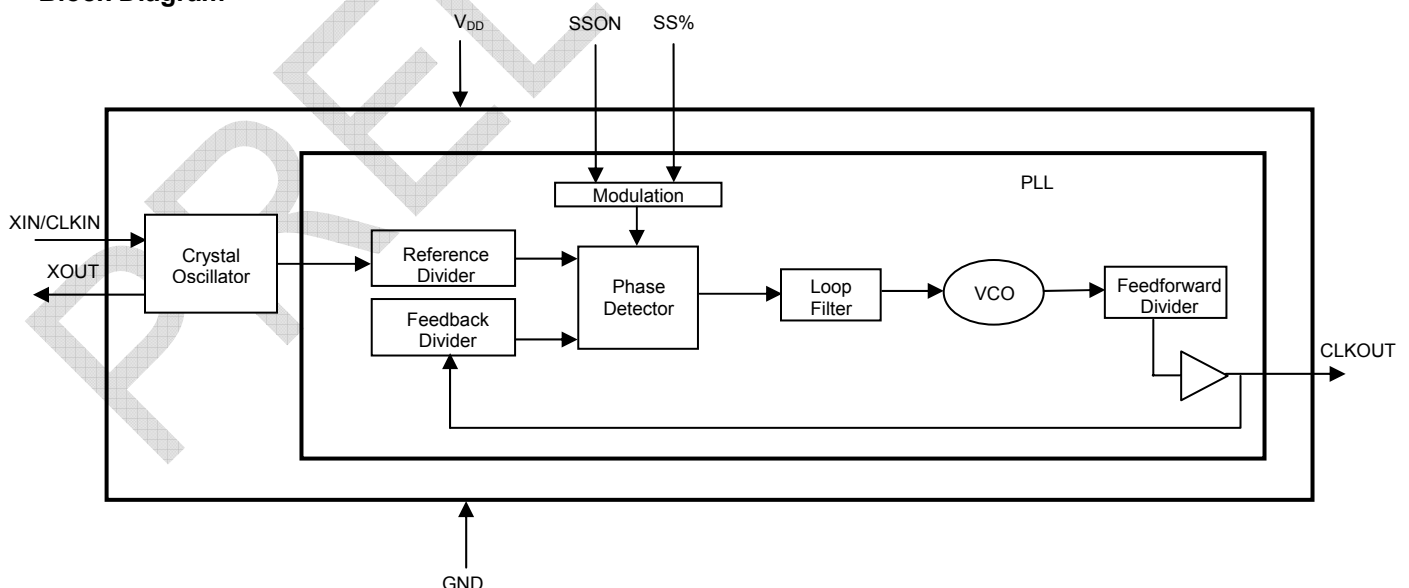
The output has less than 200pS of cycle-to-cycle jitter. The input and output propagation delay is guaranteed to be less than 250pS, and the output-to-output skew is guaranteed to be less than 250pS.

Functional Description

ASM3P622S01B/J is a versatile, 3.3V Zero-delay buffer designed to distribute low frequency Timing-Safe™ clocks with Peak EMI Reduction. The ASM3P622S01B/J is the

Refer “Spread Spectrum Control and Input-Output Skew Table” for deviations and Input-Output Skew for ASM3P622S01B/J devices.

Block Diagram



Spread Spectrum Frequency Generation

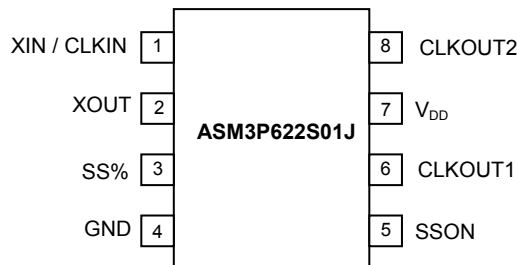
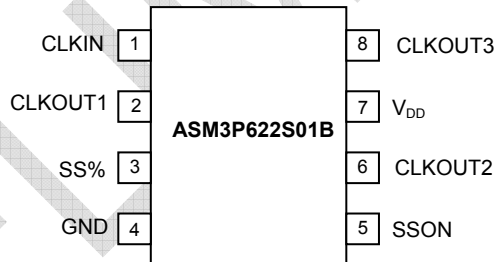
The clocks in digital systems are typically square waves with a 50% duty cycle and as frequencies increase the edge rates also get faster. Analysis shows that a square wave is composed of fundamental frequency and harmonics. The fundamental frequency and harmonics generate the energy peaks that become the source of EMI. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact, the peak level allowed decreases as the frequency increases. The standard methods of reducing EMI are to use shielding, filtering, multi-layer

PCBs etc. These methods are expensive. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. The ASM3P622S01B/J uses the center modulation spread spectrum technique in which the modulated output frequency varies above and below the reference frequency with a specified modulation rate. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation.

Timing-Safe™ technology

Timing-Safe™ technology is the ability to modulate a clock source with Spread Spectrum technology and maintain synchronization with any associated data path.

Pin Configuration



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Pin Description for ASM3P622S01B

| Pin # | Pin Name | Description |
|-------|----------------------|---|
| 1 | CLKIN | Input reference frequency, 5V-tolerant input |
| 2 | CLKOUT1 ¹ | Buffered clock output |
| 3 | SS% ² | Spread Spectrum Selection |
| 4 | GND | Ground |
| 5 | SSON ² | Spread Spectrum enable and disable option When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. |
| 6 | CLKOUT2 ¹ | Buffered clock output |
| 7 | V _{DD} | 3.3V supply |
| 8 | CLKOUT3 ¹ | Buffered clock output |

- Notes: 1. Weak pull-down on all outputs.
 2. Weak pull-up on these Inputs.
 3. Buffered clock outputs are Timing-Safe™

Pin Description for ASM3P622S01J

| Pin # | Pin Name | Description |
|-------|---------------------|--|
| 1 | XIN/CLKIN | Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. |
| 2 | XOUT | Crystal connection. If using an external reference, this pin must be left unconnected. |
| 3 | SS% ² | Spread Spectrum Selection |
| 4 | GND | Ground |
| 5 | SSON ² | Spread Spectrum enable and disable option When SSON is HIGH, the spread spectrum is enabled and when LOW, it turns off the spread spectrum. |
| 6 | CLKOUT ¹ | Buffered clock output |
| 7 | V _{DD} | 3.3V supply |
| 8 | CLKOUT ¹ | Buffered clock output |

- Notes: 1. Weak pull-down on all outputs
 2. Weak pull-up on these Inputs
 3. Buffered clock outputs are Timing-Safe™

Spread Spectrum Control and Input-Output Skew Table

| Device | Input Frequency | SS % | Deviation | Input-Output Skew(±T _{SKREW}) |
|----------------|-----------------|------|-----------|---|
| ASM3P622S01B/J | 12MHz | 0 | ±0.25 % | 0.063 |
| | | 1 | ±0.50 % | 0.125 |

Note: T_{SKREW} is measured in units of the Clock Period

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Unit |
|------------------|---|--------------|------|
| V _{DD} | Voltage on any pin with respect to Ground | -0.5 to +4.6 | V |
| T _{STG} | Storage temperature | -65 to +125 | °C |
| T _s | Max. Soldering Temperature (10 sec) | 260 | °C |
| T _J | Junction Temperature | 150 | °C |
| T _{DV} | Static Discharge Voltage (As per JEDEC STD22- A114-B) | 2 | KV |

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions for ASM3P622S01B/J Device

| Parameter | Description | Min | Max | Unit |
|-----------------|---|-----|-----|------|
| V _{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | -40 | +85 | °C |
| C _L | Load Capacitance | | 30 | pF |
| C _{IN} | Input Capacitance | | 7 | pF |

Electrical Characteristics for ASM3P622S01B/J

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------------------|-----------------------------------|-----|-----|-----|------|
| V _{IL} | Input LOW Voltage ¹ | | | | 0.8 | V |
| V _{IH} | Input HIGH Voltage ¹ | | 2.0 | | | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | | | 50 | µA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | | 100 | µA |
| V _{OL} | Output LOW Voltage ² | I _{OL} = 8mA | | | 0.4 | V |
| V _{OH} | Output HIGH Voltage ² | I _{OH} = -8mA | 2.4 | | | V |
| I _{DD} | Supply Current | Unloaded outputs | | 15 | | mA |
| Z _o | Output Impedance | | | 23 | | Ω |

Note: 1. CLKIN input has a threshold voltage of V_{DD}/2

2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Characteristics for ASM3P622S01B/J

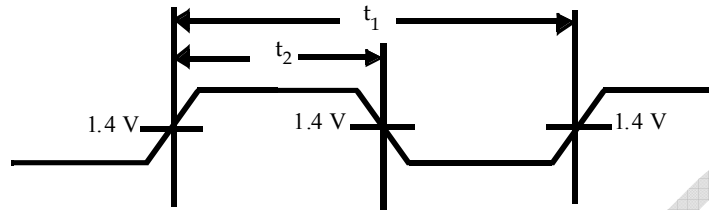
| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|------------|---|---|-----|-----|------|------|
| $1/t_1$ | Output Frequency | 30pF load | 4 | | 20 | MHz |
| | Duty Cycle ² = $(t_2 / t_1) * 100$ | Measured at $V_{DD}/2$ | 40 | 50 | 60 | % |
| t_3 | Output Rise Time ^{1, 2} | Measured between 0.8V and 2.0V | | | 2.5 | nS |
| t_4 | Output Fall Time ^{1, 2} | Measured between 2.0V and 0.8V | | | 2.5 | nS |
| t_5 | Output-to-output skew ² | All outputs equally loaded | | | 250 | pS |
| t_6 | Delay, CLKIN Rising Edge to CLKOUT Rising Edge ² | Measured at $V_{DD} / 2$ | | | ±250 | pS |
| t_7 | Device-to-Device Skew ² | Measured at $V_{DD}/2$ on the CLKOUT pins of the device | | | 700 | pS |
| t_J | Cycle-to-cycle jitter ² | Loaded outputs | | | 200 | pS |
| t_{LOCK} | PLL Lock Time ² | Stable power supply, valid clock presented on CLKIN pin | | | 1.0 | mS |

Note: 1. The parameters specified with loaded outputs.

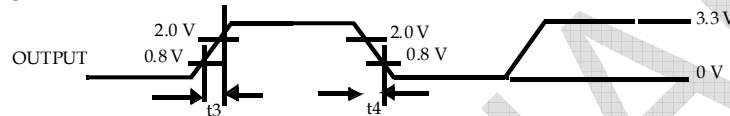
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Waveforms

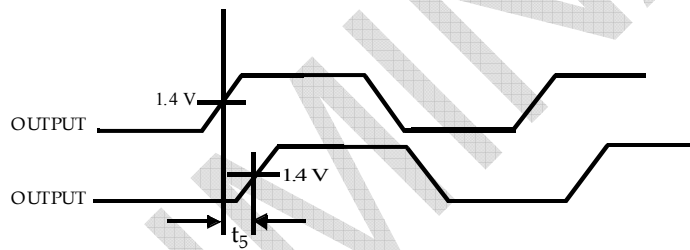
Duty Cycle Timing



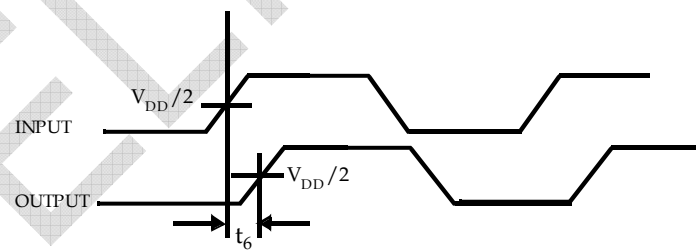
All Outputs Rise/Fall Time



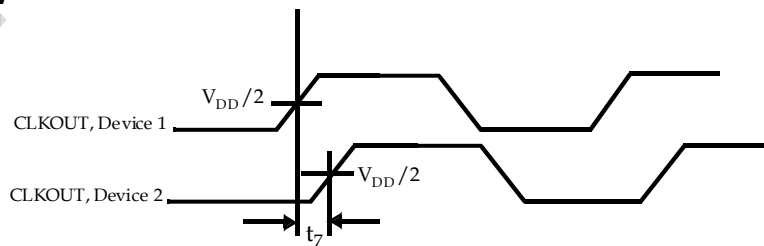
Output - Output Skew



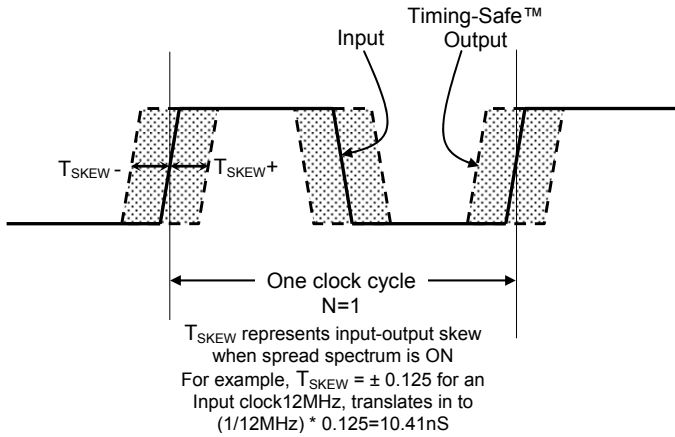
Input - Output Propagation Delay



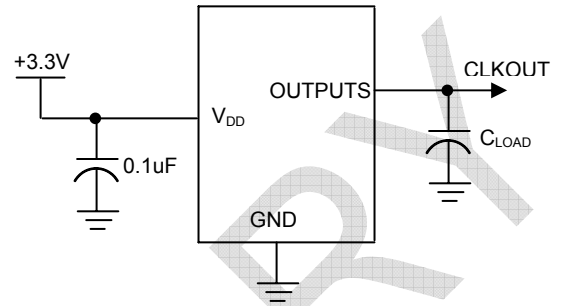
Device - Device Skew



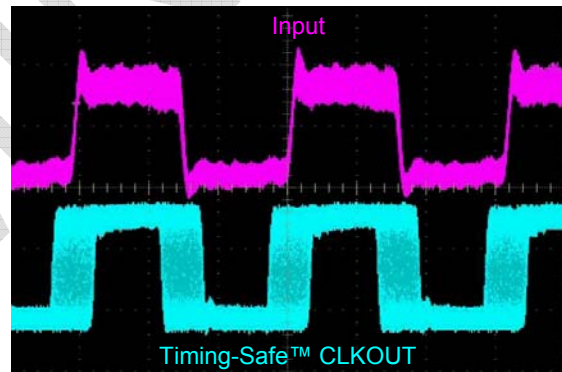
Input-Output Skew



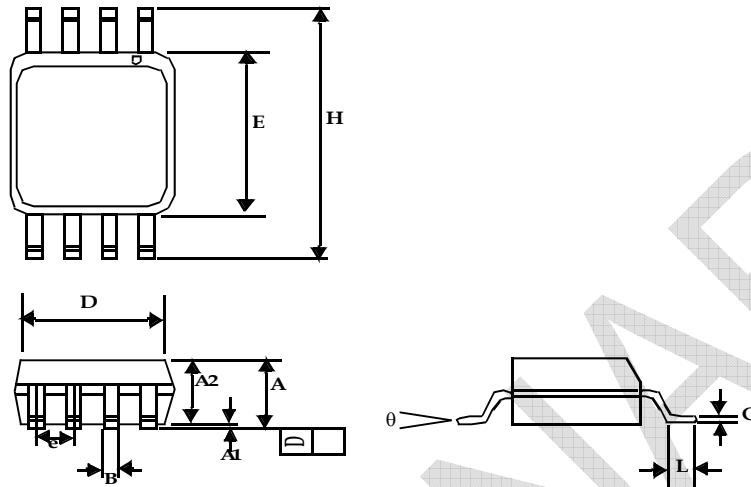
Test Circuit



A Typical example of Timing-Safe™ waveform

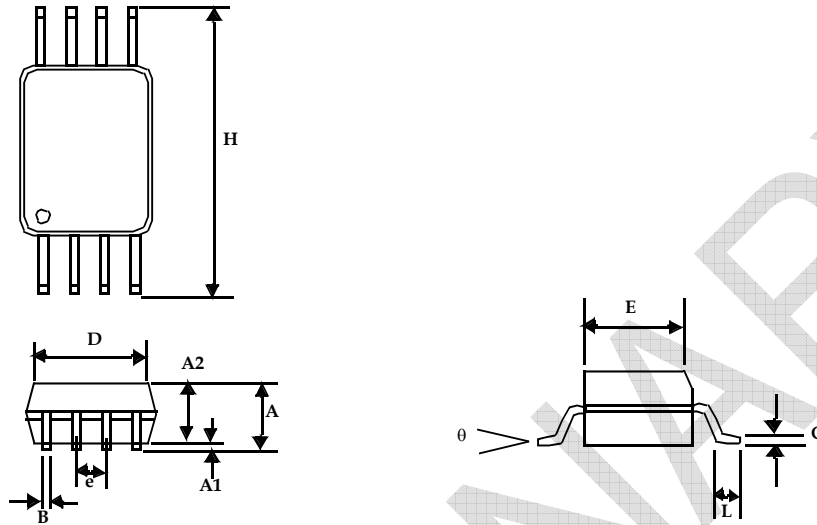


8-lead (150-mil) SOIC Package



| Symbol | Dimensions | | | |
|--------|------------|-------|-------------|------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A2 | 0.049 | 0.059 | 1.25 | 1.50 |
| B | 0.012 | 0.020 | 0.31 | 0.51 |
| C | 0.007 | 0.010 | 0.18 | 0.25 |
| D | 0.193 BSC | | 4.90 BSC | |
| E | 0.154 BSC | | 3.91 BSC | |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.236 BSC | | 6.00 BSC | |
| L | 0.016 | 0.050 | 0.41 | 1.27 |
| θ | 0° | 8° | 0° | 8° |

8-lead TSSOP (4.40-MM Body)



| Symbol | Dimensions | | | |
|--------|------------|-------|-------------|------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.043 | | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 |
| B | 0.008 | 0.012 | 0.19 | 0.30 |
| c | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.252 BSC | | 6.40 BSC | |
| L | 0.020 | 0.028 | 0.50 | 0.70 |
| theta | 0° | 8° | 0° | 8° |

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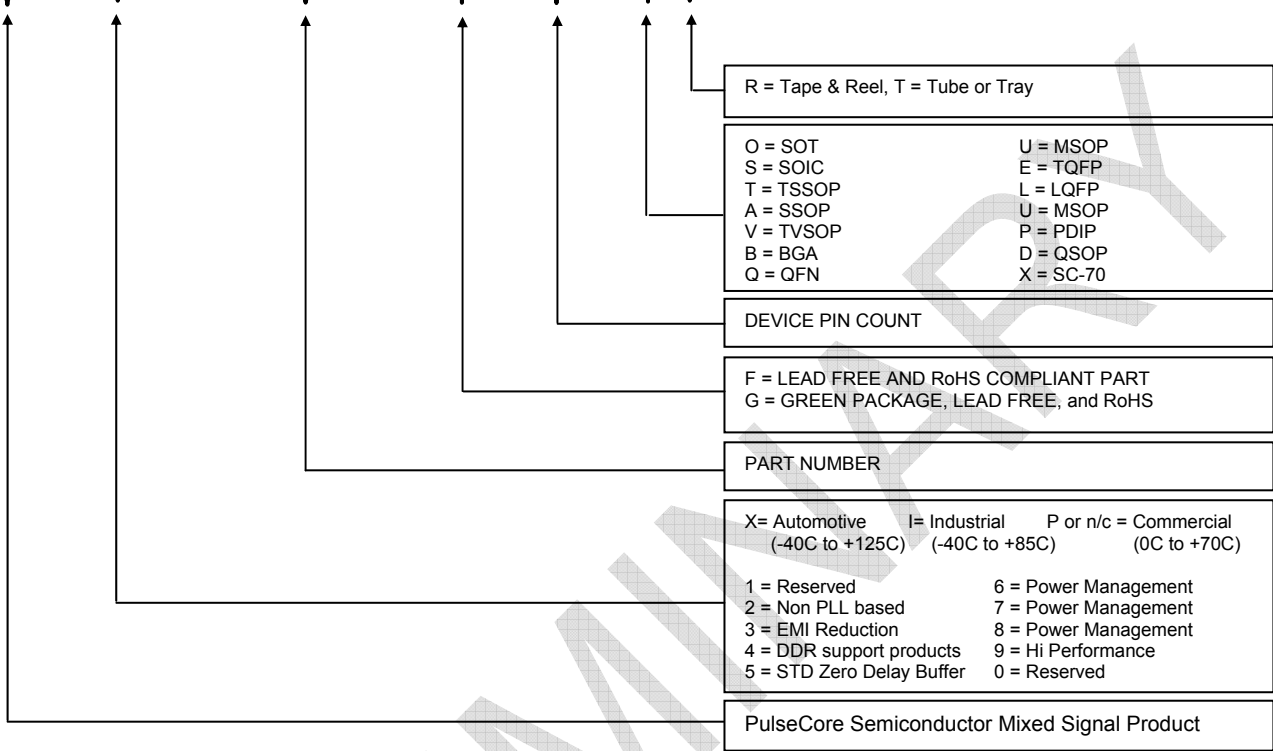
Ordering Codes

| Ordering Code | Marking | Package Type | Temperature |
|---------------------|------------|---|-------------|
| ASM3P622S01BF-08-ST | 3P622S01BF | 8-pin 150-mil SOIC-TUBE, Pb Free | Commercial |
| ASM3I622S01BF-08-ST | 3I622S01BF | 8-pin 150-mil SOIC-TUBE, Pb Free | Industrial |
| ASM3P622S01BF-08-SR | 3P622S01BF | 8-pin 150-mil SOIC-TAPE & REEL, Pb Free | Commercial |
| ASM3I622S01BF-08-SR | 3I622S01BF | 8-pin 150-mil SOIC-TAPE & REEL, Pb Free | Industrial |
| ASM3P622S01BF-08-TT | 3P622S01BF | 8-pin 4.4-mm TSSOP - TUBE, Pb Free | Commercial |
| ASM3I622S01BF-08-TT | 3I622S01BF | 8-pin 4.4-mm TSSOP - TUBE, Pb Free | Industrial |
| ASM3P622S01BF-08-TR | 3P622S01BF | 8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free | Commercial |
| ASM3I622S01BF-08-TR | 3I622S01BF | 8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free | Industrial |
| ASM3P622S01BG-08-ST | 3P622S01BG | 8-pin 150-mil SOIC-TUBE, Green | Commercial |
| ASM3I622S01BG-08-ST | 3I622S01BG | 8-pin 150-mil SOIC-TUBE, Green | Industrial |
| ASM3P622S01BG-08-SR | 3P622S01BG | 8-pin 150-mil SOIC-TAPE & REEL, Green | Commercial |
| ASM3I622S01BG-08-SR | 3I622S01BG | 8-pin 150-mil SOIC-TAPE & REEL, Green | Industrial |
| ASM3P622S01BG-08-TT | 3P622S01BG | 8-pin 4.4-mm TSSOP - TUBE, Green | Commercial |
| ASM3I622S01BG-08-TT | 3I622S01BG | 8-pin 4.4-mm TSSOP - TUBE, Green | Industrial |
| ASM3P622S01BG-08-TR | 3P622S01BG | 8-pin 4.4-mm TSSOP - TAPE & REEL, Green | Commercial |
| ASM3I622S01BG-08-TR | 3I622S01BG | 8-pin 4.4-mm TSSOP - TAPE & REEL, Green | Industrial |
| ASM3P622S01JF-08-ST | 3P622S01JF | 8-pin 150-mil SOIC-TUBE, Pb Free | Commercial |
| ASM3I622S01JF-08-ST | 3I622S01JF | 8-pin 150-mil SOIC-TUBE, Pb Free | Industrial |
| ASM3P622S01JF-08-SR | 3P622S01JF | 8-pin 150-mil SOIC-TAPE & REEL, Pb Free | Commercial |
| ASM3I622S01JF-08-SR | 3I622S01JF | 8-pin 150-mil SOIC-TAPE & REEL, Pb Free | Industrial |
| ASM3P622S01JF-08-TT | 3P622S01JF | 8-pin 4.4-mm TSSOP - TUBE, Pb Free | Commercial |
| ASM3I622S01JF-08-TT | 3I622S01JF | 8-pin 4.4-mm TSSOP - TUBE, Pb Free | Industrial |
| ASM3P622S01JF-08-TR | 3P622S01JF | 8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free | Commercial |
| ASM3I622S01JF-08-TR | 3I622S01JF | 8-pin 4.4-mm TSSOP - TAPE & REEL, Pb Free | Industrial |
| ASM3P622S01JG-08-ST | 3P622S01JG | 8-pin 150-mil SOIC-TUBE, Green | Commercial |
| ASM3I622S01JG-08-ST | 3I622S01JG | 8-pin 150-mil SOIC-TUBE, Green | Industrial |
| ASM3P622S01JG-08-SR | 3P622S01JG | 8-pin 150-mil SOIC-TAPE & REEL, Green | Commercial |
| ASM3I622S01JG-08-SR | 3I622S01JG | 8-pin 150-mil SOIC-TAPE & REEL, Green | Industrial |
| ASM3P622S01JG-08-TT | 3P622S01JG | 8-pin 4.4-mm TSSOP - TUBE, Green | Commercial |
| ASM3I622S01JG-08-TT | 3I622S01JG | 8-pin 4.4-mm TSSOP - TUBE, Green | Industrial |
| ASM3P622S01JG-08-TR | 3P622S01JG | 8-pin 4.4-mm TSSOP - TAPE & REEL, Green | Commercial |
| ASM3I622S01JG-08-TR | 3I622S01JG | 8-pin 4.4-mm TSSOP - TAPE & REEL, Green | Industrial |

rev 0.4

Device Ordering Information

A S M 3 P 6 2 2 S 0 1 B F - 0 8 - T R



PRELIMINARY

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



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Part Number: ASM3P622S01B/J
Document Version: 0.4

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Timing-Safe™ US Patent Pending.

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