

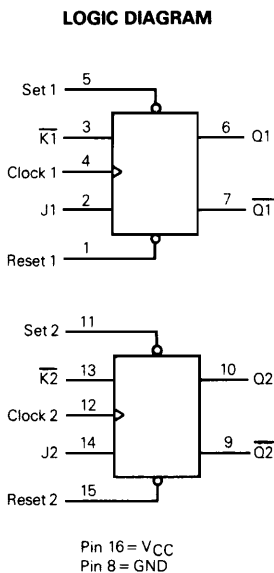
Dual J-K Flip-Flop with Set and Reset

High-Performance Silicon-Gate CMOS

The MC54/74HC109 is identical in pinout to the LS109. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two J-K flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q and \bar{Q} outputs are available from each flip-flop.

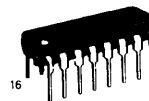
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 148 FETs or 37 Equivalent Gates



MC54/74HC109



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06



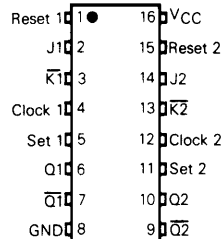
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = -55° to 125°C for all packages.
Dimensions in Chapter 6.

PIN ASSIGNMENT



FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↔	L	L	L	H
H	H	↔	H	L	Toggle	
H	H	↔	L	H	No Change	
H	H	↔	H	H	H	L
H	H	L	X	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MC54/74HC109

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating – Plastic DIP: -10 mW/°C from 65° to 125°C
Ceramic DIP: -10 mW/°C from 100° to 125°C
SOIC Package: -7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $ I_{out} \leq 20$ μ A	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	3.98	3.84	3.70	
			6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 20$ μ A	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		$V_{in} = V_{IH}$ or V_{IL} $ I_{out} \leq 4.0$ mA $ I_{out} \leq 5.2$ mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μ A
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0$ μ A	6.0	4	40	80	μ A

NOTE: Information on typical parametric values can be found in Chapter 4.

MC54/74HC109

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or \bar{Q} (Figures 1 and 4)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or \bar{Q} (Figures 2 and 4)	2.0	230	290	345	ns
		4.5	46	58	69	
		6.0	39	49	59	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Flip-Flop) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		40	

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, J or \bar{K} to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to J or \bar{K} (Figure 3)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

MC54/74HC109

SWITCHING WAVEFORMS

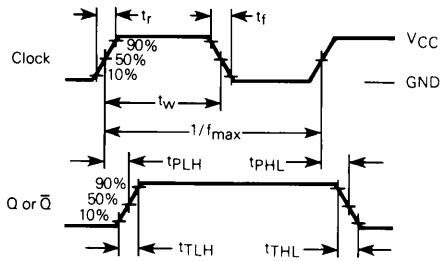


Figure 1.

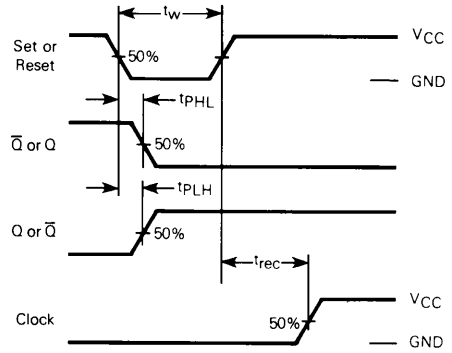


Figure 2.

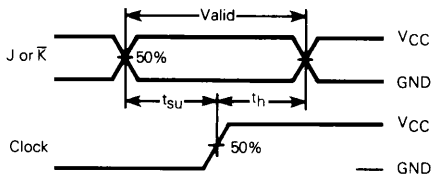
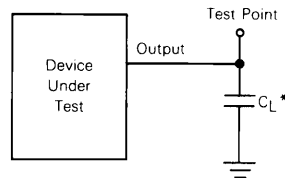


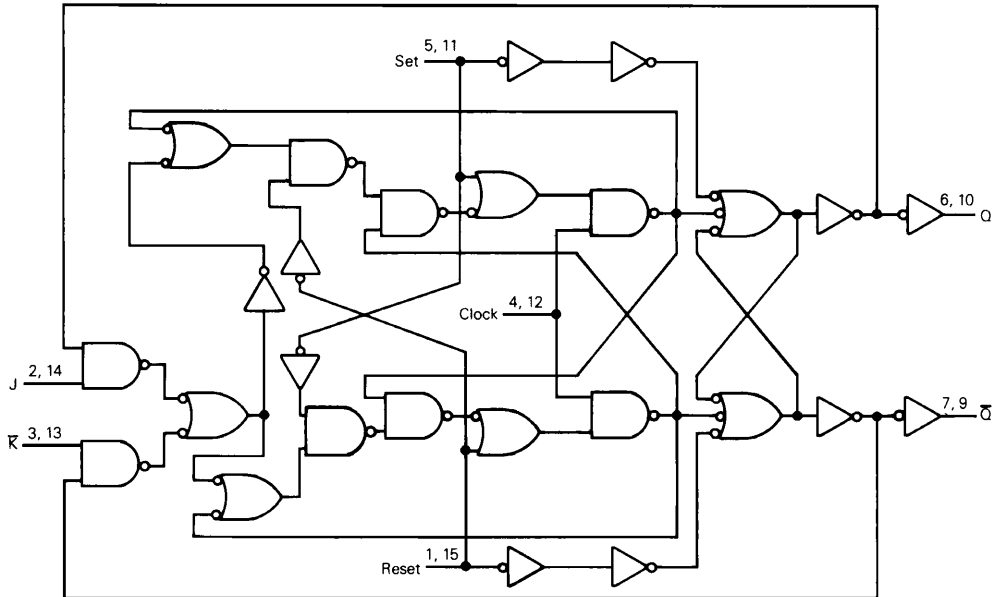
Figure 3.



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



5