HIGH GRADE Specification HIGH RELIABILITY series

Microwire BUS Serial EEPROMs

Supply voltage 2.7V~5.5V
Operating temperature –40°C~+125°C type

BR93H56-W, BR93H66-W, BR93H76-W, BR93H86-W

● Description

BR93H□□-W series is a serial EEPROM of serial 3-line interface method.

● Features

- ・ Withstands electrostatic voltage 8kV, (twice more than other series) (HBM method typ.)
- ・ Wide action range –40 ˚C ~ +125 ˚C
  (–40˚C ~ +85˚C, –40˚C ~ +105˚C in other series)
- • Conforming to Microwire BUS
- ・ Highly reliable connection by Au pad and Au wire
- • Address auto increment function at read action
- • Write mistake prevention function
  Write prohibition at power on
  Write prohibition by command code
  Write mistake prevention circuit at low voltage
- ・ Program cycle auto delete and auto end function
- ・ Program condition display by READY / $\overline{\text{BUSY}}$
- ・ Low current consumption
  At write action (5V) : 0.6mA (Typ.)
  At read action (5V) : 0.6mA (Typ.)
  At standby action (5V) : 0.1µA (Typ.)
- ・ Built-in noise filter CS, SK, DI terminals
- ・ Compact package SOP8, SOP-J8
- ・ High reliability by ROHM original Double-Cell structure
- ・ High reliability ultrafine CMOS process
- ・ Data rewrite up to 1,000,000 times
- ・ Data kept for 40 years• Easily connectable with serial port BR93H series
- ・ Data at shipment all addresses FFFFh

Capacity	Bit format	Type	Power source voltage	SOP8		SOP-J8		SSOP-B8		TSSOP-B8		MSOP8	TSSOP-B8J
Package type				F	RF	FJ	RFJ	FV	RFV	FVT	RFVT	RFVM	RFVJ
2Kbit	128 × 16	BR93H56-W	2.7V ~ 5.5V		●		●						
4Kbit	256 × 16	BR93H66-W	2.7V ~ 5.5V		●		●						
8Kbit	512 × 16	BR93H76-W	2.7V ~ 5.5V		●		●						
16Kbit	1K × 16	BR93H86-W	2.7V ~ 5.5V		●		●						

● Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Limits		Unit
Impressed voltage	VCC	-0.3 ~ +6.5		V
Permissible dissipation	Pd	SOP8 (RF)	450 (*1)	mW
		SOP-J8 (RFJ)	450 (*2)	
Storage temperature range	Tstg	-65 ~ +150		˚C
Action temperature range	Topr	-40 ~ +125		˚C
Terminal voltage	-	-0.3 ~ Vcc+0.3		V

* When using at Ta = 25˚C or higher, 3.6mW (*1, *2) to be reduced per 1˚C.

● Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	2.7 ~ 5.5	V
Input voltage	VIN	0 ~ VCC	V

● Electrical characteristics (Unless otherwise specified, Ta = -40 ~ +125˚C, Vcc = 2.7V ~ 5.5V)

Item	Symbol	Limits			Unit	Conditions	Measurement circuit
		Min.	Typ.	Max.			
"L" input voltage	VIL	-0.3	–	0.3× Vcc	V		
"H" input voltage	VIH	0.7× Vcc	–	Vcc +0.3	V		
"L" output voltage 1	VOL1	0	–	0.4	V	IOL=2.1mA,4.0 Vcc 5.5V	Fig. 4
"L" output voltage 2	VOL2	0	–	0.2	V	IOL=100µA	Fig. 4
"H" output voltage 1	VOH1	2.4	–	Vcc	V	IOH=−0.4mA,4.0 Vcc 5.5V	Fig. 5
"H" output voltage 2	VOH2	Vcc -0.2	–	Vcc	V	IOH=−100µA	Fig. 5
Input leak current	ILI	-10	–	10	µA	VIN=0 ~ Vcc	Fig. 6
Output leak current	ILO	-10	–	10	µA	VOUT=0 ~ Vcc,CS=0V	Fig. 7
Current consumption at operation	ICC1	–	–	3.0	mA	fSK=1.25MHz,tE/W=10ms (WRITE)	Fig. 8
	ICC2	–	–	1.5	mA	fSK=1.25MHz (READ)	Fig. 8
	ICC3	–	–	4.5	mA	fSK=1.25MHz,tE/W=10ms (WRAL)	Fig. 8
Standby current	ISB	–	0.1	10	µA	CS=0V,DO=OPEN	Fig. 9

○This IC is not designed to be radiation-resistant.

● Operation timing characteristics (Ta=-40˚C ~ +125˚C, Vcc=2.7V ~ 5.5V)

Item	Symbol	Min.	Typ.	Max.	Unit
SK frequency	fSK	–	–	1.25	MHz
SK "H" time	tSKH	250	–	–	ns
SK "L" time	tSKL	250	–	–	ns
CS "L" time	tCS	200	–	–	ns
CS setup time	tCSS	200	–	–	ns
DI setup time	tDIS	100	–	–	ns
CS hold time	tCSH	0	–	–	ns
DI hold time	tDIH	100	–	–	ns
Data "1" output delay time	tPD1	–	–	300	ns
Data "0" output delay time	tPD0	–	–	300	ns
Time from CS to output establishment	tSV	–	–	200	ns
Time from CS to High-Z	tDF	–	–	200	ns
Write cycle time	tE/W	–	7	10	ms

● Memory cell characteristics (Vcc=2.7V ~ 5.5V)

	Limits			Unit	Conditions
	Min.	Typ.	Max.		
Number of data rewrite times *1	1,000,000	–	–	Times	Ta 85˚C
	500,000	–	–	Times	Ta 105˚C
	300,000	–	–	Times	Ta 125˚C
Data hold years *1	40	–	–	Years	Ta 25˚C
	10	–	–	Years	Ta 50˚C

* 1 NOT 100%TESTED

● Sync data input / output timing

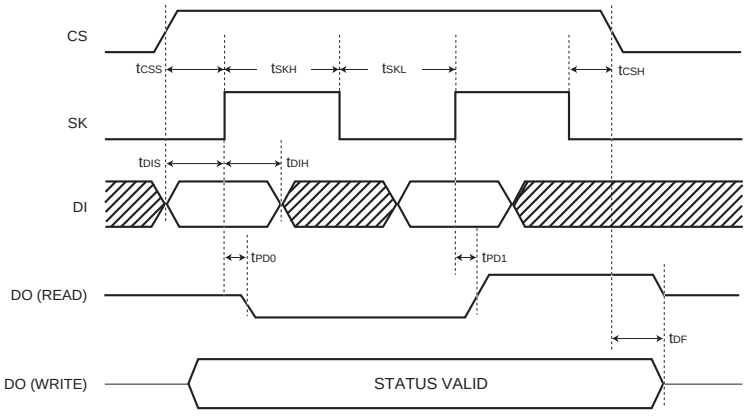


Fig.1 Sync data input / output timing diagram

○ Data is taken by DI in sync with the rise of SK.

○ At read action, data is output from DO in sync with the rise of SK.

○ The status signal at write (READY / $\overline{\text{BUSY}}$) is output after tCS from the fall of CS after write command input. This is at the DO area where CS is "H", and valid until the next command start bit is input. While CS is "L", DO becomes High-Z.

○ After each mode execution is competed, set CS to "L" once for internal circuit reset, and execute the following action mode.

● Characteristic data

The following characteristic data are Typ. values.

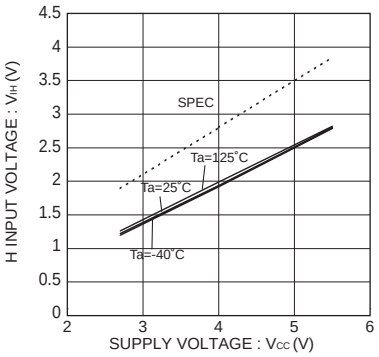


Fig.2 H input voltage VIH (CS,SK,DI)

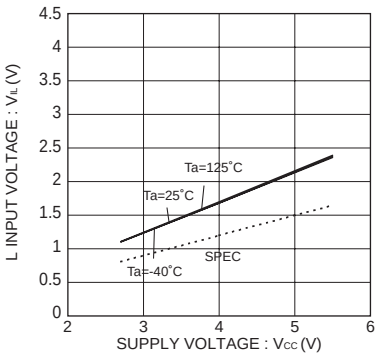


Fig.3 L input voltage VIL (CS,SK,DI)

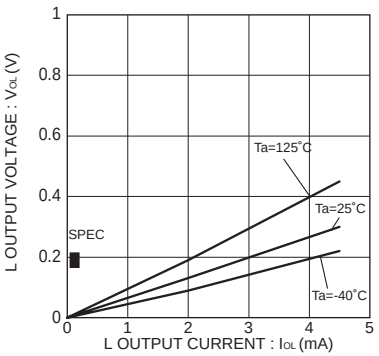


Fig.4 L output voltage VOL-IOL (VCC=2.7V)

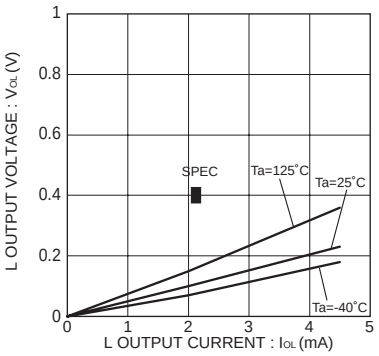


Fig.5 L output voltage VOL-IOL (VCC=4.0V)

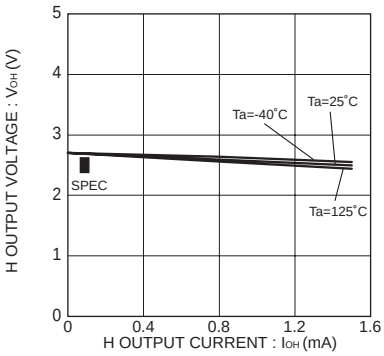


Fig.6 H output voltage VOH-IOH (VCC=2.7V)

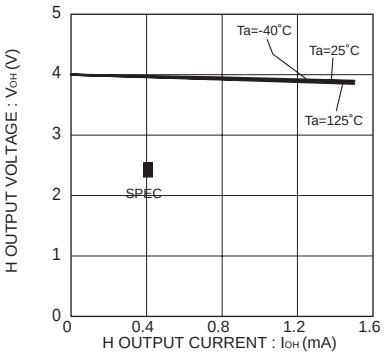


Fig.7 H output voltage VOH-IOH (VCC=4.0V)

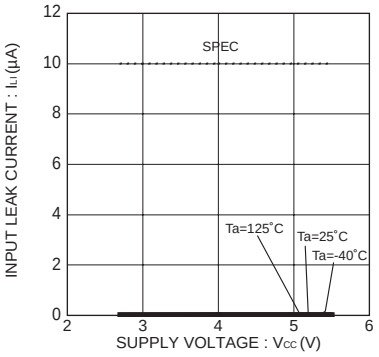


Fig.8 Input leak current ILI (CS,SK,DI)

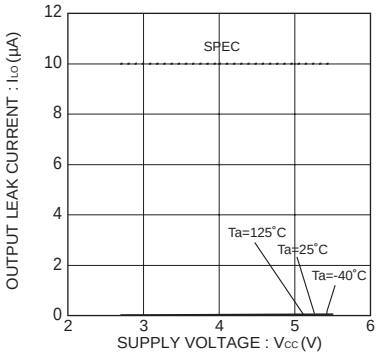


Fig.9 Output leak current ILO (DO)

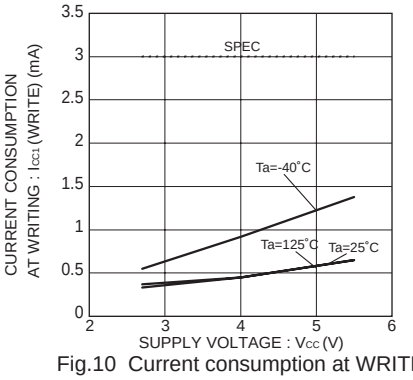


Fig.10 Current consumption at WRITE operation ICC1 (WRITE,fSK=1.25MHz)

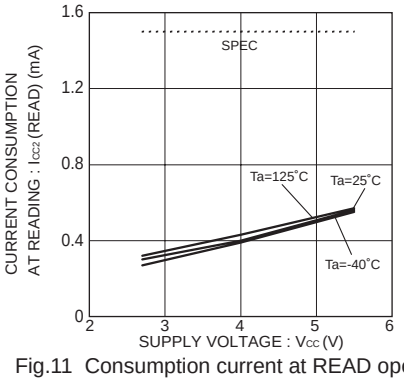


Fig.11 Consumption current at READ operation ICC2 (READ,fSK=1.25MHz)

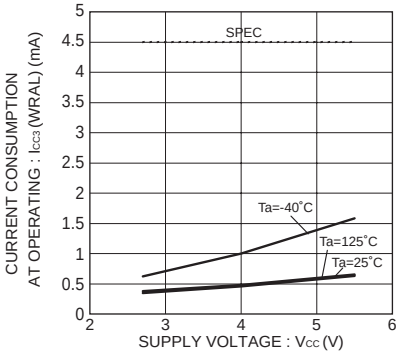


Fig.12 Consumption current at WRAL operation ICC3 (WRAL,fSK=1.25MHz)

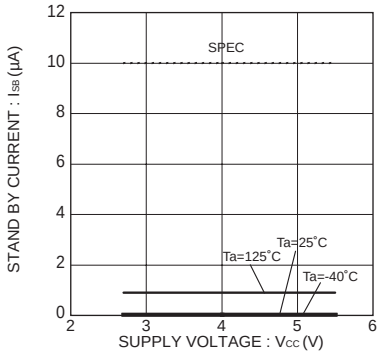


Fig.13 Consumption current at standby operation ISB

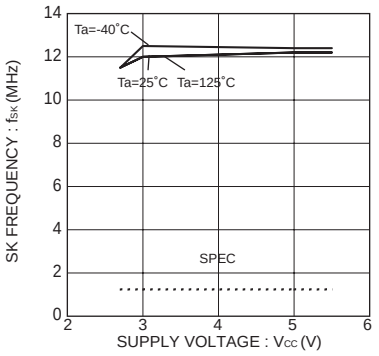


Fig.14 SK frequency fSK

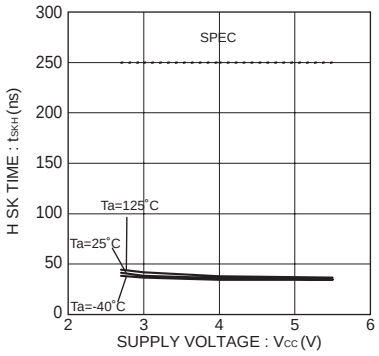


Fig.15 SK high time tSKH

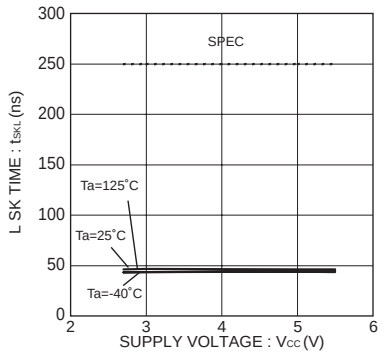


Fig.16 SK low time tSKL

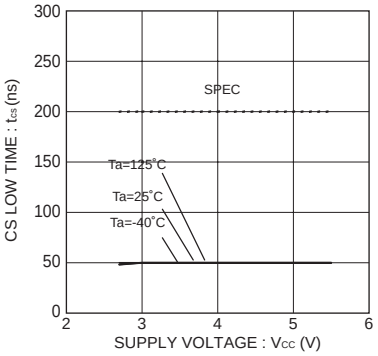


Fig.17 CS low time tCS

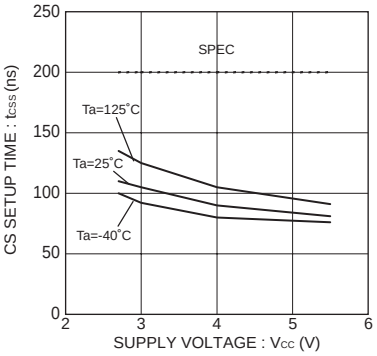


Fig.18 CS setup time tCSS

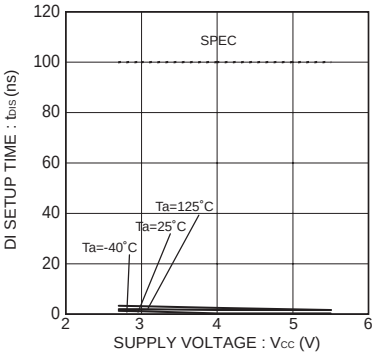


Fig.19 DI setup time tDIS

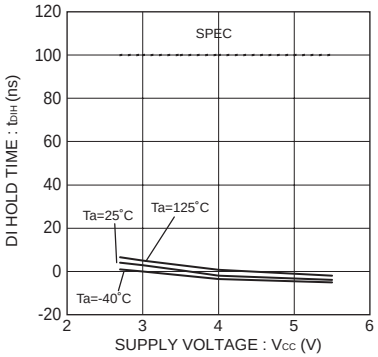


Fig.20 DI hold time tDIH

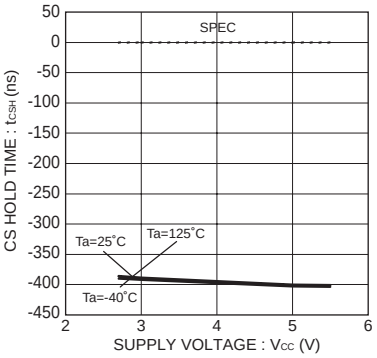


Fig.21 CS hold time tCSH

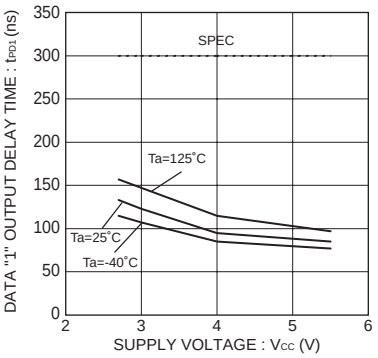


Fig.22 Data "1" output delay time tPD1

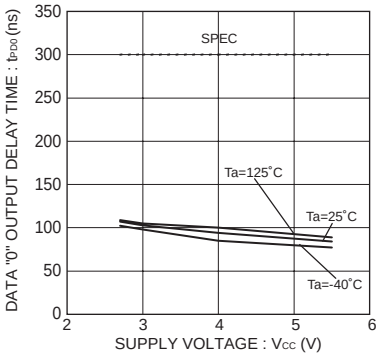


Fig.23 Data "0" output delay time tPD0

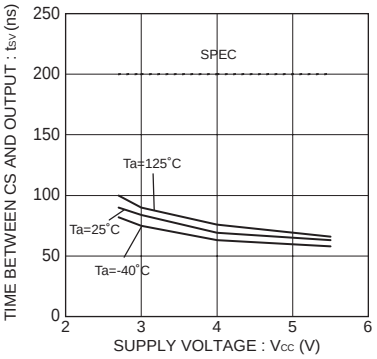


Fig.24 Time from CS to output establishment tSV

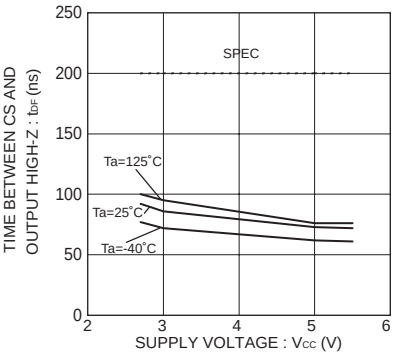


Fig.25 Time from CS to High-Z tDF

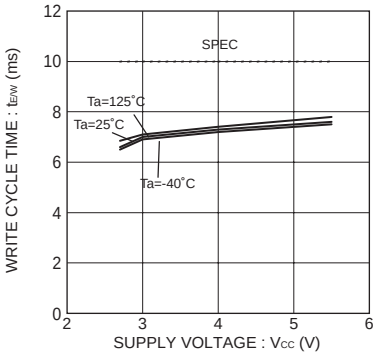


Fig.26 Write cycle time tE/W

● Block diagram

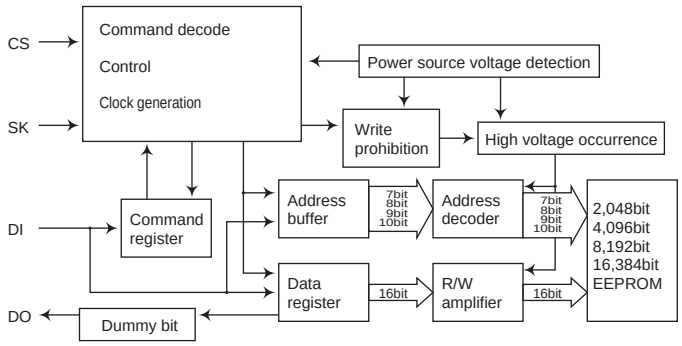


Fig.27 Block diagram

● Pin assignment and function

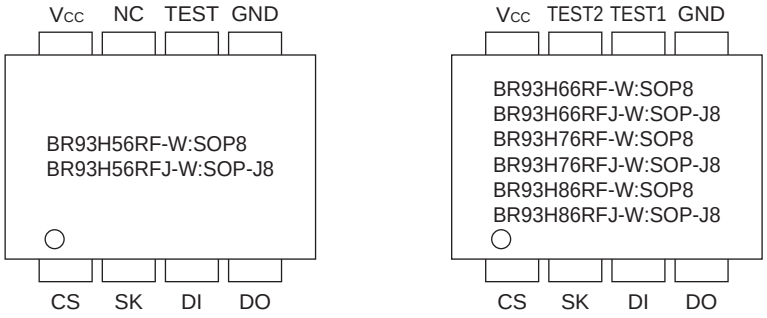


Fig.28 Pin assignment diagram

Pin name	Input / output	Function
Vcc	–	Power source
GND	–	All input / output reference voltage, 0V
CS	Input	Chip select input
SK	Input	Serial clock input
DI	Input	Start bit, ope code, address, and serial data input
DO	Output	Serial data output, READY / $\overline{\text{BUSY}}$ internal condition display output
TEST	–	TEST terminal, GND or OPEN
NC	–	Non connected terminal, Vcc, GND or OPEN
TEST1	–	TEST terminal, GND or OPEN
TEST2	–	TEST terminal, Vcc, GND or OPEN

● Command mode

Command		Start bit	Ope code	Address BR93H56/66-W	Address BR93H76/86-W	Data
Read (READ)	(*1)	1	10	A7,A6,A5,A4,A3,A2,A1,A0,	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0 (READ DATA)
Write enable (WEN)		1	00	1 1 * * * * * *	1 1 * * * * * * * *	
Write (WRITE)	(*2)	1	01	A7,A6,A5,A4,A3,A2,A1,A0,	A9,A8,A7,A6,A5,A4,A3,A2,A1,A0	D15~D0 (WRITE DATA)
Write all (WRAL)	(*2,3)	1	00	0 1 * * * * * B0	0 1 * * * * * B2,B1,B0	D15~D0 (WRITE DATA)
Write disable (WDS)		1	00	0 0 * * * * * *	0 0 * * * * * * * *	

A7 - B0 of BR93H56-W becomes Don't Care.
A9 - B2 of BR93H76-W becomes Don't Care.

- Input the address and the data in MSB.
  - As for *, input either VIH or VIL.
    * Start bit
      Acceptance of all the commands of this IC starts at recognition of the start bit.
      The start bit refers to the first "1" input after the rise of CS.

(*1) : For read, by continuous SK clock input after setting the read command, data output of the set address starts, and address data in significant order are continuously output in sequence. (Auto increment function)

(*2) : When the read and the write all commands are executed, data written in the selected memory cell is automatically deleted, and input data is written.

(*3) : For the write all command, data written in memory cell of the areas designated by B2, B1, and B0, are automatically deleted, and input data is written in bulk.

● Write all area

B2	B1	B0	Write area
0	0	0	000h ~ 07Fh
0	0	1	080h ~ 0FFh
0	1	0	100h ~ 17Fh
0	1	1	180h ~ 1FFh
1	0	0	200h ~ 27Fh
1	0	1	280h ~ 2FFh
1	1	0	300h ~ 37Fh
1	1	1	380h ~ 3FFh

Designation of B2, B1, and B0

H56	*	*	*
H66	*	*	B0
H76	*	B1	B0
H86	B2	B1	B0

- The write all command is written in bulk in 2Kbit unit.
  The write area can be selected up to 3bit. Confirm the settings and write areas of the above B2, B1, and B0.

● Description of operations

Communications of the Microwire Bus are carried out by SK (serial clock), DI (serial data input), DO (serial data output), and CS (chip select) for device selection.When connecting one EEPROM to a microcontroller, connect as shown in Fig. 29 (a) or Fig. 29 (b). When using the input and output common I/O port of the microcontroller, connect DI and DO via a resistor, as shown in Fig. 29 (b) (Refer to pages 13 and 14.). Connection by 3 lines is available.For plural connections, refer to Fig. 29 (c).

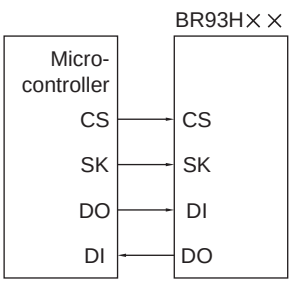


Fig.29(a) Connection by 4 lines

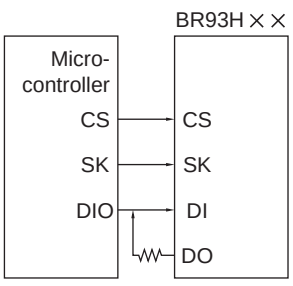


Fig.29(b) Connection by 3 lines

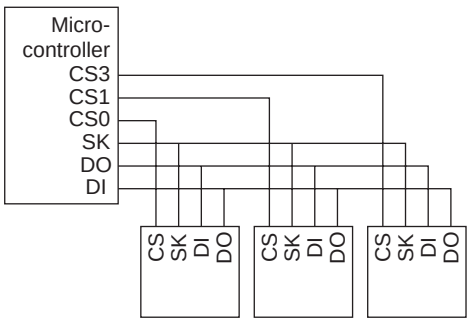


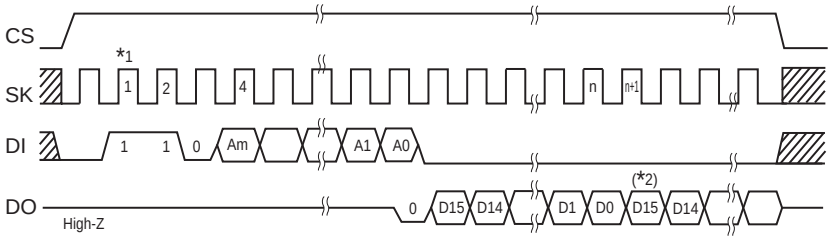
Fig29.(c) Connection example of plural devices

Fig.29 Connection method with microcontroller

Communications of the Microwire Bus are started by the first "1" input after the rise of CS. This input is called a start bit. After input of the start bit, input ope code, address, and data. Address and data are input all in MSB.
"0" input after the rise of CS to the start bit input is all ignored. Therefore, when there is limitation in the PIO bit width of the microcontroller, input "0" before the start bit input, to control the bit width.

● Timing chart

1) Read cycle (READ)



BR93H56/66-W : n=27, m=7
BR93H76/86-W : n=29, m=9

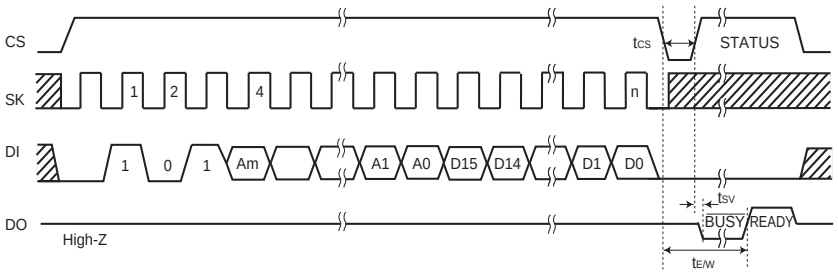
(*2) The following address data output (auto increment function)

*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And when "1" is input after plural "0" are input, it is recognized as a start bit, and the following operation is started. This is common to all the commands to described hereafter.

Fig.30 Read cycle

○When the read command is acknowledged, the data (16 bits) for the input address is output serially. The data is synchronized with the SK rise during A0 acquisition and a ì0î (dummy bit) is output. All further data is output in synchronization with the SK pulse rises. This IC has an address auto increment function, active only at read command. In this function the above address data is read sequentially by continuously inputting SK clock. During the auto increment, keep CS at "H".

2) Write cycle (WRITE)



BR93H56/66-W : n=27,m=7
BR93H76/86-W : n=29,m=9

○In this command, input 16bit data (D15 ~ D0) are written to designated addresses (Am ~ A0). The actual write starts by the fall of CS from the rise of D0 taken SK clock (n-th clock from the start bit input), to the rise of the (n+1)-th clock.
When STATUS is not detected, (CS = "L" fixed) Max. 10ms in conformity with tE/W, and when STATUS is detected (CS = "H"), all commands are not accepted for areas where "L" ($\overline{\text{BUSY}}$) is output from D0, therefore, do not input any command.
Write is not made even if CS is started after input of clock after (n+1)-th clocks.
Note) Take tSKH or more from the rise of the n-th clock to the fall of CS.

Fig.31 Write cycle

3) Write all cycle (WRAL)

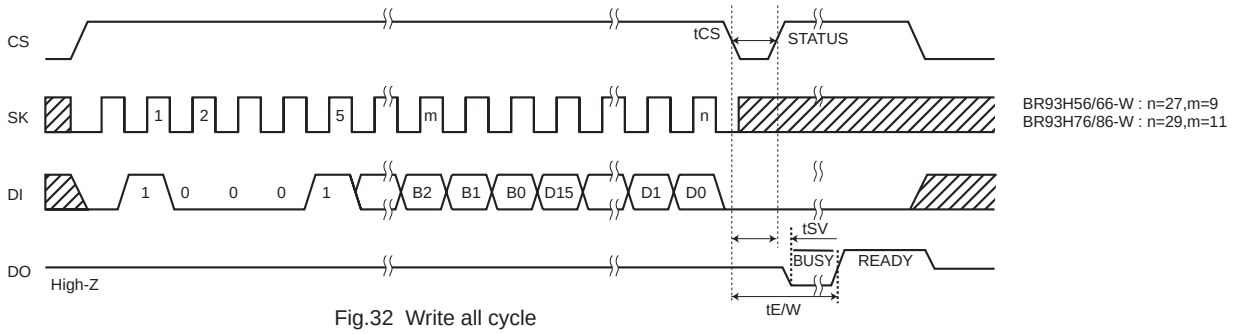


Fig.32 Write all cycle

○ In this command, input 16bit data is written simultaneously to designated block for 128 words. Data is writen in bulk at a write time of only Max. 10ms in conformity with tE/W. When writing data to all addresses, designate each block by B2, B1, and B0, and execute write. Write time is Max. 10ms. The actual write starts by the fall of CS from the rise of D0 taken at SK clock (n-th clock from the start bit input), to the rise of the (n+1)-th clock. When CS is ended after clock input after the rise of the (n+1)-th clock, command is cancelled, and write is not completed.Note: Take tSKH or more from the rise of the n-th clock to the fall of CS.

Designation of B2, B1, and B0

H56	*	*	*
H66	*	*	B0
H76	*	B1	B0
H86	B2	B1	B0

4) Write enable (WEN) / disable (WDS) cycle

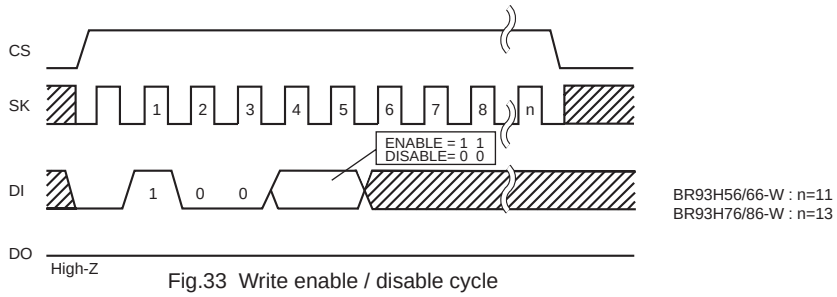


Fig.33 Write enable / disable cycle

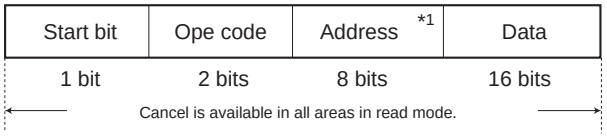
○ At power on, this IC is in write disable status by the internal RESET circuit. Before executing the write command, it is necessary to execute the write enable command. And, once this command is executed, it is valid until the write disable command is executed or the power is turned off. However, the read command is valid irrespective of write enable / disable command. input to SK after 6 clocks of this command is available by either "H" or "L", but be sure to input it.

○ When the write enable command is executed after power on, write enable status gets in. When the write disable command is executed then, the IC gets in write disable status as same as at power on, and then the write command is cancelled thereafter in software manner. However, the read command is executable. In write enable status, even when the write command is input by mistake, write is started. To prevent such a mistake, it is recommended to execute the write disable command after completion of write.

● Application

1) Method to cancel each command

○READ

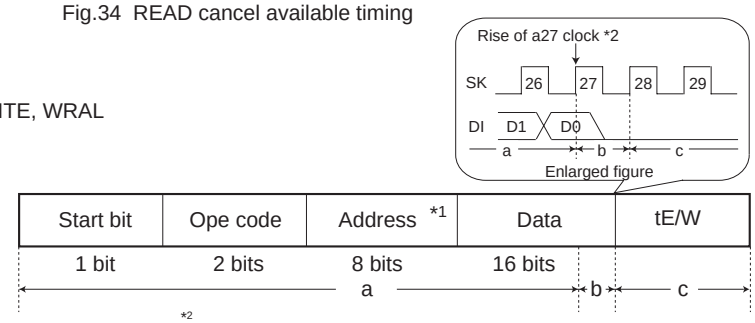


ü Method to cancel : cancel by CS = "L"

*1 Address is 8 bits in BR93H56-W, and BR93H66-W.
Address is 10 bits in BR93H76-W, and BR93H86-W.

Fig.34 READ cancel available timing

○WRITE, WRAL



*1 Address is 8 bits in BR93H56-W, and BR93H66-W.
Address is 10 bits in BR93H76-W, and BR93H86-W.

*2 27 clocks in BR93H56-W, and BR93H66-W
29 clocks in BR93H76-W, and BR93H86-W

*3 28 clocks in BR93H56-W, and BR93H66-W
30 clocks in BR93H76-W, and BR93H86-W

a : from start bit to 27 clock rise *2
Cancel by CS = "L"

b : 27 clock rise *2 and after
Cancellation is not available by any means. If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

c : 28 clock rise *3 and after
Cancel by CS = "L"

However, when write is started in b area (CS is ended), cancellation is not available by any means.
And when SK clock is input continuously, cancellation is not available.

Note 1) If Vcc is made OFF in this area, designated address data is not guaranteed, therefore write once again.

Note 2) If CS is started at the same timing as that of the SK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SK = "L" area.
As for SK rise, recommend timing of tCSS/tCSH or higher.

Fig.35 WRITE, WRAL cancel available timing

2) Equivalent circuit

○Output circuit

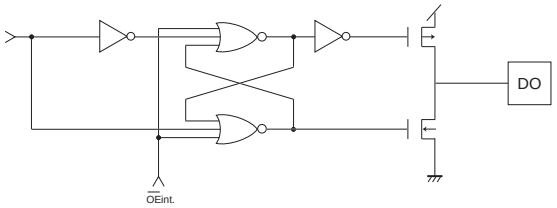


Fig.36 DO output equivalent circuit

○Input circuit

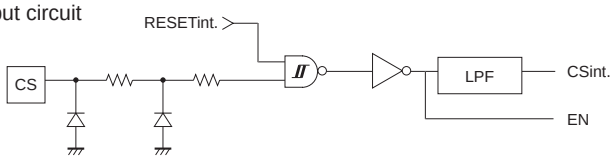


Fig.37 CS input equivalent circuit

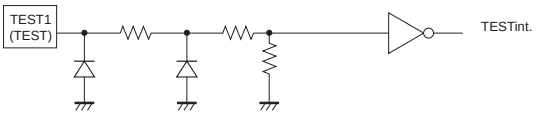


Fig.39 TEST1 (TEST) input equivalent circuit

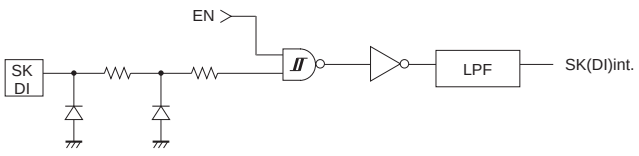


Fig.38 SK, DI input equivalent circuit

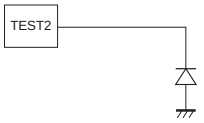


Fig.40 TEST2 input equivalent circuit

3) I/O peripheral circuit

3-1) Pull down CS.

By making CS = "L" at power ON/OFF, mistake in action and mistake write are prevented.
Refer to the item 6) Notes at power ON/OFF in page 15.

○ Pull down resistance Rpd of CS pin

To prevent operation and write error at power ON/OFF, CS pull down resistance is necessary. Select an appropriate resistance value from microcontroller VOH, IOH, and VIL characteristics of this IC.

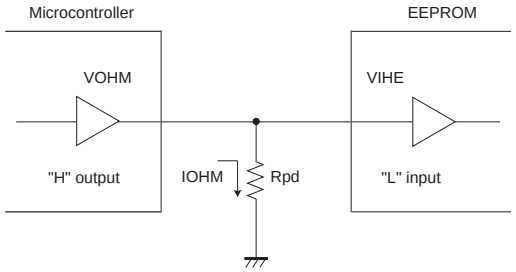


Fig.41 CS pull down resistance

$$Rpd \quad \frac{VOHM}{IOHM} \quad \cdots ①$$

$$VOHM \quad VIHE \quad \cdots ②$$

Example) When Vcc = 5V, VIHE = 2V, VOHM = 2.4V, IOHM = 2mA, from the equation ①,

$$Rpd \quad \frac{2.4}{2\times10^{-3}}$$

$$\therefore \quad Rpd \quad 1.2\ (k\ )$$

With the value of Rpd to satisfy the above equation, VOHM becomes 2.4V or higher, and with VIHE (= 2.0V), the equation ② is also satisfied.

- VIHE : EEPROM VIH specifications
- VOHM : microcontroller VOH specifications
- IOHM : microcontroller IOH specifications

3-2) DO is available in both pull up and pull down.

DO output become "High-Z" in other READY / $\overline{BUSY}$ output timing than after data output at read command and write command.
When malfunction occurs at "High-Z" input of the microcontroller port connected to DO, it is necessary to pull down and pull up DO.
When there is no influence upon the microcontroller actions, DO may be OPEN.
If DO is OPEN, and at timing to output status READY, at timing of CS = "H", SK = "H", DI = "H", EEPROM recognizes this as a start bit, resets READY output, and DO = "High-Z", therefore, READY signal cannot be detected. To avoid such output, pull up DO pin for improvement.

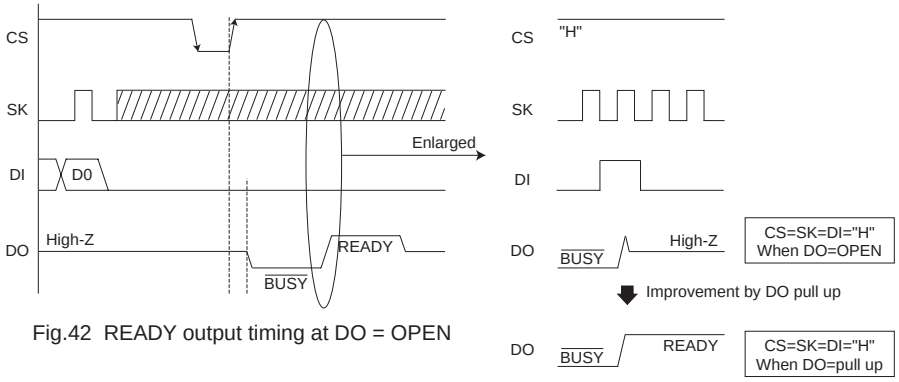


Fig.42 READY output timing at DO = OPEN

○ Pull up resistance Rpu and pull down resistance Rpd of DO pin

As for pull up and pull down resistance value, select an appropriate value to this resistance value from microcontroller VIH, VIL, and VOH, IOH, VOL, IOL characteristics of this IC.

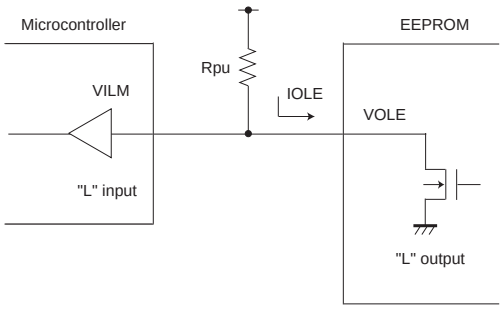


Fig43 DO pull up resistance

$$Rpu \quad \frac{V_{CC}\text{-}VOLE}{IOLE} \quad \cdots ③$$

$$VOLE \quad VILM \quad \cdots ④$$

Example) When Vcc = 5V, VOLE = 0.4V, IOLE = 2.1mA, VILM = 0.8V, from the equation ③,

$$Rpu \quad \frac{5\text{-}0.4}{2.1\times10^{-3}}$$

$$\therefore \quad Rpu \quad 2.2\ (k\ )$$

With the value of Rpu to satisfy the above equation, VOLE becomes 0.4V or below, and with VILM (= 0.8V), the equation ④ is also satisfied.

- VOLE : EEPROM VOL specifications
- IOLE : EEPROM IOL specifications
- VILM : microcontroller VIL specifications

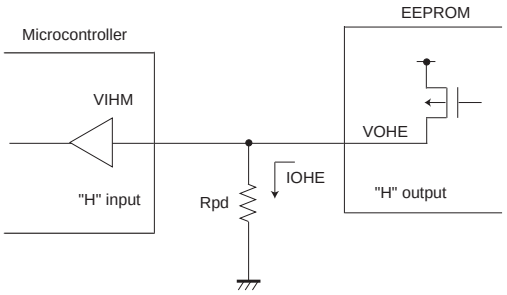


Fig.44 DO pull down resistance

$$Rpd \quad \frac{VOHE}{IOHE} \quad \cdots ⑤$$

$$VOHE \quad VIHM \quad \cdots ⑥$$

Example) When Vcc = 5V, VOHE = Vcc ~ 0.2V, IOHE = 0.1mA, VIHM = Vcc×0.7V, from the equation ⑤,

$$Rpd \quad \frac{5-0.2}{0.1\times10^{-3}}$$

$$\therefore \quad Rpd \quad 48\ (k\ )$$

With the value of Rpd to satisfy the above equation, VOHE becomes 2.4V or higher, and with VIHM (= 3.5V), the equation ⑥ is also satisfied.

- VOHE : EEPROM VOH specifications
- IOHE : EEPROM IOH specifications
- VIHM : microcontroller VIH specifications

○ READY / $\overline{BUSY}$ status display (DO terminal) (common to BR93H56-W, BR93H66-W, BR93H76-W, BR93H86-W)

This display outputs the internal status signal. When CS is started after tCS (Min. 200ns) from CS fall after write command input, "H" or "L" is output.

R/$\overline{B}$ display = "L" ($\overline{BUSY}$) = write under execution
(D0 status)

After the timer circuit in the IC works and creates the period of tE/W, this time circuit completes automatically. And write to the memory cell is made in the period of tE/W, and during this period, other command is not accepted.

R/$\overline{B}$ display = "H" (READY) = command wait status
(D0 status)

Even after tE/W (Max. 10ms) from write of the memory cell, the following command is accepted. Therefore, CS = "H" in the period of tE/W, and when input is in SK, DI, malfunction may occur, therefore, DI = "L" in the area CS = "H". (Especially, in the case of shared input port, attention is required.)

Do not input any command while status signal is output. Command input in $\overline{BUSY}$ area is cancelled, but command input in READY area is accepted. Therefore, status READY output is cancelled, and malfunction and mistake write may be made.

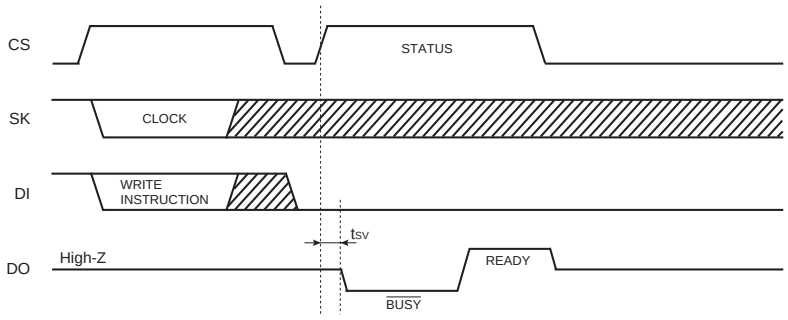


Fig.45 R/$\overline{B}$ status output timing chart

4) When to directly connect DI and DO

This IC has independent input terminal DI and output terminal DO, and separate signals are handled on timing chart, meanwhile, by inserting a resistance R between these DI and DO terminals, it is possible to carry out control by 1 control line.

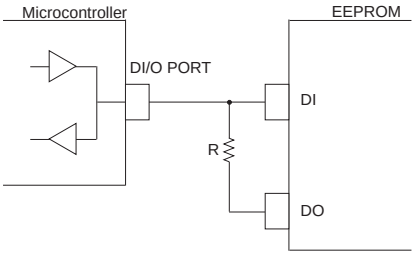


Fig.46 DI, DO control line common connection

○ Data collision of microcontroller DI/DO output and DO output and feedback of DO output to DI input

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following points.

4-1) 1 clock cycle to take in A0 address data at read command

Dummy bit "0" is output to DO terminal.

→ When address data A0 = "1" input, through current route occurs.

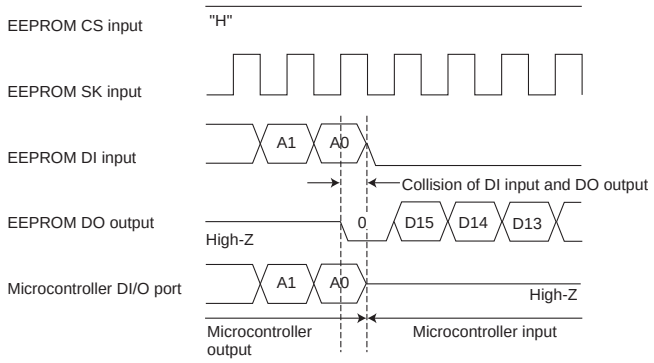


Fig.47 Collision timing at read data output at DI, DO direct connection

4-2) Timing of CS = "H" after write command. DO terminal in READY / BUSY function output.

When the next start bit input is recognized, "HIGH-Z" enters.

→Particularly, at command input after write, when CS input is started with microcontroller DI/O output "L"

READY output "H" is output from DO terminal, and a through current path occurs.

Feedback input at timing of these 4-1) and 4-2) does not cause disorder in basic operations, if resistance R is inserted.

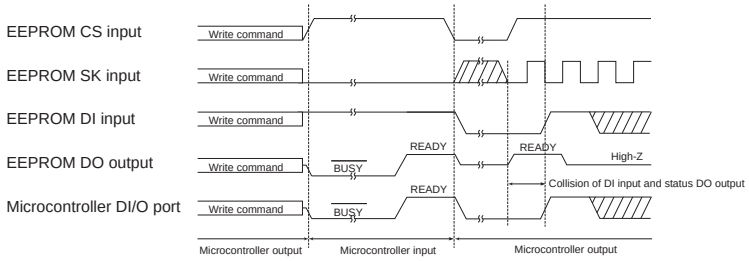


Fig.48 Collision timing at DI, DO direct connection

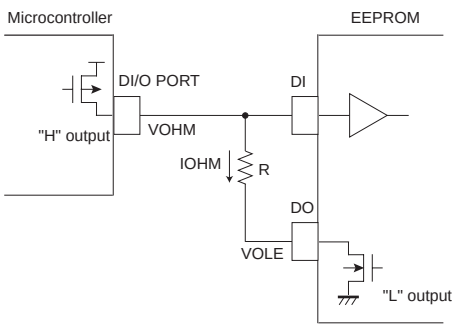
○ Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current value with consideration of impedance and of power source line in set. Insert resistance R, and set the value R to satisfy EEPROM input level VIH/VIL, even under influence of voltage decline due to leak current. Insertion of R will not cause any influence upon basic operations.

4-3) Address data A0 = "1" input, dummy bit "0" output timing

(When microcontroller DI/O output is "H", EEPROM DO outputs "L", and "H" is input to DI)

- Make the through current to EEPROM 10mA or below.
- See to it that the input level VIH of EEPROM should satisfy the following.



Conditions

$VOHM \geq VIHE$

$VOHM \geq IOHM \times R + VOLE$

At this moment, if VOLE = 0V,

$VOHM \geq IOHM \times R$

$\therefore R \quad \frac{VOHM}{IOHM} \quad \cdots ⑦$

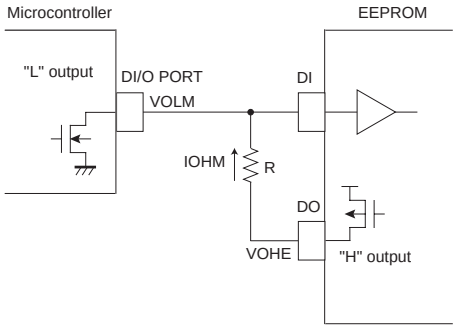
- VIHE : EEPROM VIH specifications
- VOLE : EEPROM VOL specifications
- VOHM : Microcontroller VOH specifications
- IOHM : Microcontroller IOH specifications

Fig.49 Circuit at DI, DO direct connection (Microcontroller DI/O "H" output, EEPROM "L" output)

4-4) DO status READY output timing

(When the microcontroller DI/O is "L", EEPROM DO outputs "H", and "L" is input to DI)

・Set the EEPROM input level VIL so as to satisfy the following.



Conditions

VOLM VILE

VOLM VOHE - IOLM × R

At this moment, if VOHE=V_{CC}

VOLM V_{CC} - IOLM × R

$\therefore$ R $\dfrac{V_{CC} - VOLM}{IOLM}$ ... ⑧

・VILE : EEPROM VIL specifications
・VOHE : EEPROM VOH specifications
・VOLM : Microcontroller VOL specifications
・IOLM : Microcontroller IOL specifications

Example) When Vcc = 5, VOHM = 5V, IOHM = 0.4mA, VOLM = 5V, IOLM = 0.4mA

From the equation ⑦,

R $\dfrac{VOHM}{IOHM}$

R $\dfrac{5}{0.4\times10^{-3}}$

$\therefore$ R 12.5 [k] ... ⑨

From the equation ⑧,

R $\dfrac{V_{CC} - VOLM}{IOLM}$

R $\dfrac{5 - 0.4}{2.1\times10^{-3}}$

$\therefore$ R 2.2 [k] ... ⑩

Therefore, from the equations ⑨ and ⑩,

$\therefore$ R 12.5 [k]

Fig.50 Circuit at DI, DO direct connection (Microcontroller DI/O "L" output, EEPROM "H" output)

5) Notes at test pin wrong input

There is no influence of external input upon TEST2 pin.

For TEST1 (TEST) pin, input must be GND or OPEN. If H level is input, the following may occur:

1. At WEN, WDS, READ command input

   There is no influence by TEST1 (TEST) pin.

2. WRITE, WRAL command input

* BR93H56-W, BR93H66-W, address 8 bits
BR93H76-W,BR93H86-W, address 10 bits

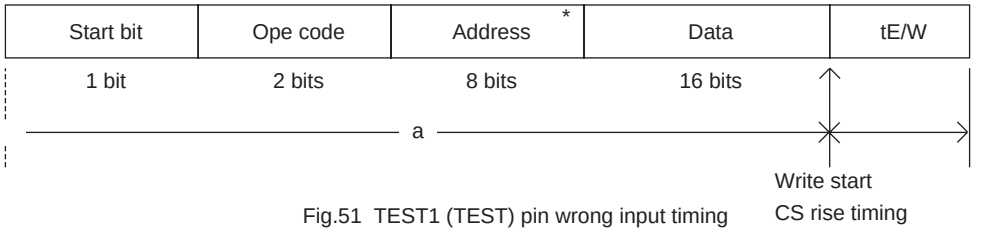


Fig.51 TEST1 (TEST) pin wrong input timing

a. There is no influence by TEST1 (TEST) pin.

a. If H during write execution, it may not be written correctly. And H area remains $\overline{BUSY}$ and READY does not go back. Avoid noise input, and at use, be sure to connect it to GND terminal or set it OPEN.

6) Notes on power ON/OFF

・At power ON/OFF, set CS "L".
When CS is "H", IC gets in input accept status (active). At power ON, set CS "L" to prevent malfunction from noise. (When CS is in "L" status, all inputs are cancelled.) At power decline low power status may prevail. Therefore, at power OFF, set CS "L" to prevent malfunction from noise.

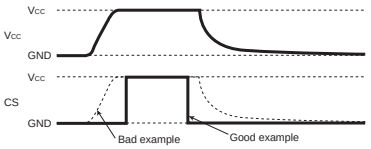


Fig.51 Timing at power ON/OFF

(Bad example) CS pin is pulled up to Vcc.
In this case, CS becomes "H" (active status). EEPROM may malfunction or have write error due to noises. This is true even when CS input is High-Z.

(Good example) It is "L" at power ON/OFF.
Set 10ms or higher to recharge at power OFF.When power is turned on without following the above condition, IC internal circuit may not be reset.

○POR circuit

This IC has a POR (Power On Reset) circuit as a mistake write countermeasure.After POR is activated, write disable status is active. The POR circuit is active only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may enable write status due to noise.For secure actions, observe the following conditions:

1 Set CS = "L".
2 Turn on power so as to satisfy the recommended conditions of tR, tOFF, Vbot for POR circuit operation.

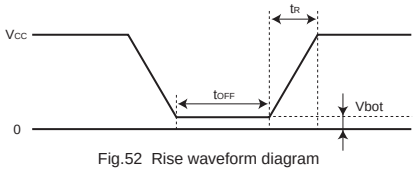


Fig.52 Rise waveform diagram

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

○LVCC circuit

LVCC (Vcc - Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
At LVCC voltage (Typ. = 1.9V) or below, it prevent data rewrite.

7) Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur. Therefore, it is recommended to attach a by pass capacitor (0.1μF) between IC Vcc and GND to remove noise or surge. Attach it as close to the IC as possible.It is also recommended to attach a bypass capacitor between board Vcc and GND.

○SK noise

When the rise time (tR) of SK is long, and noise exists, malfunction may occur due to clock bit displacement. To avoid this, a Schmitt trigger circuit is built into SK input. The hysteresis width of this circuit is set to about 0.2V (at Vcc = 5V). If noises exists at SK input, set the noise amplitude to 0.2Vp-p or below.It is recommended to set the rise time (tR) of SK to 100ns or below. If the rise time is 100ns or higher, take sufficient noise countermeasures. Set the clock rise and fall time as small as possible.

●Cautions on use

(1) Numbers and data in entries are representative design values and are not guaranteed values of the items.
(2) Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sucircuit constants.
(3) Absolute maximum ratings Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
(4) GND potential Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
(5) Heat design
In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.
(6) Short circuit between terminals and erroneous mounting Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
(7) Operation in strong electromagnetic field Using the ICs in a strong electromagnetic field can cause operation malfunction

●Selection of order type

BR	93	H	56	RF	–	W	E2

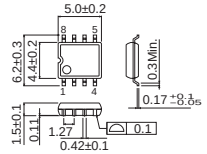
ROHM type name	BUS type 93 : Microwire	Operating temperature L : -40˚C ~ +85 ˚C A : -40˚C ~ +105 ˚C H : -40˚C ~ +125 ˚C	Capacity ■Microwire BUS 56=2K 66=4K 76=8K 86=16K	Package type RF:SOP RFJ:SOP-J(JEDEC)	Double cell	Taping type name E2 : reel shape emboss taping

●Package specifications

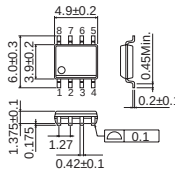
SOP8/SOP-J8

<External appearance>

• SOP8

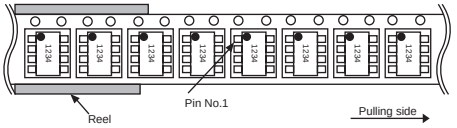


• SOP-J8



<Package specifications>

Package type	Emboss taping
Package quantity	2500pcs
Package direction	E2 (When the reel is gripped by the left hand, and the tape is pulled out by the right hand, No.1 pin of the product is at the left top.)



* For ordering, specify a number of multiples of the package quantity.

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