OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

DESCRIPTION

The M74HC244-1 is an integrated circuit chip consisting of two blocks of 3-state noninverting buffers with four independent circuits that share a common enable input.

FEATURES

- High-fanout 3-state output : (I_{OL}=24mA, I_{OH}=−24mA)
- High-speed : 9ns typ. (C_L=50pF, V_{CC}=5V)
- Low power dissipation : 25μ/W/package, max (V_{CC}=5V, T_a=25℃, quiescent state)
- High noise margin : 30% of V_{CC}, min (V_{CC}=4.5, 6V)
- Capable of driving 60 74 LSTTL loads
- Wide operating voltage range : V_{CC}=2～6V
- Wide operating temperature range : T_a=−40～+85℃
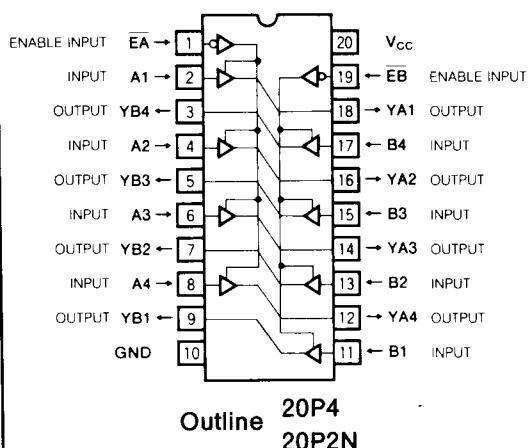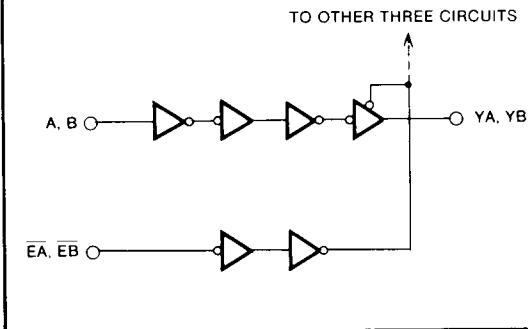
APPLICATION

General purpose, for use in industrial and consumer digital equipment.

FUNCTION

Use of silicon gate technology allows the M74HC244-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS244. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. The M74HC244-1 consists of two independent blocks with each block containing four buffers.

When enable input $\overline{E}$ is low and input A or B is low, output Y will be set low, However, if A or B is high, then Y will be set high. When $\overline{E}$ is high, all outputs within the block will become high-impedance state, irrespective A or B. All eight buffer circuits can be controlled simultaneously by connecting $\overline{EA}$ and $\overline{EB}$.

PIN CONFIGURATION (TOP VIEW)

Outline 20P4
20P2N

LOGIC DIAGRAM (EACH BUFFER)

FUNCTION TABLE (Note 1)

Inputs		output
A, B	$\overline{EA}$, $\overline{EB}$	YA, YB
L	L	L
H	L	H
X	H	Z

Note 1 : Z : High impedance
X : Irrelevant

OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

ABSOLUTE MAXIMUM RATINGS ($T_a=-40\sim+85℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5\sim+7.0$	V
V_I	Input voltage		$-0.5\sim V_{CC}+0.5$	V
V_O	Output voltage		$-0.5\sim V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I<0V$	-20	mA
		$V_I>V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_O<0V$	-20	mA
		$V_O>V_{CC}$	20	
I_O	Output current		±50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	±200	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		$-65\sim+150$	℃

Note 2 : M74HC244-1FP ; $T_a=-40\sim+75℃$ and $T_a=75\sim85℃$ are derated at $-7mW/℃$

RECOMMENDED OPERATING CONDITIONS ($T_a=-40\sim+85℃$)

Symbol	Parameter		Min	Typ	Max	Unit
				Limits		
V_{CC}	Supply voltage		2		6	V
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		-40		$+85$	℃
t_r, t_f	Input rise time, fall time	$V_{CC}=2.0V$	0		500	ns/V
		$V_{CC}=4.5V$	0		50	
		$V_{CC}=6.0V$	0		30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	$V_{CC}(V)$	25℃ Min	25℃ Typ	25℃ Max	$-40\sim+85℃$ Min	$-40\sim+85℃$ Max	Unit
V_{IH}	High-level input voltage	$V_O=V_{CC}-0.1V$ $I_O=20\mu A$	2.0	1.5			1.5		V
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_O=0.1V$, $V_{CC}-0.1V$ $I_O=20\mu A$	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_I=V_{IL}$, V_{IH} $I_{OH}=-20\mu A$	2.0	1.9			1.9		V
		$I_{OH}=-20\mu A$	4.5	4.4			4.4		
		$I_{OH}=-20\mu A$	6.0	5.9			5.9		
		$I_{OH}=-24mA$	4.5	3.83			3.70		
V_{OL}	Low-level output voltage	$V_I=V_{IH}$, V_{IL} $I_{OL}=20\mu A$	2.0			0.1		0.1	V
		$I_{OL}=20\mu A$	4.5			0.1		0.1	
		$I_{OL}=20\mu A$	6.0			0.1		0.1	
		$I_{OL}=24mA$	4.5			0.44		0.53	
I_{IH}	High-level input current	$V_I=6V$	6.0			0.1		1.0	μA
I_{IL}	Low-level input current	$V_I=0V$	6.0			-0.1		-1.0	μA
I_{OZH}	Off state high-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=V_{CC}$	6.0			0.5		5.0	μA
I_{OZL}	Off-state low-level output current	$V_I=V_{IH}$, V_{IL}, $V_O=GND$	6.0			-0.5		-5.0	μA
I_{CC}	Static supply current	$V_I=V_{CC}$, GND, $I_O=0\mu A$	6.0			5.0		50.0	μA

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OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{TLH}	Low-to high-level and high-to low-level output	C_L=50pF (Note 4)			10	ns
t_{THL}	transition time				10	ns
t_{PLH}	Low-to high-level and high-to low-level output				15	ns
t_{PHL}	propagation time (A−YA, B−YB)				15	ns
t_{PLZ}	Low-level and high-level output disable time	C_L=5 pF (Note 4)			18	ns
t_{PHZ}	($\overline{EA}$−YA, $\overline{EB}$−YB)				18	ns
t_{PZL}	Low-level and high-level output enable time	C_L=50pF (Note 4)			20	ns
t_{PZH}	($\overline{EA}$−YA, $\overline{EB}$−YB)				20	ns
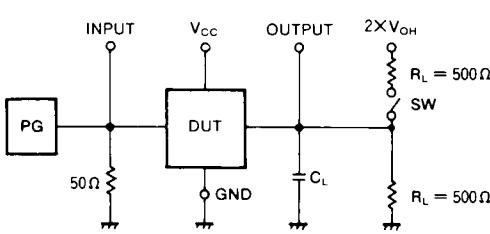
SWITCHING CHARACTERISTICS (V_{CC}=2~6V, T_a=−40~+85°C)

Symbol	Parameter	Test conditions	V_{CC}(V)	Limits					Unit
				25°C			−40~+85°C		
				Min	Typ	Max	Min	Max	
t_{TLH}	Low-to high-level and		2.0		13	60		75	
			4.5		5	12		15	ns
	high-to low-level		6.0		4	10		13	
t_{THL}	output transition time		2.0		18	60		75	
			4.5		4	12		15	ns
			6.0		4	10		13	
t_{PLH}	Low-to high-level and		2.0		24	80		100	
	high-to low-level		4.5		8	16		20	ns
	output propagation time		6.0		7	14		17	
t_{PHL}	(A−YA, B−YB)	C_L=50pF (Note 4)	2.0		22	80		100	
			4.5		8	16		20	ns
			6.0		7	14		17	
t_{PLZ}	Low-level and high-level		2.0		12	105		130	
			4.5		6	21		26	ns
	output disable time		6.0		5	18		22	
t_{PHZ}	($\overline{EA}$−YA, $\overline{EB}$−YB)		2.0		16	105		130	
			4.5		9	21		26	ns
			6.0		8	18		22	
t_{PZL}	Low-level and high-level		2.0		21	105		130	
			4.5		7	21		26	ns
	output enable time		6.0		6	18		22	
t_{PZH}	($\overline{EA}$−YA, $\overline{EB}$−YB)		2.0		24	105		130	
			4.5		8	21		26	ns
			6.0		7	18		22	
C_I	Input capacitance					10		10	pF
C_O	Off-state output capacitance	$\overline{EA}=V_{CC}$, $\overline{EB}=V_{CC}$				15		15	pF
C_{PD}	Power dissipation capacitance (Note 3)				42.4				pF

Note 3 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions (per buffer). The power dissipated during operation under no-load condition is calculated using the following formula :
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_I + I_{CC} \cdot V_{CC}$$

Note 4 : Test Circuit
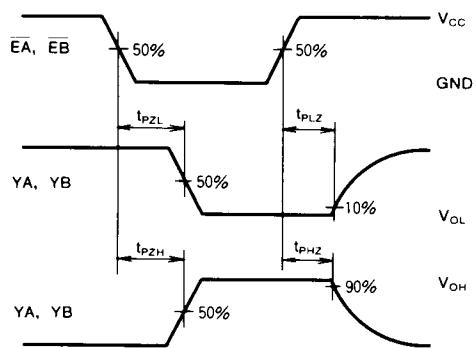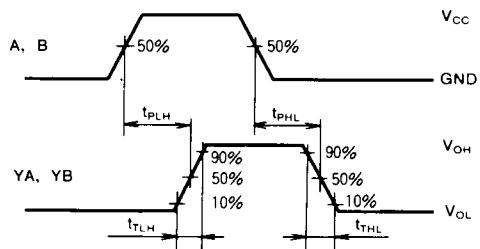
Parameter	SW
t_{TLH}, t_{THL} t_{PLH}, t_{PHL}	Open
t_{PLZ}	Closed
t_{PHZ}	Open
t_{PZL}	Closed
t_{PZH}	Open

(1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER

TIMING DIAGRAM

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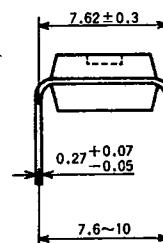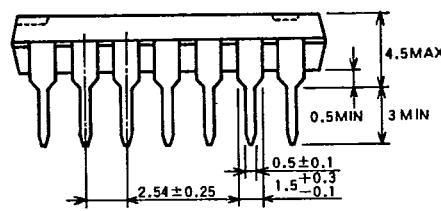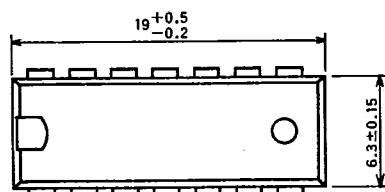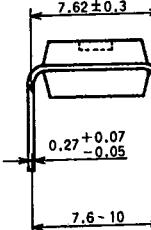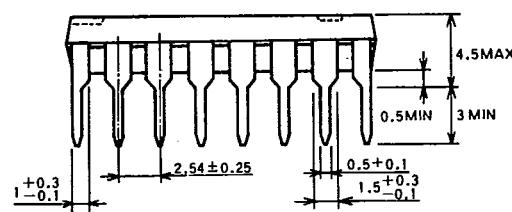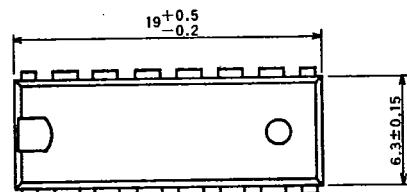
MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES
91D 12849   D T·90·20

TYPE 14P4 14-PIN MOLDED PLASTIC DIP   Dimension in mm


TYPE 16P4   16-PIN MOLDED PLASTIC DIP   Dimension in mm

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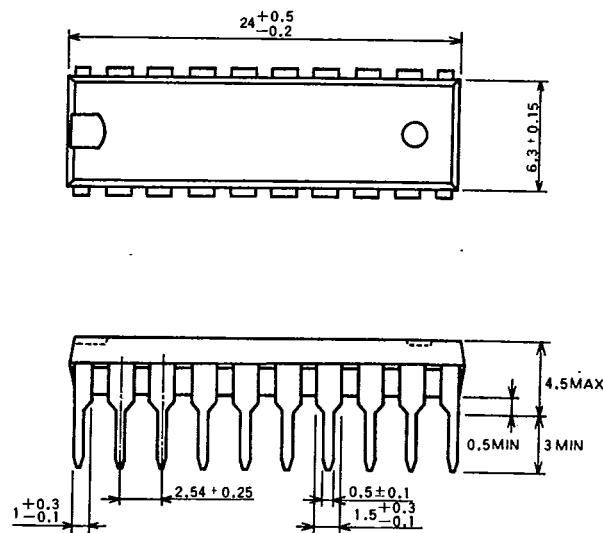
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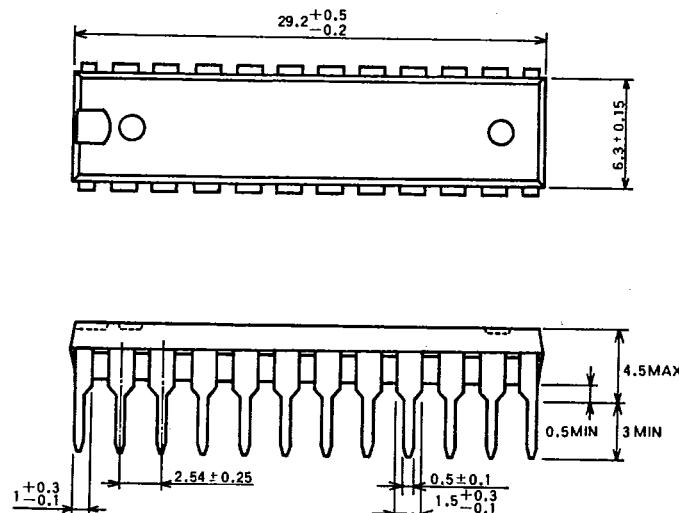
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm

$24^{+0.5}_{-0.2}$

6.3 ± 0.15

4.5MAX

0.5MIN 3 MIN

$1^{+0.3}_{-0.1}$ 2.54 ± 0.25 0.5 ± 0.1 $1.5^{+0.3}_{-0.1}$

7.62 ± 0.3

$0.27^{+0.07}_{-0.05}$

7.6~10

TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm

$29.2^{+0.5}_{-0.2}$

6.3 ± 0.15

4.5MAX

0.5MIN 3 MIN

$1^{+0.3}_{-0.1}$ 2.54 ± 0.25 0.5 ± 0.1 $1.5^{+0.3}_{-0.1}$

7.62 ± 0.3

$0.27^{+0.07}_{-0.05}$

7.6~10

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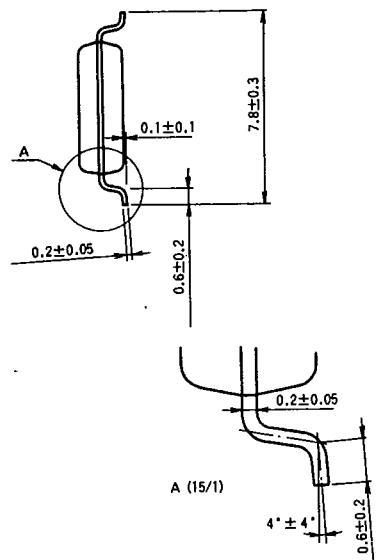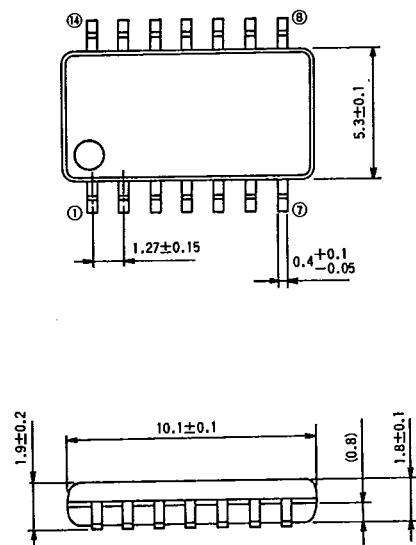
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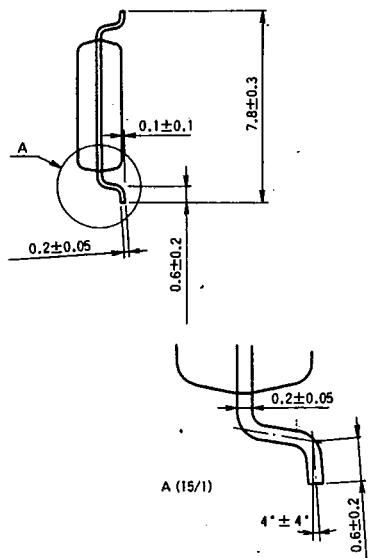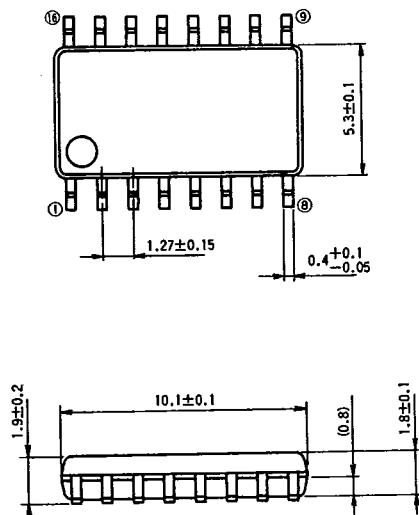
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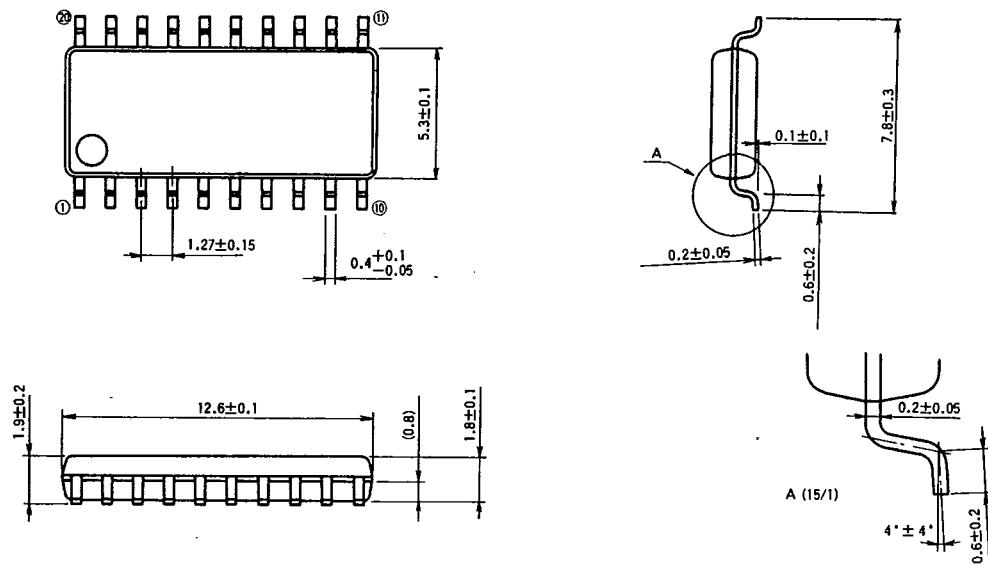
Dimension in mm

TYPE 16P2N 16PIN MOLDED PLASTIC SOP

Dimension in mm

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6249827 MITSUBISHI (DGTL LOGIC)

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MITSUBISHI HIGH SPEED CMOS
PACKAGE OUTLINES
91D 12852   D . T-90-20
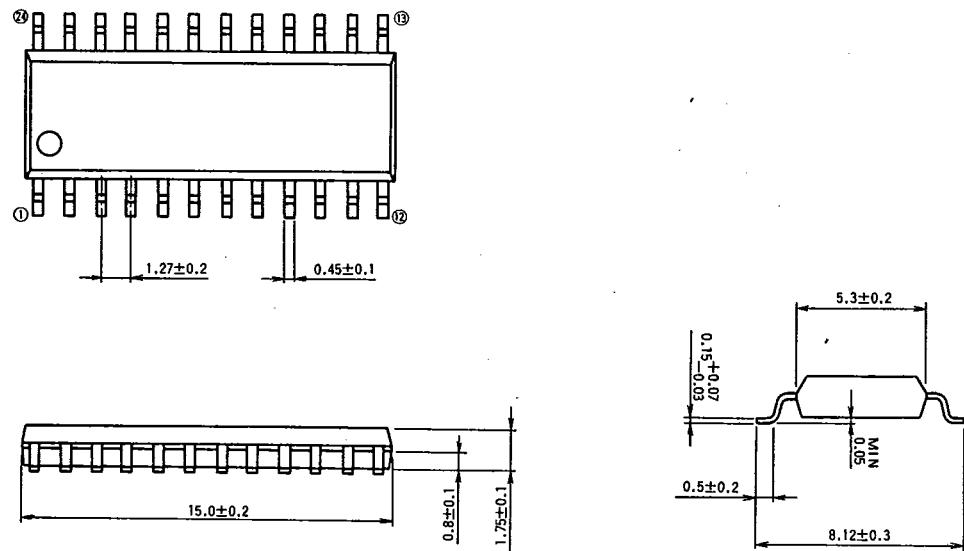
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm

5.3±0.1

1.27±0.15

0.4 +0.1 −0.05

7.8±0.3

0.1±0.1

A

0.2±0.05

0.6±0.2

1.9±0.2

12.6±0.1

(0.8)

1.8±0.1

0.2±0.05

A (15/1)

4°±4°

0.6±0.2

TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm

1.27±0.2

0.45±0.1

15.0±0.2

0.8±0.1

1.75±0.1

5.3±0.2

0.4+0.07 −0.03 +0.15

MIN 0.05

0.5±0.2

8.12±0.3

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MITSUBISHI HIGH SPEED CMOS
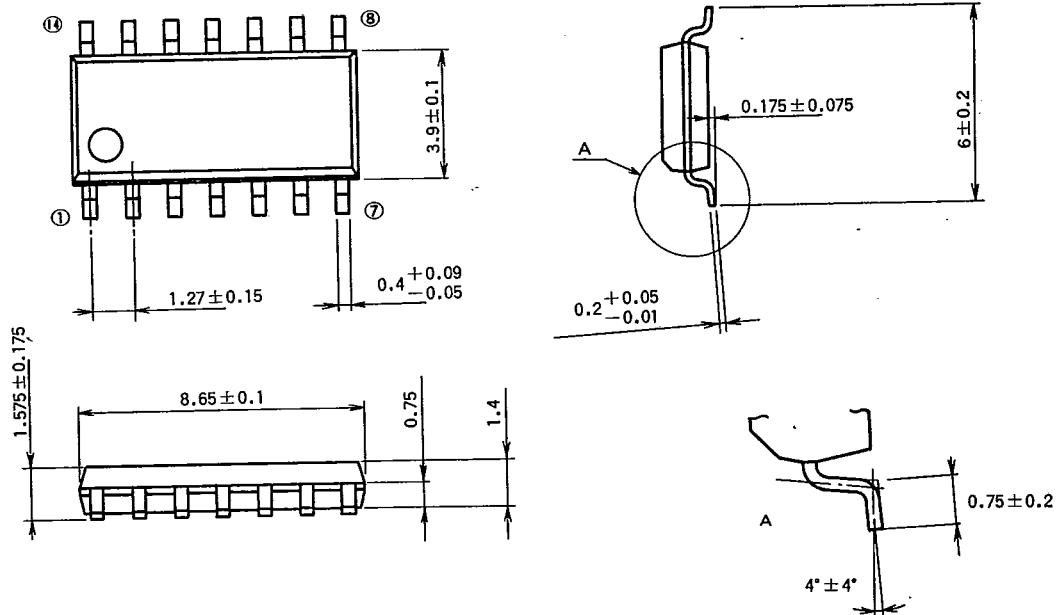
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)   91D 12853   D T-90-20
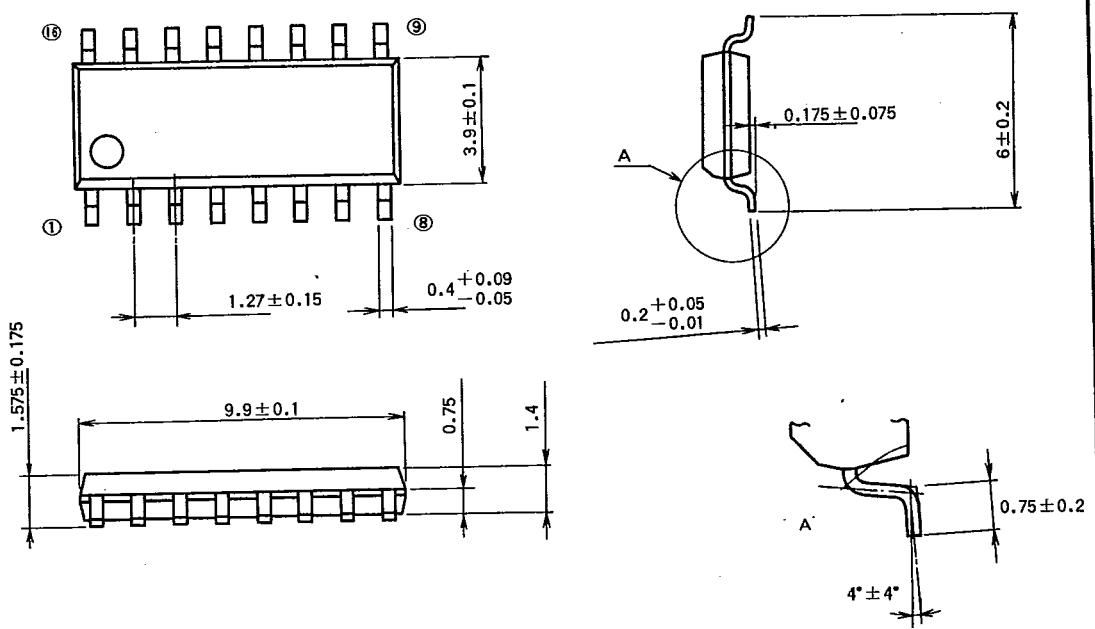
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)   Dimension in mm

3.9±0.1

6±0.2

0.175±0.075

A

1.27±0.15

0.4 +0.09 −0.05

0.2 +0.05 −0.01

1.575±0.175

8.65±0.1

0.75

1.4

A

0.75±0.2

4°±4°

TYPE 16P2P 16-PIN MOLDED PLASTIC SOP(JEDEC 150mil body)   Dimension in mm

3.9±0.1

6±0.2

0.175±0.075

A

1.27±0.15

0.4 +0.09 −0.05

0.2 +0.05 −0.01

1.575±0.175

9.9±0.1

0.75

1.4

A

0.75±0.2

4°±4°

MITSUBISHI ELECTRIC

MITSUBISHI HIGH SPEED CMOS

PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12854   D T-90-20

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP(JEDEC 300mil body)

Dimension in mm

7.5 ± 0.1

10.3 ± 0.3

0.2 ± 0.1

A

1.27 ± 0.15 $0.4^{+0.09}_{-0.05}$

$0.25^{+0.07}_{-0.02}$

2.5 ± 0.15

12.8 ± 0.1 1.025 2.3

0.8 ± 0.2

$4°\pm4°$

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