T-46-07-12

National Semiconductor

74FCT823A • 74FCT823B
9-Bit D Flip-Flop

General Description

The 'FCT823A/B is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

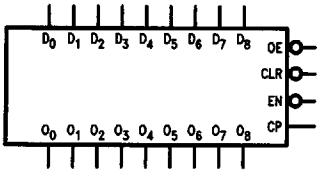
AC Specifications for 'FCT823A are preliminary.

Features

- NSC 74FCT823A/B is pin and functionally equivalent to IDT 74ACT823A/B
- High speed parallel registers with positive edge-triggered D-type flip-flop
- Buffered common clock enable ($\overline{EN}$) and asynchronous clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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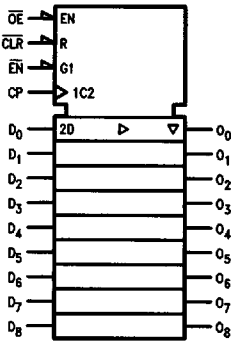
Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

IEEE/IEC



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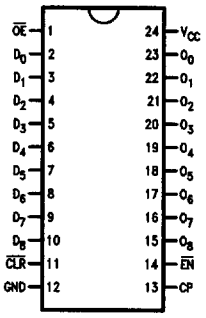
Connection Diagram

Pin Assignment for DIP and SOIC



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Functional Description

The 'FCT823A/B consists of nine D-type edge-triggered flip-flops. These have TRI-STATE® outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

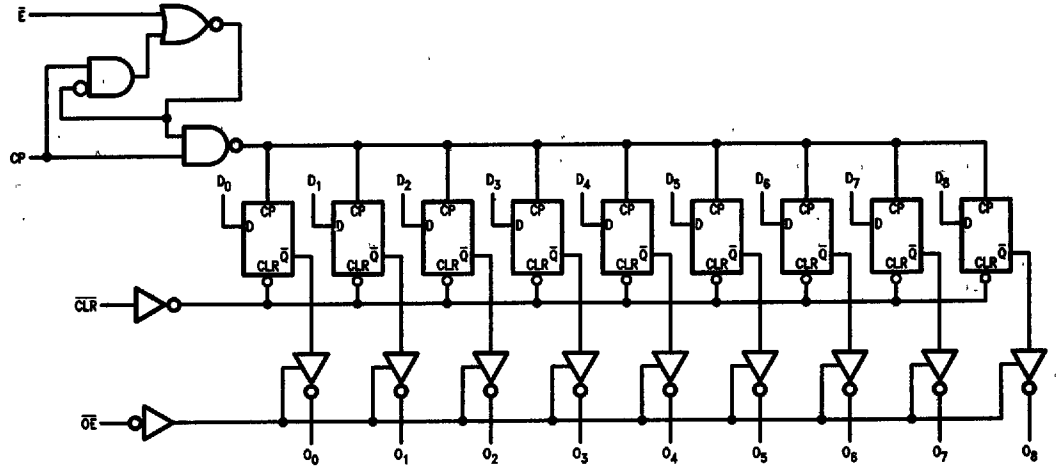
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
74FCTA/B −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
74FCTA/B −55°C to +125°C

Storage Temperature (T_{STG})
74FCTA/B −55°C to +125°C

Power Dissipation (P_T) 0.5W

DC Output Current ((I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCTA/B 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
74FCTA/B −0°C to +70°C

Junction Temperature (T_J)
PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCTA/B Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA/B Min	74FCTA/B Typ	74FCTA/B Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	µA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	µA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	µA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−75	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8 V_{HC} 2.4 2.4	3.0 V_{CC} 4.3 4.3		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 µA V_{CC} = Min; V_{IN} = V_{IH} or V_{IL}	 I_{OH} = −300 µA I_{OL} = −24 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.5 0.5	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 µA V_{CC} = Min; V_{IN} = V_{IH} or V_{IL}	 I_{OH} = 300 µA I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.2	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = f_{CP} = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)			0.35	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	 $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

DC Characteristics for 'FCTA/B Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA/B			Units	Conditions	
		Min	Typ	Max			
I_C	Total Power Supply Current (Note 6)			4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				6.0			V_{IN} = 3.4V V_{IN} = GND
				9.5		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter is guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	Test Conditions	74FCTA T_A, V_{CC} = Com		74FCTB T_A, V_{CC} = Com		Units	Fig. No.
			Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to On ($\overline{OE}$ = Low)	C_L = 50 pF R_L = 500Ω		10.0		7.5	ns	2-9
		C_L = 300 pF (Note 1) R_L = 500Ω		20.0		15.0	ns	2-9
t_{SU}	Data to C_p Setup Time	C_L = 50 pF R_L = 500Ω	4.0		3.0		ns	2-10
t_H	Data to C_P Hold Time		2.0		1.5		ns	2-10
t_{SU}	Enable ($\overline{EN}$ ⌐) to C_P Setup Time		4.0		2.0		ns	2-10
t_H	Enable ($\overline{EN}$) Hold Time		2.0		1.5		ns	2-10
t_{PHL}	Propagation Delay Clear to O_1			14.0		9.0	ns	2-10
t_{REC}	Clear Recovery ($\overline{CLR}$ ⌐) Time		6.0		6.0		ns	2-10
t_P	Clock Pulse Width		7.0		6.0		ns	2-9
t_P	Clear ($\overline{CLR}$ = Low) Pulse Width		6.0		6.0		ns	2-9
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ ⌐ to On	C_L = 50 pF R_L = 500Ω		12.0		8.0	ns	2-11
		C_L = 300 pF (Note 1) R_L = 500Ω		23.0		15.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ ⌐ to On	C_L = 5 pF (Note 1) R_L = 500Ω		7.0		6.5	ns	2-11
		C_L = 50 pF R_L = 500Ω		8.0		7.5	ns	2-11

Note 1: These parameters are guaranteed but not tested.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Note 1: This parameter is measured at characterization but not tested.

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