

T-52-31 54AC16834, 54ACT16834
 74AC16834, 74ACT16834
 DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS
 TI0271—D3547, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C

54AC16834, 54ACT16834 ... WD PACKAGE
 74AC16834, 74ACT16834 ... DL PACKAGE
 (TOP VIEW)

10EB	1	56	10EA
1CLK	2	55	1CLR
1ERR	3	54	1PARITY
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V _{CC}	7	50	V _{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V _{CC}	22	35	V _{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2ERR	26	31	2PARITY
2CLK	27	30	2CLR
20EB	28	29	20EA

description

The 'AC16834 and 'ACT16834 contain two inverting 8-bit to 9-bit parity bus transceivers. For each transceiver, when data is transmitted from the A bus to the B bus, an odd-parity bit is generated and output on the parity I/O pin (1PARITY or 2PARITY). When data is transmitted from the B bus to the A bus, 1PARITY (or 2PARITY) is configured as an input and combined with the B input data to generate an active-low error flag if odd parity is not detected.

The error output (1ERR or 2ERR) is configured as an open-collector output. The B-to-A parity error flag is clocked into 1ERR (or 2ERR) on the low-to-high transition of 1CLK (or 2CLK). 1ERR (or 2ERR) is cleared (set high) by taking the clear input 1CLR (or 2CLR) low.

The 74AC16834 and 74ACT16834 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16834 has CMOS-compatible input thresholds. The 'ACT16834 has TTL-compatible input thresholds.

The 54AC16834 and 54ACT16834 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16834 and 74ACT16834 are characterized for operation from -40°C to 85°C.

PRODUCT PREVIEW

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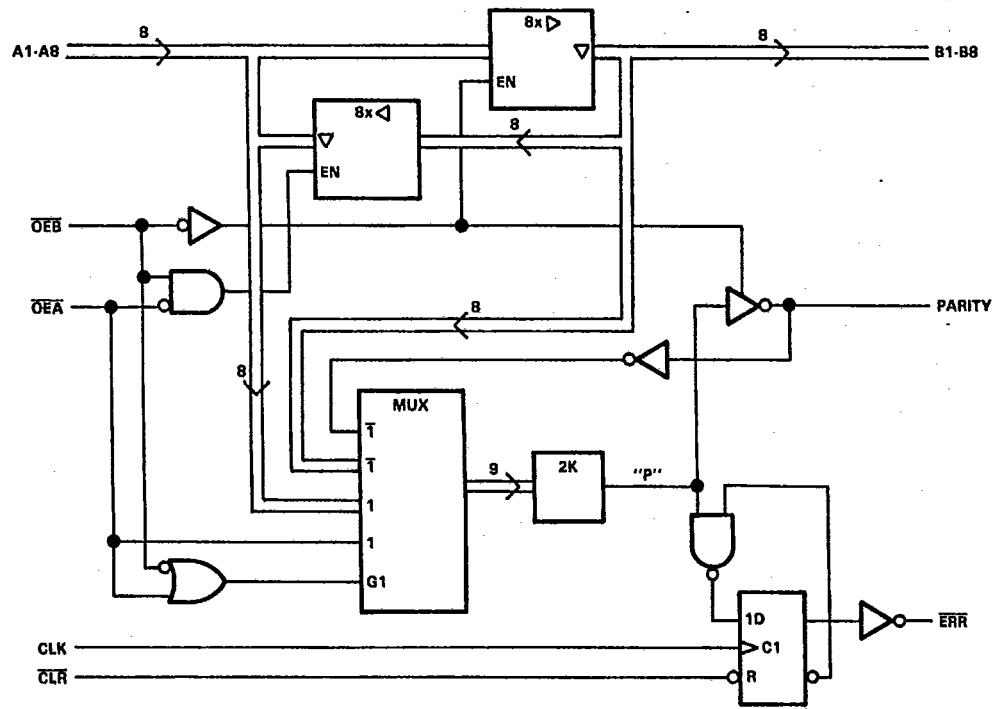


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D3547, JUNE 1990—T10271

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logic diagram, each transceiver (positive logic)



PRODUCT PREVIEW



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