DRAF123J

Silicon PNP epitaxial planar type

For digital circuits Complementary to DRCF123J DRA3123J in ML3 type package

■ Features

- ullet Low collector-emitter saturation voltage $V_{\text{CE(sat)}}$
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

■ Packaging

DRAF123J0L Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Collector-base voltage (Emitter open)	V _{CBO}	-50	V	
Collector-emitter voltage (Base open)	V _{CEO}	-50	V	
Collector current	I_{C}	-100	mA	
Total power dissipation *	P _T	100	mW	
Junction temperature	T_j	150	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

Note) *: Copper plate at the collector is 5.0 mm^2 on substrate at $10 \text{ mm} \times 12 \text{ mm} \times 0.8 \text{ mm}$.

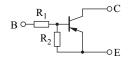
■ Package

• Code

ML3-N4-B

Package dimension clicks here.→

- Pin Name
 - 1: Base
 - 2: Emitter
 - 3: Collector
- Marking Symbol: L4
- Internal Connection



Resistance value	R_1	2.2	kΩ
	R_2	47	kΩ

■ Electrical Characteristics $T_a = 25$ °C±3°C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_{\rm C} = -10 \mu\text{A}, I_{\rm E} = 0$	-50			V
Collector-emitter voltage (Base open)	V _{CEO}	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{\rm CB} = -50 \text{ V}, I_{\rm E} = 0$			-0.1	μΑ
Collector-emitter cutoff current (Base open)	I _{CEO}	$V_{CE} = -50 \text{ V}, I_{B} = 0$			-0.5	μΑ
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -6 \text{ V}, I_C = 0$			-0.2	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = -10 \text{ V}, I_{C} = -5 \text{ mA}$	80			_
Collector-emitter saturation voltage	V _{CE(sat)}	$I_C = -10 \text{ mA}, I_B = -0.5 \text{ mA}$			-0.25	V
Input voltage (ON)	V _{I(on)}	$V_{CE} = -0.2 \text{ V}, I_{C} = -5 \text{ mA}$	-1.2			V
Input voltage (OFF)	V _{I(off)}	$V_{CE} = -5 \text{ V}, I_{C} = -100 \mu\text{A}$			-0.4	V
Input resistance	R_1		-30%	2.2	+30%	kΩ
Resistance ratio	R_1/R_2		0.037	0.047	0.057	_

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

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