

SN54ALS652, SN54ALS653, SN54AS651, SN54AS652 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

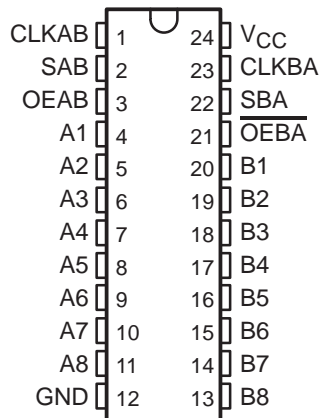
DEVICE	A OUTPUT	B OUTPUT	LOGIC
SN74ALS651A, 'AS651	3 State	3 State	Inverting
SN54ALS652, SN74ALS652A, 'AS652	3 State	3 State	True
'ALS653	Open Collector	3 State	Inverting
SN74ALS654	Open Collector	3 State	True

description

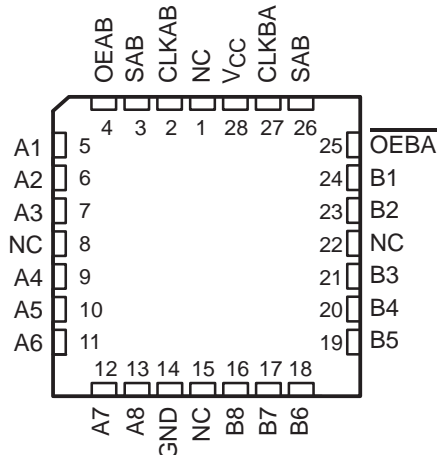
These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

**SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)**



**SN54ALS', SN54AS' . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
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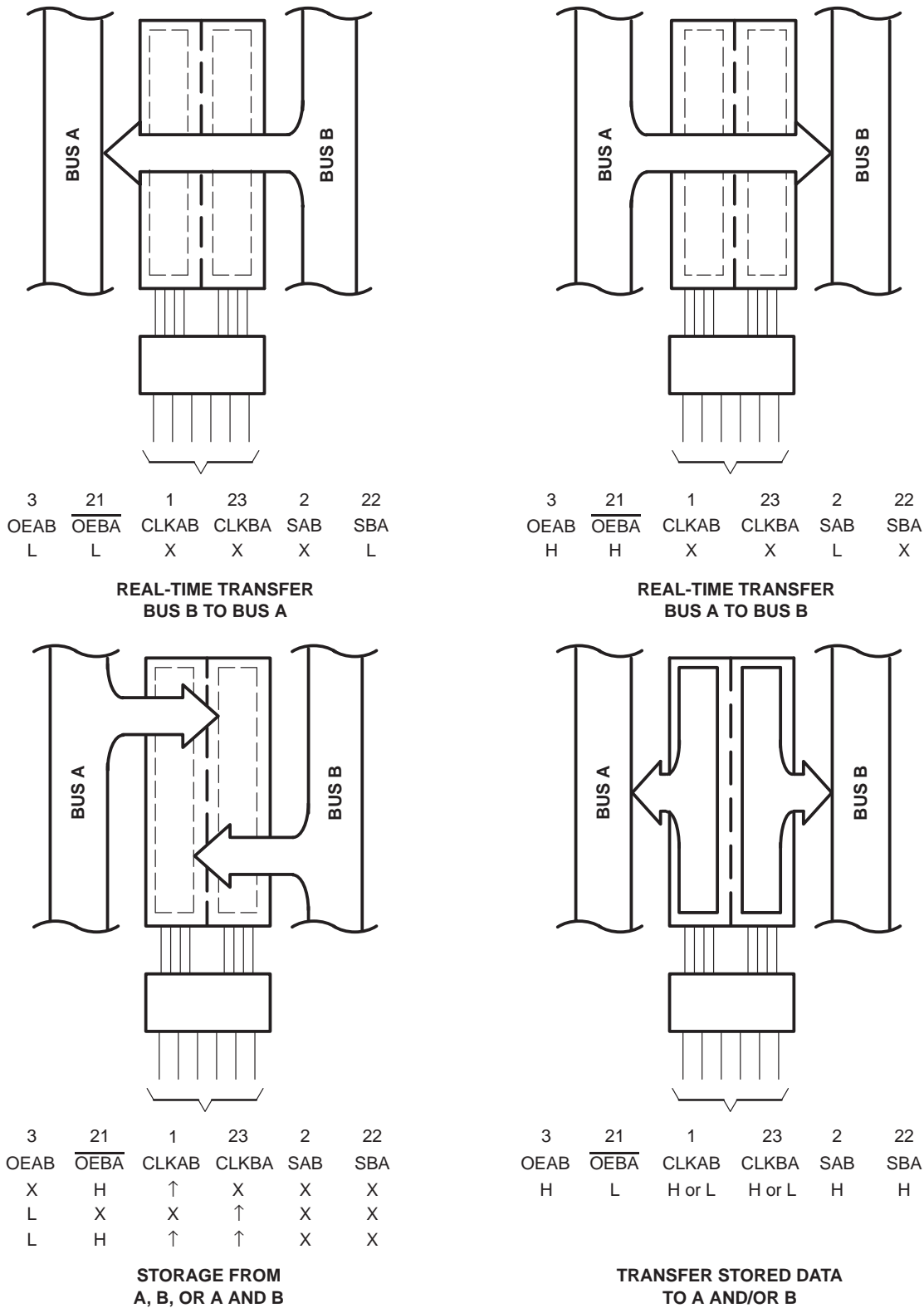
description (continued)

The -1 versions of the SN74ALS651A and SN74ALS652A are identical to the standard versions except that the recommended maximum I_{OL} for the -1 versions is increased to 48 mA. There are no -1 versions of the SN54ALS652, SN54ALS653, SN74ALS653, and SN74ALS654.

The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS' and SN74AS' families are characterized for operation from 0°C to 70°C .

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Pin numbers are for the DW, JT, and NT packages.

Figure 1. Bus-Management Functions

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
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FUNCTION TABLES

**SN54ALS653, SN54AS651,
SN74ALS651A, SN74ALS653, SN74AS651**

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

**SN54ALS652, SN54AS652,
SN74ALS652A, SN74ALS654, SN74AS652**

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

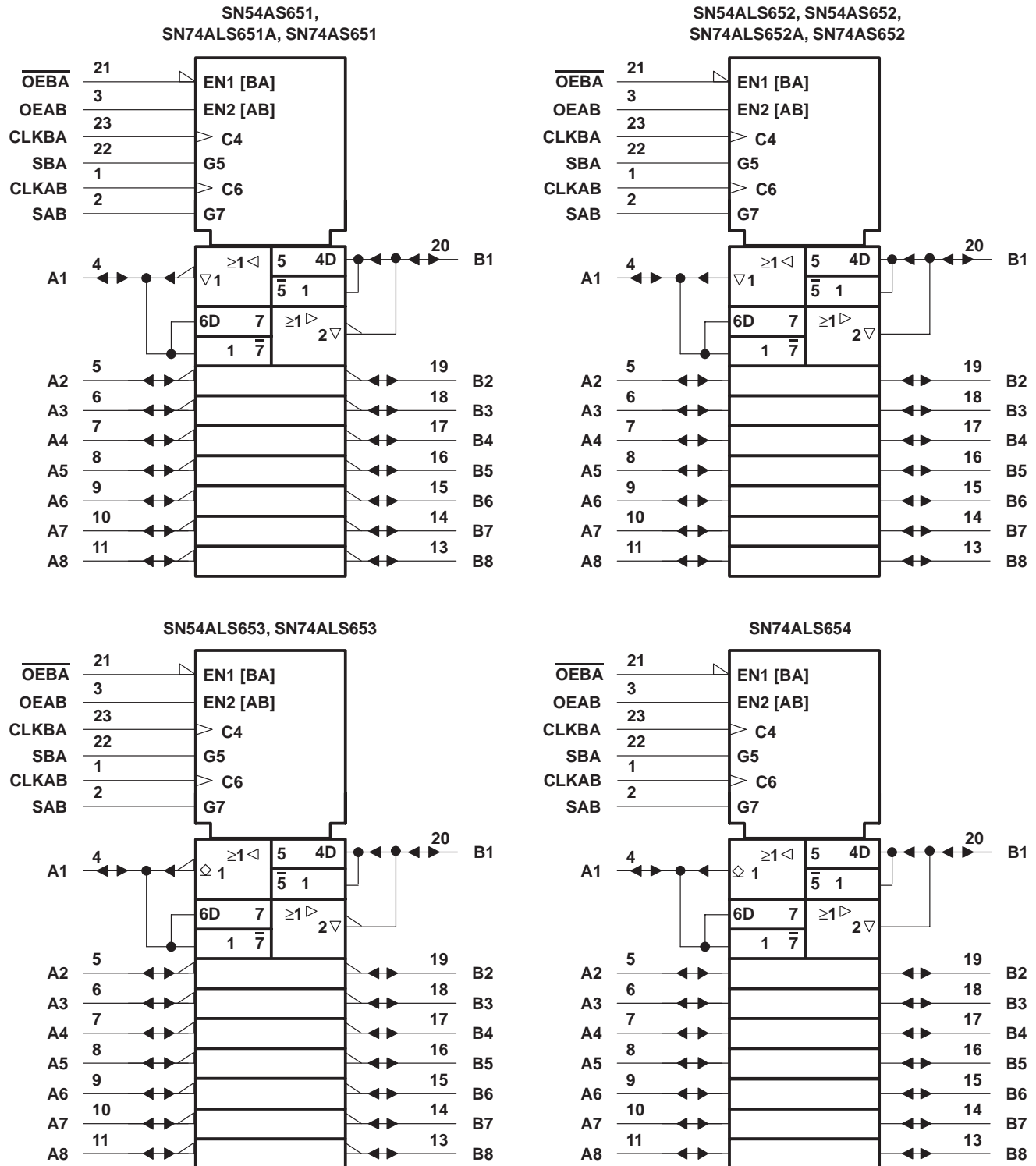
Select control = H; clocks must be staggered to load both registers.



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logic symbols†

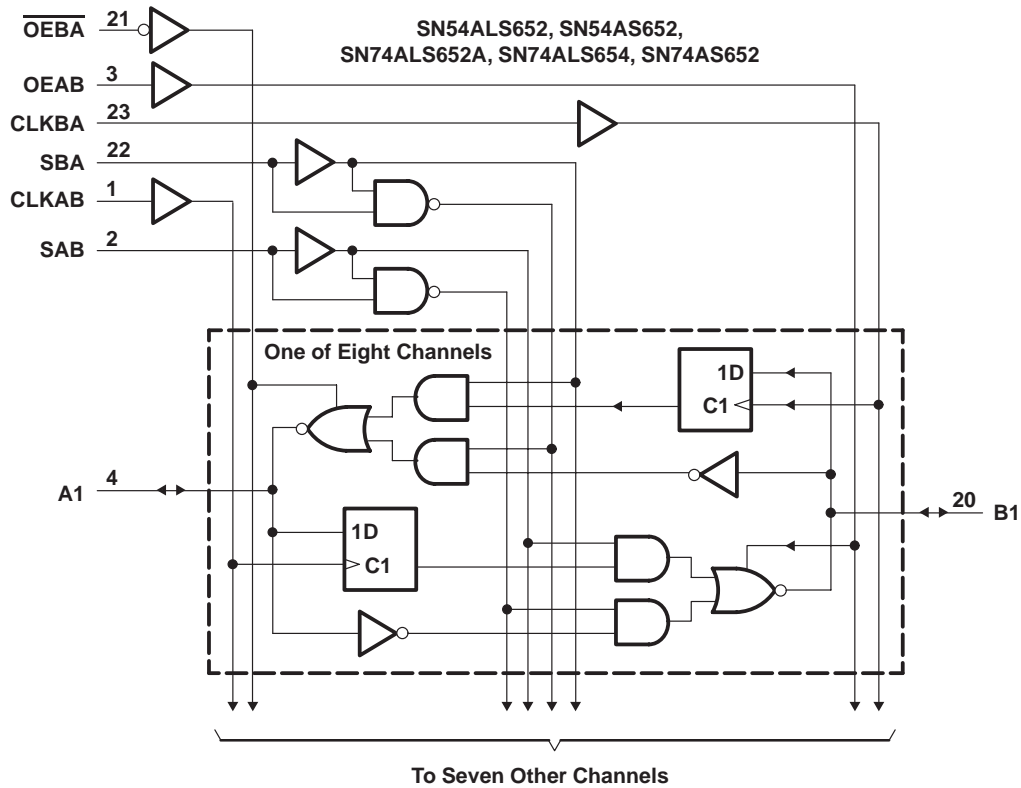
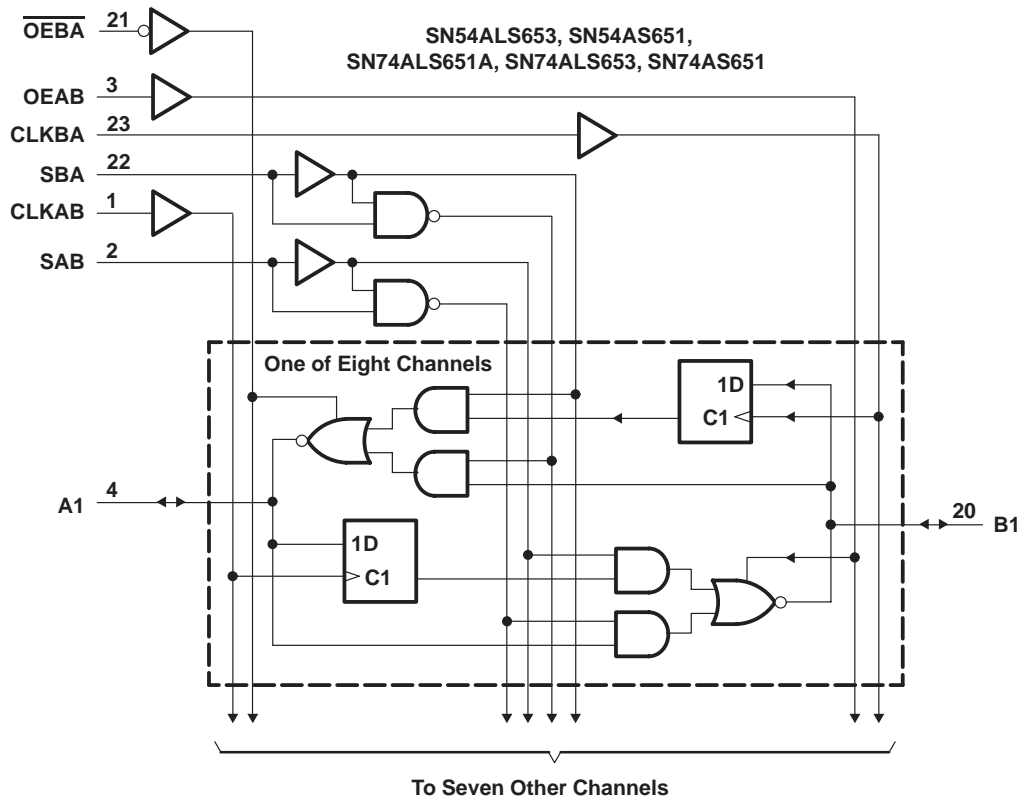


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

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logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS652	–55°C to 125°C
SN74ALS651A, SN74ALS652A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS651A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			24	mA
				48‡	
f_{clock}	Clock frequency	0		40	MHz
t_w	Pulse duration	CLKBA or CLKAB high	12.5		ns
		CLKBA or CLKAB low	12.5		
t_{su}	Setup time before CLKAB↑ or CLKBA↑	A or B	10		ns
t_h	Hold time after CLKAB↑ or CLKBA↑	A or B	0		ns
T_A	Operating free-air temperature		0	70	°C

‡ Applies only to the SN74ALS651A-1 and only if V_{CC} is maintained between 4.75 V and 5.25 V

recommended operating conditions

		SN54ALS652			SN74ALS652A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
							48‡	
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration	CLKBA or CLKAB high	14.5		12.5			ns
		CLKBA or CLKAB low	14.5		12.5			
t_{su}	Setup time before CLKAB↑ or CLKBA↑	A or B	15		10			ns
t_h	Hold time after CLKAB↑ or CLKBA↑	A or B	5		0			ns
T_A	Operating free-air temperature		–55	125		0	70	°C

‡ Applies only to the SN74ALS652A-1 and only if V_{CC} is maintained between 4.75 V and 5.25 V



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74ALS651A			UNIT
		MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	V
		$I_{OL} = 24\text{ mA}$	0.35	0.5	
	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 48\text{ mA (-1 versions)}$	0.35	0.5		
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$		0.1	mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$		20	μA
	A or B ports‡			20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$		-0.2	mA
	A or B ports‡			-0.2	
$I_{O§}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	42	68	mA
		Outputs low	52	82	
		Outputs disabled	52	82	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS652		SN74ALS652A		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	2.4		3.2
		$I_{OH} = -12\text{ mA}$	2				
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V
		$I_{OL} = 24\text{ mA}$			0.35	0.5	
	$V_{CC} = 4.75\text{ V}$, $I_{OL} = 48\text{ mA}$ (-1 versions)			0.35		0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$	0.1		0.1		mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$	0.1		0.1		
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$	20		20		μA
	A or B ports‡		20		20		
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$	-0.2		-0.2		mA
	A or B ports‡		-0.2		-0.2		
$I_{O\S}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA	
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	47	76	47	76	mA
		Outputs low	55	88	55	88	
		Outputs disabled	55	88	55	88	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
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switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS651A		
			MIN	MAX	
f _{max}			40		MHz
t _{PLH}	CLKBA or CLKAB	A or B	8	32	ns
t _{PHL}			5	17	
t _{PLH}	A or B	B or A	2	18	ns
t _{PHL}			2	10	
t _{PLH}	SBA or SAB‡ (with A or B high)	A or B	8	38	ns
t _{PHL}			6	21	
t _{PLH}	SBA or SAB‡ (with A or B low)	A or B	8	25	ns
t _{PHL}			7	21	
t _{PZH}	\overline{OEBA}	A	3	20	ns
t _{PZL}			5	18	
t _{PHZ}	\overline{OEBA}	A	2	9	ns
t _{PLZ}			3	12	
t _{PZH}	OEAB	B	3	22	ns
t _{PZL}			6	21	
t _{PHZ}	OEAB	B	2	12	ns
t _{PLZ}			2	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.



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switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS652		SN74ALS652A		
			MIN	MAX	MIN	MAX	
t _{max}			35		40	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	10	35	8	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A or B	B or A	5	20	4	18	ns
t _{PHL}			3	15	3	12	
t _{PLH}	SBA or SAB‡ (with A or B high)	A or B	15	40	8	35	ns
t _{PHL}			6	23	6	20	
t _{PLH}	SBA or SAB‡ (with A or B low)	A or B	8	30	8	25	ns
t _{PHL}			5	24	5	20	
t _{PZH}	\overline{OEBA}	A	3	20	3	17	ns
t _{PZL}			5	22	5	18	
t _{PHZ}	\overline{OEBA}	A	1	12	1	10	ns
t _{PLZ}			2	20	2	16	
t _{PZH}	OEAB	B	8	25	3	22	ns
t _{PZL}			6	21	5	18	
t _{PHZ}	OEAB	B	1	12	1	10	ns
t _{PLZ}			2	21	2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : All inputs and A I/O ports	7 V
B I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS653	–55°C to 125°C
SN74ALS653, SN74ALS654	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS653			SN74ALS653			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
V_{OH}	High-level output voltage	A ports		5.5	5.5		V	
I_{OH}	High-level output current	B ports		–12	–15		mA	
I_{OL}	Low-level output current			12	24		mA	
f_{clock}	Clock frequency	0		25	0		35	MHz
t_w	Pulse duration	CLKBA or CLKAB high		20	14.5		ns	
		CLKBA or CLKAB low		20	14.5			
t_{su}	Setup time before CLKAB↑ or CLKBA↑	A or B		15	10		ns	
t_h	Hold time after CLKAB↑ or CLKBA↑	A or B		5	0		ns	
T_A	Operating free-air temperature	–55		125	0		70	°C

recommended operating conditions

		SN74ALS654			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage	0.8			V
V_{OH}	High-level output voltage	A ports		5.5	V
I_{OH}	High-level output current	B ports		–15	mA
I_{OL}	Low-level output current			24	mA
f_{clock}	Clock frequency	0		35	MHz
t_w	Pulse duration	CLKBA or CLKAB high		14.5	ns
		CLKBA or CLKAB low		14.5	
t_{su}	Setup time before CLKAB↑ or CLKBA↑	A or B		10	ns
t_h	Hold time after CLKAB↑ or CLKBA↑	A or B		0	ns
T_A	Operating free-air temperature	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS653		SN74ALS653		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA	-1.2		-1.2		V	
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2		V	
		V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.2	2.4		3.2
			I _{OH} = -12 mA	2				
			I _{OH} = -15 mA			2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
		I _{OL} = 24 mA			0.35	0.5		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA	
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1		0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA	
	A or B ports‡		20		20			
I _{IL}	Control inputs	V _{CC} = 5.5 V, V _I = 0.4 V	-0.2		-0.2		mA	
	A or B ports‡		-0.2		-0.2			
I _{OH}	A ports	V _{CC} = 4.5 V, V _{OH} = 5.5 V	0.1		0.1		mA	
I _O §	B ports	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112	mA	
I _{CC}		V _{CC} = 5.5 V	Outputs high	47	76	47	76	mA
			Outputs low	55	88	55	88	
			Outputs disabled	55	88	55	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS654			UNIT	
				MIN	TYP†	MAX		
V _{IK}		V _{CC} = 4.5 V,	I _I = -18 mA			-1.2	V	
V _{OH}	B ports	V _{CC} = 4.5 V to 5.5 V,		I _{OH} = -0.4 mA		V _{CC} -2		
		V _{CC} = 4.5 V	I _{OH} = -3 mA		2.4	3.2	V	
			I _{OH} = -15 mA		2			
V _{OL}		V _{CC} = 4.5 V		I _{OL} = 12 mA		0.25	0.4	
				I _{OL} = 24 mA		0.35		V
I _I	Control inputs	V _{CC} = 5.5 V,	V _I = 7 V			0.1	mA	
	A or B ports	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1		
I _{IH}	Control inputs	V _{CC} = 5.5 V,		V _I = 2.7 V		20		
	A or B ports‡					20		
I _{IL}	Control inputs	V _{CC} = 5.5 V,		V _I = 0.4 V		-0.2		
	A or B ports‡					-0.2		
I _{OH}	A ports	V _{CC} = 4.5 V,	V _{OH} = 5.5 V			0.1	mA	
I _O §	B ports	V _{CC} = 5.5 V,	V _O = 2.25 V	-30			-112	mA
I _{CC}	V _{CC} = 5.5 V		Outputs high		47	76	mA	
			Outputs low		55	88		
			Outputs disabled		55	88		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R ₁ = R ₂ = 500 Ω (B outputs), T _A = MIN to MAX†				UNIT
			SN54ALS653		SN74ALS653		
			MIN	MAX	MIN	MAX	
f _{max}			25		35		MHz
t _{PLH}	CLKBA	A	16	71	16	64	ns
t _{PHL}			6	24	6	22	
t _{PLH}	CLKAB	B	10	35	10	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A	B	5	20	5	18	ns
t _{PHL}			1.5	18	2	15	
t _{PLH}	B	A	8	63	12	56	ns
t _{PHL}			2	18	2	15	
t _{PLH}	SBA‡ (with B high)	A	12	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SBA‡ (with B low)	A	12	68	19	62	ns
t _{PHL}			5	27	5	25	
t _{PLH}	SAB‡ (with A high)	B	8	30	15	35	ns
t _{PHL}			6	25	6	22	
t _{PLH}	SAB‡ (with A low)	B	12	40	8	25	ns
t _{PHL}			6	25	6	22	
t _{PLH}	\overline{OEBA}	A	6	35	6	30	ns
t _{PHL}			6	27	6	24	
t _{PZH}	OEAB	B	7	25	8	22	ns
t _{PZL}			6	25	6	22	
t _{PHZ}	OEAB	B	1	16	1	14	ns
t _{PLZ}			2	21	2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω (A outputs), R ₁ = R ₂ = 500 Ω (B outputs), T _A = MIN to MAX†		UNIT
			SN74ALS654		
			MIN	MAX	
f _{max}			35		MHz
t _{PLH}	CLKBA	A	16	64	ns
t _{PHL}			6	22	
t _{PLH}	CLKAB	B	10	30	ns
t _{PHL}			5	17	
t _{PLH}	A	B	5	18	ns
t _{PHL}			2	15	
t _{PLH}	B	A	12	56	ns
t _{PHL}			2	21	
t _{PLH}	SBA‡ (with B low)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SBA‡ (with B high)	A	19	62	ns
t _{PHL}			5	25	
t _{PLH}	SAB‡ (with A low)	B	15	35	ns
t _{PHL}			6	22	
t _{PLH}	SAB‡ (with A high)	B	8	25	ns
t _{PHL}			6	22	
t _{PLH}	\overline{OEBA}	A	6	30	ns
t _{PHL}			6	24	
t _{PZH}	OEAB	B	6	22	ns
t _{PZL}			6	22	
t _{PHZ}	OEAB	B	1	14	ns
t _{PLZ}			2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54AS651, SN54AS652	–55°C to 125°C
SN74AS651, SN74AS652	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
f_{clock}^*	Clock frequency	0		75	0		90	MHz
t_w^*	Pulse duration	CLKBA or CLKAB high		6	5		ns	
		CLKBA or CLKAB low		7	6			
t_{su}^*	Setup time before CLKAB↑ or CLKBA↑	A or B		7	6		ns	
t_h^*	Hold time after CLKAB↑ or CLKBA	A or B		0	0		ns	
T_A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA		V _{CC} -2			V _{CC} -2			V
	V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.2		2.4	3.2		
		I _{OH} = -12 mA	2		2				
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 32 mA	0.25	0.5				V	
		I _{OL} = 48 mA				0.35	0.5		
I _I	Control inputs	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA
	A or B ports	V _{CC} = 5.5 V, V _I = 5.5 V	0.1			0.1			
I _{IH}	Control inputs	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA
	A or B ports‡		70			70			
I _{IL}	Control input	V _{CC} = 5.5 V, V _I = 0.4 V	-0.5			-0.5			mA
	A or B ports‡		-0.75			-0.75			
I _O §	V _{CC} = 5.5 V, V _O = 2.25 V		-30	-112	-30	-112	mA		
I _{CC}	'AS651	V _{CC} = 5.5 V	Outputs high	110	185	110	185	mA	
			Outputs low	120	195	120	195		
			Outputs disabled	130	195	130	195		
	'AS652	V _{CC} = 5.5 V	Outputs high	120	195	120	195		
			Outputs low	130	211	130	211		
			Outputs disabled	130	211	130	211		

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f _{max} *			75		90	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	2	11	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	12	2	8	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB‡	A or B	2	15	2	11	ns
t _{PHL}			2	11	2	9	
t _{PZH}	\overline{OEBA}	A	2	11	2	10	ns
t _{PZL}			3	18	3	16	
t _{PHZ}	\overline{OEBA}	A	2	10	2	9	ns
t _{PLZ}			2	10	2	9	
t _{PZH}	OEAB	B	3	12	3	11	ns
t _{PZL}			3	20	3	16	
t _{PHZ}	OEAB	B	2	11	2	10	ns
t _{PLZ}			2	12	2	11	

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
 SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V TO 5.5 V, C _L = 50 PF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN TO MAX†				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	TYP	MAX	
f _{max} *			75		90		MHz
t _{PLH}	CLKBA or CLKAB	A or B	2	11	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	12	2	9	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB‡	A or B	2	15	2	11	ns
t _{PHL}			2	11	2	9	
t _{PZH}	$\overline{\text{OEBA}}$	A	2	11	2	10	ns
t _{PZL}			3	18	3	16	
t _{PHZ}	$\overline{\text{OEBA}}$	A	2	10	2	9	ns
t _{PLZ}			2	10	2	9	
t _{PZH}	OEAB	B	3	12	3	11	ns
t _{PZL}			3	20	3	16	
t _{PHZ}	OEAB	B	2	11	2	10	ns
t _{PLZ}			2	12	2	11	

* On products compliant to MIL-PRF-38535, this parameter is based on characterized data but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

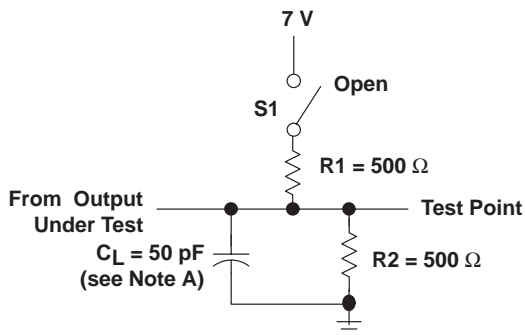
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.



**SN54ALS652, SN54ALS653, SN54AS651, SN54AS652
SN74ALS651A, SN74ALS652A, SN74ALS653, SN74ALS654, SN74AS651, SN74AS652
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS066F – DECEMBER 1983 – REVISED OCTOBER 1996

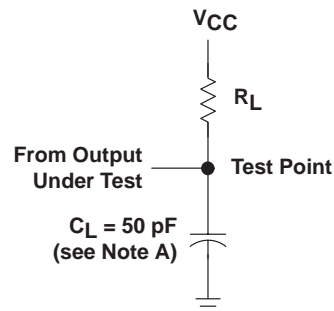
PARAMETER MEASUREMENT INFORMATION



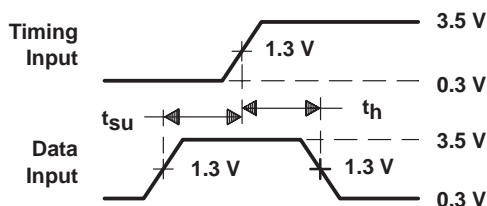
**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

SWITCH POSITION TABLE

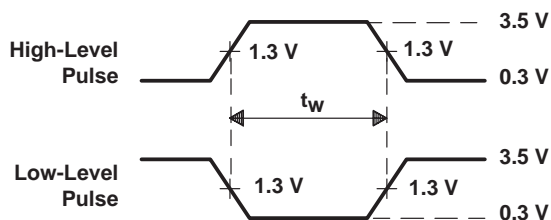
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



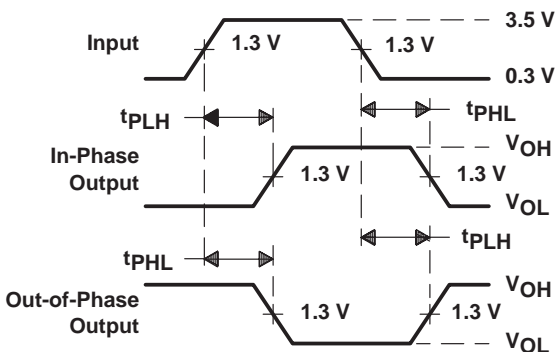
**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**



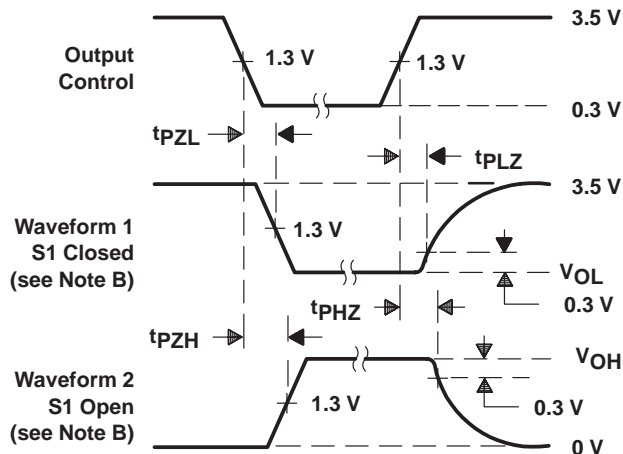
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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SN54ALS652, Octal Bus Transceivers And Registers With 3-State Outputs

Device Status: Active

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- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Related Documents](#)
- > [Training](#)

Parameter Name	SN54ALS652
Voltage Nodes (V)	5

Description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The -1 versions of the SN74ALS651A and SN74ALS652A are identical to the standard versions except that the recommended maximum I_{OL} for the -1 versions is increased to 48 mA. There are no -1 versions of the SN54ALS652, SN54ALS653, SN74ALS653, and SN74ALS654.

The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature

range of -55°C to 125°C. The SN74ALS' and SN74AS' families are characterized for operation from 0°C to 70°C.

Features

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [sdas066f.pdf](#) (331 KB)

Full datasheet in Zipped PostScript: [sdas066f.psz](#) (318 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
5962-8867301KA	<u>W</u>	24	-55 TO 125	OBSOLETE				
5962-8867301LA	<u>JT</u>	24	-55 TO 125	ACTIVE	10.27	1		Check stock or order
SN54ALS652JT	<u>JT</u>	24	-55 TO 125	ACTIVE	8.77	1		Check stock or order
SNJ54ALS652FK	<u>FK</u>	28	-55 TO 125	ACTIVE	16.28	1	5962-88673013A	Check stock or order
SNJ54ALS652JT	<u>JT</u>	24	-55 TO 125	ACTIVE	10.27	1	5962-8867301LA	Check stock or order
SNJ54ALS652W	<u>W</u>	24	-55 TO 125	OBSOLETE				

Application Reports

View Application Reports for Digital Logic

- [Advanced Schottky \(ALS and AS\) Logic Families \(SDAA010 - Updated: 08/01/1995\)](#)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(SCBA012A - Updated: 08/01/1997\)](#)
- [Designing With Logic \(SDYA009C - Updated: 06/01/1997\)](#)
- [Input And Output Characteristics Of Digital Integrated Circuits \(SDYA010 - Updated: 10/01/1996\)](#)
- [Live Insertion \(SDYA012 - Updated: 10/01/1996\)](#)

Related Documents

- [Documentation Rules \(SAP\) And Ordering Information \(SZZU001B, 4 KB - Updated: 05/06/1999\)](#)
- [Logic Selection Guide Second Half 2000 \(SDYU001N, 5035 KB - Updated: 04/17/2000\)](#)
- [MicroStar Junior BGA Design Summary \(SCET004, 284 KB - Updated: 07/28/2000\)](#)
- [More Power In Less Space - Technical Article \(SCAU001A, 850 KB - Updated: 03/01/1996\)](#)

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SN54ALS653, Octal Bus Transceivers And Registers With 3-State Outputs

Device Status: Active

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- > [Features](#)
- > [Datasheets](#)
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Parameter Name	SN54ALS653
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
No. of Outputs	8

Description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and **OEBA**) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store

data without using the internal D-type flip-flops by simultaneously enabling OEAB and **OEBA**. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The -1 versions of the SN74ALS651A and SN74ALS652A are identical to the standard versions except that the recommended maximum I_{OL} for the -1 versions is increased to 48 mA. There are no -1 versions of the SN54ALS652, SN54ALS653, SN74ALS653, and SN74ALS654.

The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' families are characterized for operation from 0°C to 70°C.

Features

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

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Datasheets

Full datasheet in Acrobat PDF: [sdas066f.pdf](#) (331 KB)

Full datasheet in Zipped PostScript: [sdas066f.psz](#) (318 KB)

Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
5962-89687013A	FK	28	-55 TO 125	ACTIVE	16.28	1		Check stock or order
SNJ54ALS653FK	FK	28	-55 TO 125	OBSOLETE				
SNJ54ALS653JT	JT	24	-55 TO 125	ACTIVE	10.27	1	5962-8968701LA	Check stock or order
SNJ54ALS653W	W	24	-55 TO 125	ACTIVE	13.36	1	5962-8968701KA	Check stock or order

Application Reports

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- [Advanced Schottky \(ALS and AS\) Logic Families \(SDAA010 - Updated: 08/01/1995\)](#)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(SCBA012A - Updated: 08/01/1997\)](#)
- [Designing With Logic \(SDYA009C - Updated: 06/01/1997\)](#)
- [Input And Output Characteristics Of Digital Integrated Circuits \(SDYA010 - Updated: 10/01/1996\)](#)
- [Live Insertion \(SDYA012 - Updated: 10/01/1996\)](#)

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- [Documentation Rules \(SAP\) And Ordering Information \(SZZU001B, 4 KB - Updated: 05/06/1999\)](#)
- [Logic Selection Guide Second Half 2000 \(SDYU001N, 5035 KB - Updated: 04/17/2000\)](#)
- [MicroStar Junior BGA Design Summary \(SCET004, 284 KB - Updated: 07/28/2000\)](#)
- [More Power In Less Space - Technical Article \(SCAU001A, 850 KB - Updated: 03/01/1996\)](#)

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SN54AS651, Octal Bus Transceivers And Registers With 3-State Outputs

Device Status: Active

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- > [Pricing/Samples/Availability](#)
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- > [Related Documents](#)
- > [Training](#)

Parameter Name	SN54AS651
Voltage Nodes (V)	5
Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
No. of Outputs	8

Description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store

data without using the internal D-type flip-flops by simultaneously enabling OEAB and . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

The -1 versions of the SN74ALS651A and SN74ALS652A are identical to the standard versions except that the recommended maximum I_{OL} for the -1 versions is increased to 48 mA. There are no -1 versions of the SN54ALS652, SN54ALS653, SN74ALS653, and SN74ALS654.

The SN54ALS' and SN54AS' families are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS' and SN74AS' families are characterized for operation from 0°C to 70°C.

Features

- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

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Datasheets

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Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
5962-88753013A	<u>FK</u>	28	-55 TO 125	ACTIVE	16.28	1		<u>Check stock or order</u>
5962-8875301KA	<u>W</u>	24	-55 TO 125	OBSOLETE				
SN54AS651JT	<u>JT</u>	24	-55 TO 125	ACTIVE	8.77	1		<u>Check stock or order</u>
SNJ54AS651JT	<u>JT</u>	24	-55 TO 125	ACTIVE	10.27	1	5962-8875301LA	<u>Check stock or order</u>

Application Reports

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- [Designing With Logic](#) (SDYA009C - Updated: 06/01/1997)
- [Input And Output Characteristics Of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

Related Documents

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- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 284 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

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SN54AS652, Octal Bus Transceivers And Registers With 3-State Outputs

Device Status: Active

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Parameter Name	SN54AS652
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Vcc range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
No. of Outputs	8

Description

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SN54AS652JT	<u>JT</u>	24	-55 TO 125	ACTIVE	8.77	1		Check stock or order
SNJ54AS652FK	<u>FK</u>	28	-55 TO 125	ACTIVE	16.28	1	5962-88687013A	Check stock or order
SNJ54AS652JT	<u>JT</u>	24	-55 TO 125	ACTIVE	10.27	1	5962-8868701LA	Check stock or order
SNJ54AS652W	<u>W</u>	24	-55 TO 125	OBSOLETE			5962-8868701KA	

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