

Document Title**128K x8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	July 3, 1996	Preliminary
1.0	Finalize - Increased I _{SB} , I _{DR} Commercial part = 10 μ A Industrial part = 20 μ A	December 16, 1996	Final
2.0	Revise - Change speed bin KM68V1000C Family: 70/85ns \rightarrow 70/100ns KM68U1000C Family: 70/100ns \rightarrow 85/100ns - Improved operating current: 40mA \rightarrow 35mA - Improved power dissipation PD: 0.7W \rightarrow 1.0W - Improved standby current Extended/Industrial: 20 \rightarrow 10 μ A - VIL: 0.4V \rightarrow 0.6V	November 25, 1997	Final

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128K x8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: 0.4µm CMOS
- Organization: 128K x8
- Power Supply Voltage:
 - KM68V1000C family: 3.0~3.6V
 - KM68U1000C family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-SOP-525, 32-TSOP1-0820F/R, 32-TSOP1-0813.4F/R

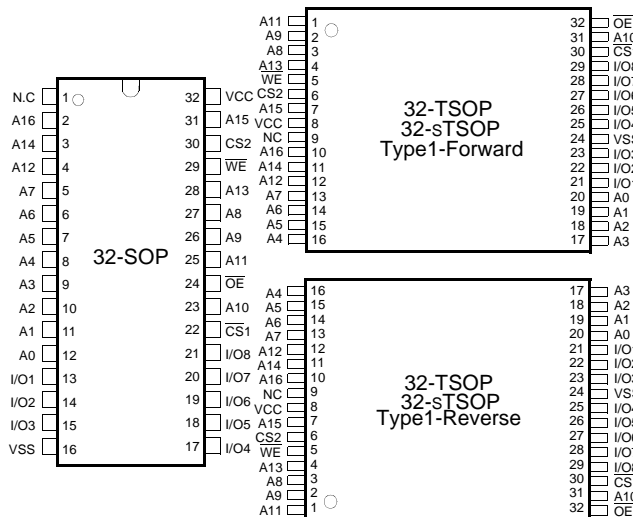
GENERAL DESCRIPTION

The KM68V1000C and KM68U1000C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

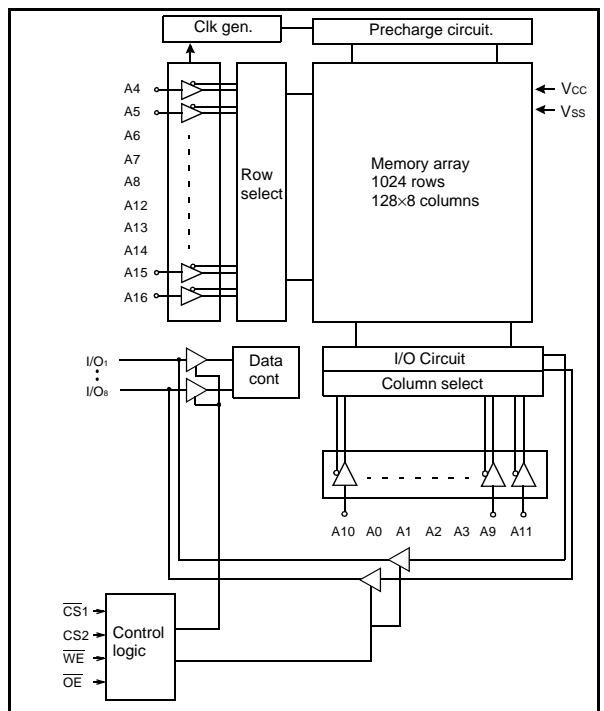
Product Family	Operating Temperature	Vcc Range(V)	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{sb1} , Max)	Operating (I _{cc2} , Max)	
KM68V1000CL-L	Commercial (0~70°C)	3.0~3.6V	70/100	10µA	35mA	32-SOP 32-TSOP1-F/R 32-sTSOP1-F/R
KM68U1000CL-L		2.7~3.3V	85/100			
KM68V1000CLE-L	Extended (-25~85°C)	3.0~3.6V	70/100			
KM68U1000CLE-L		2.7~3.3V	85/100			
KM68V1000CLI-L	Industrial (-40~85°C)	3.0~3.6V	70/100			
KM68U1000CLI-L		2.7~3.3V	85/100			

PIN DESCRIPTION



Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
A ₀ ~A ₁₆	Address Inputs
I/O ₁ ~I/O ₈	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
KM68V1000CLG-7L	32-SOP, 70ns, 3.3V	KM68V1000CLGE-7L	32-SOP, 70ns, 3.3V	KM68V1000CLGI-7L	32-SOP, 70ns, 3.3V
KM68V1000CLG-10L	32-SOP, 100ns, 3.3V	KM68V1000CLGE-10L	32-SOP, 100ns, 3.3V	KM68V1000CLGI-10L	32-SOP, 100ns, 3.3V
KM68V1000CLT-7L	32-TSOP F, 70ns, 3.3V	KM68V1000CLTE-7L	32-TSOP F, 70ns, 3.3V	KM68V1000CLTI-7L	32-TSOP F, 70ns, 3.3V
KM68V1000CLT-10L	32-TSOP F, 100ns, 3.3V	KM68V1000CLTE-10L	32-TSOP F, 100ns, 3.3V	KM68V1000CLTI-10L	32-TSOP F, 100ns, 3.3V
KM68V1000CLR-7L	32-TSOP R, 70ns, 3.3V	KM68V1000CLRE-7L	32-TSOP R, 70ns, 3.3V	KM68V1000CLRI-7L	32-TSOP R, 70ns, 3.3V
KM68V1000CLR-10L	32-TSOP R, 100ns, 3.3V	KM68V1000CLRE-10L	32-TSOP R, 100ns, 3.3V	KM68V1000CLRI-10L	32-TSOP R, 100ns, 3.3V
KM68U1000CLG-8L	32-SOP, 85ns, 3.0V	KM68U1000CLGE-8L	32-SOP, 85ns, 3.0V	KM68U1000CLGI-8L	32-SOP, 85ns, 3.0V
KM68U1000CLG-10L	32-SOP, 100ns, 3.0V	KM68U1000CLGE-10L	32-SOP, 100ns, 3.0V	KM68U1000CLGI-10L	32-SOP, 100ns, 3.0V
KM68U1000CLT-8L	32-TSOP F, 85ns, 3.0V	KM68U1000CLTE-8	32-TSOP F, 85ns, 3.0V	KM68U1000CLTI-8L	32-TSOP F, 85ns, 3.0V
KM68U1000CLT-10L	32-TSOP F, 100ns, 3.0V	KM68U1000CLTE-10L	32-TSOP F, 100ns, 3.0V	KM68U1000CLTI-10L	32-TSOP F, 100ns, 3.0V
KM68U1000CLR-8L	32-TSOP R, 85ns, 3.0V	KM68U1000CLRE-8	32-TSOP R, 85ns, 3.0V	KM68U1000CLRI-8L	32-TSOP R, 85ns, 3.0V
KM68U1000CLR-10L	32-TSOP R, 100ns, 3.0V	KM68U1000CLRE-10L	32-TSOP R, 100ns, 3.0V	KM68U1000CLRI-10L	32-TSOP R, 100ns, 3.0V
KM68V1000CLTG-7L	32-sTSOP F, 70ns, 3.3V	KM68V1000CLTGE-7L	32-sTSOP F, 70ns, 3.3V	KM68V1000CLTGI-7L	32-sTSOP F, 70ns, 3.3V
KM68V1000CLTG-10L	32-sTSOP F, 100ns, 3.3V	KM68V1000CLTGE-10L	32-sTSOP F, 100ns, 3.3V	KM68V1000CLTGI-10L	32-sTSOP F, 100ns, 3.3V
KM68V1000CLRG-7L	32-sTSOP R, 70ns, 3.3V	KM68V1000CLRGE-7L	32-sTSOP R, 70ns, 3.3V	KM68V1000CLRGI-7L	32-sTSOP R, 70ns, 3.3V
KM68V1000CLRG-10L	32-sTSOP R, 100ns, 3.3V	KM68V1000CLRGE-10L	32-sTSOP R, 100ns, 3.3V	KM68V1000CLRGI-10L	32-sTSOP R, 100ns, 3.3V
KM68U1000CLTG-8L	32-sTSOP F, 85ns, 3.0V	KM68U1000CLTGE-8L	32-sTSOP F, 85ns, 3.0V	KM68U1000CLTGI-8L	32-sTSOP F, 85ns, 3.0V
KM68U1000CLTG-10L	32-sTSOP F, 100ns, 3.0V	KM68U1000CLTGE-10L	32-sTSOP F, 100ns, 3.0V	KM68U1000CLTGI-10L	32-sTSOP F, 100ns, 3.0V
KM68U1000CLTG-8L	32-sTSOP R, 85ns, 3.0V	KM68U1000CLTGE-8L	32-sTSOP R, 85ns, 3.0V	KM68U1000CLTGI-8L	32-sTSOP R, 85ns, 3.0V
KM68U1000CLTG-10L	32-sTSOP R, 100ns, 3.0V	KM68U1000CLTGE-10L	32-sTSOP R, 100ns, 3.0V	KM68U1000CLTGI-10L	32-sTSOP R, 100ns, 3.0V

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O Pin	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low status.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68V1000CL/KM68U1000CL
		-25 to 85	°C	KM68V1000CLE/KM68U1000CLE
		-40 to 85	°C	KM68V1000CLI/KM68U1000CLI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM68V1000C Family	3.0	3.3	3.6	V
		KM68U1000C Family	2.7	3.0	3.3	
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM68V1000C, KM68U1000C Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	KM68V1000C, KM68U1000C Family	-0.3 ³⁾	-	0.6	V

- Commercial Product: T_A=0 to 70°C, unless otherwise specified
 Extended Product: T_A=-25 to 85°C, unless otherwise specified
 Industrial Product: T_A=-40 to 85°C, unless otherwise specified
- Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns
- Undershoot: -3.0V in case of pulse width ≤30ns
- Overshoot and undershoot is sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	6	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

- Capacitance is sampled, not 100% tested

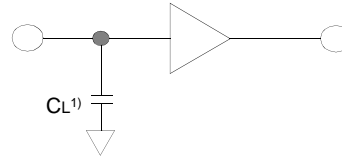
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH} , Read	-	2	5	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	1.5	5	mA
			Write	-	10	15	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IL} or V _{IH}	-	25	35	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IL} or V _{IH}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0~V _{CC}	-	0.3	10	μA	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load (see right): $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (Commercial product: $T_A = 0$ to 70°C , Extended product: $T_A = -25$ to 85°C , Industrial product: $T_A = -40$ to 85°C)

KM68V1000C Family: $V_{CC} = 3.0 \sim 3.6\text{V}$, KM68U1000C Family: $V_{CC} = 2.7 \sim 3.3\text{V}$)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	0	30	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns

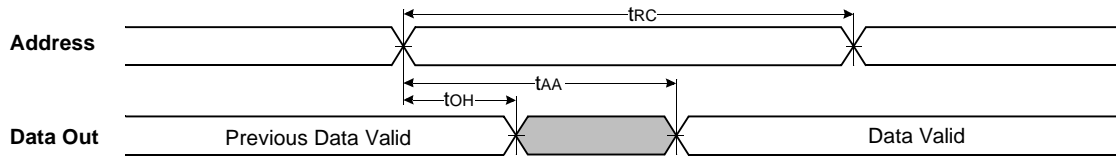
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition ¹⁾	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC} = 3.0\text{V}$, $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$, $CS_2 \geq V_{CC} - 0.2\text{V}$, or $CS_2 \leq 0.2\text{V}$	-	0.3	5	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

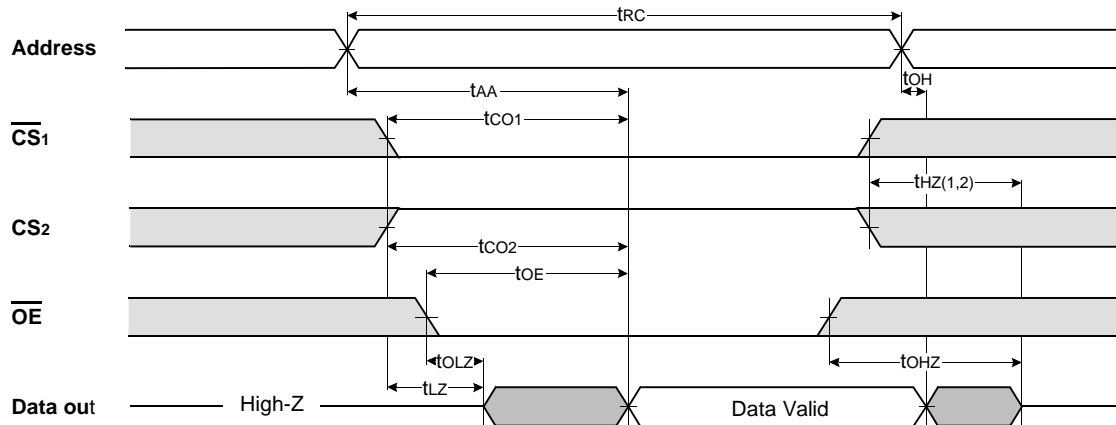
1. $CS_1 \geq V_{CC} - 0.2\text{V}$, $CS_2 \geq V_{CC} - 0.2\text{V}$, or $CS_2 \leq 0.2\text{V}$

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



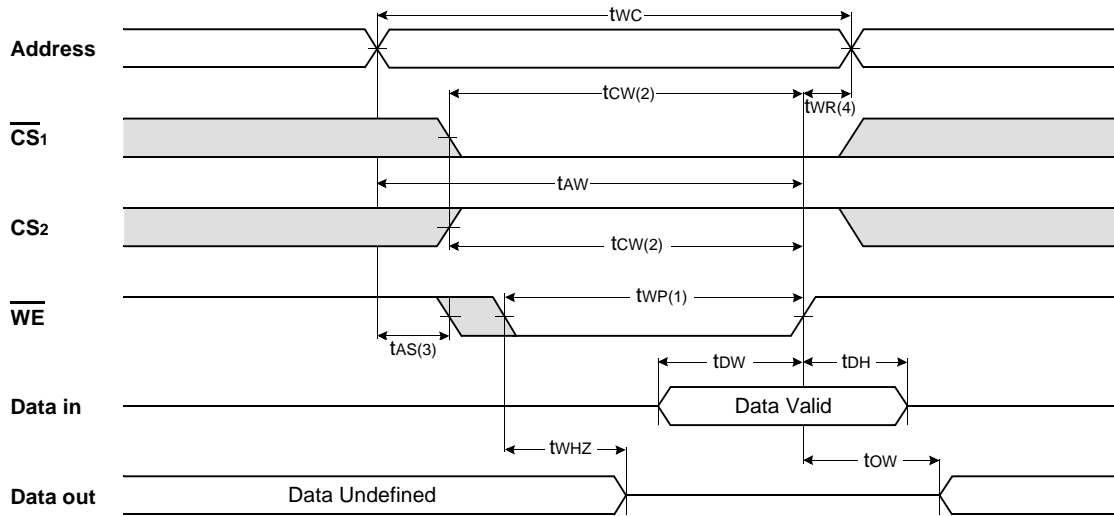
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



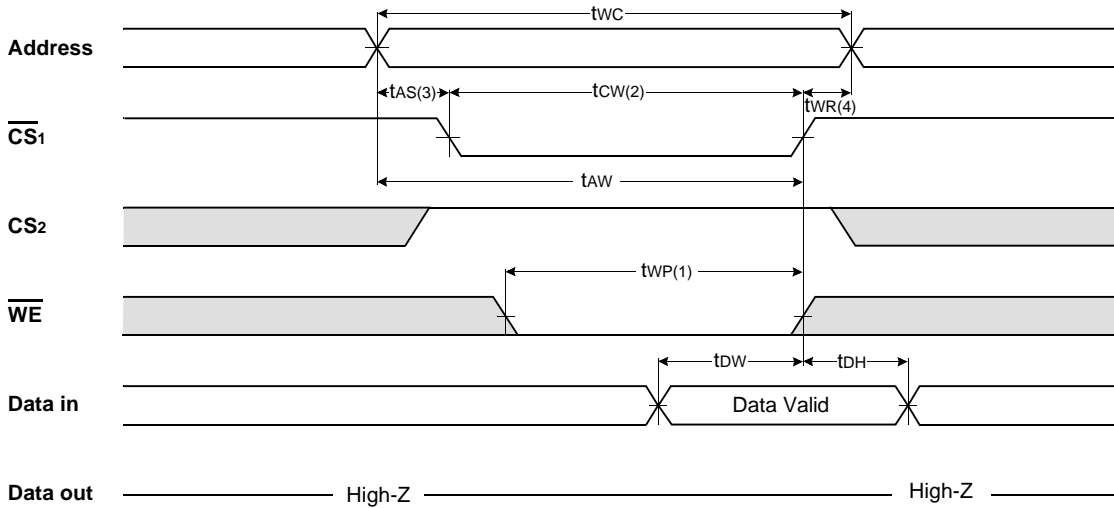
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

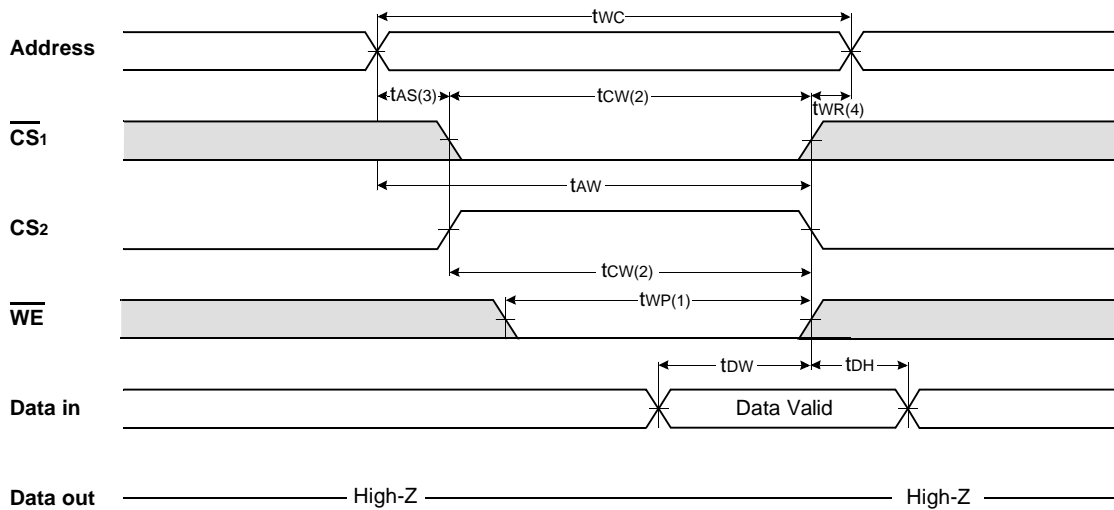
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

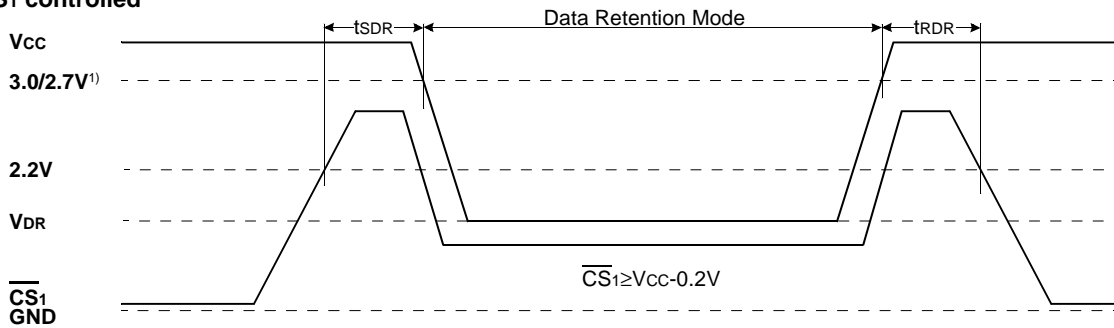


NOTES (WRITE CYCLE)

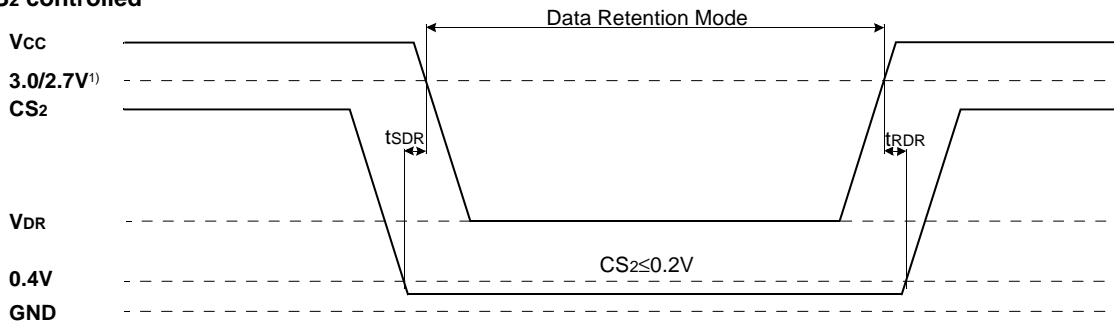
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low: A write ends at the earliest transition among \overline{CS}_1 going high, CS_2 going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as \overline{CS}_1 or \overline{WE} going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

\overline{CS}_1 controlled



CS_2 controlled

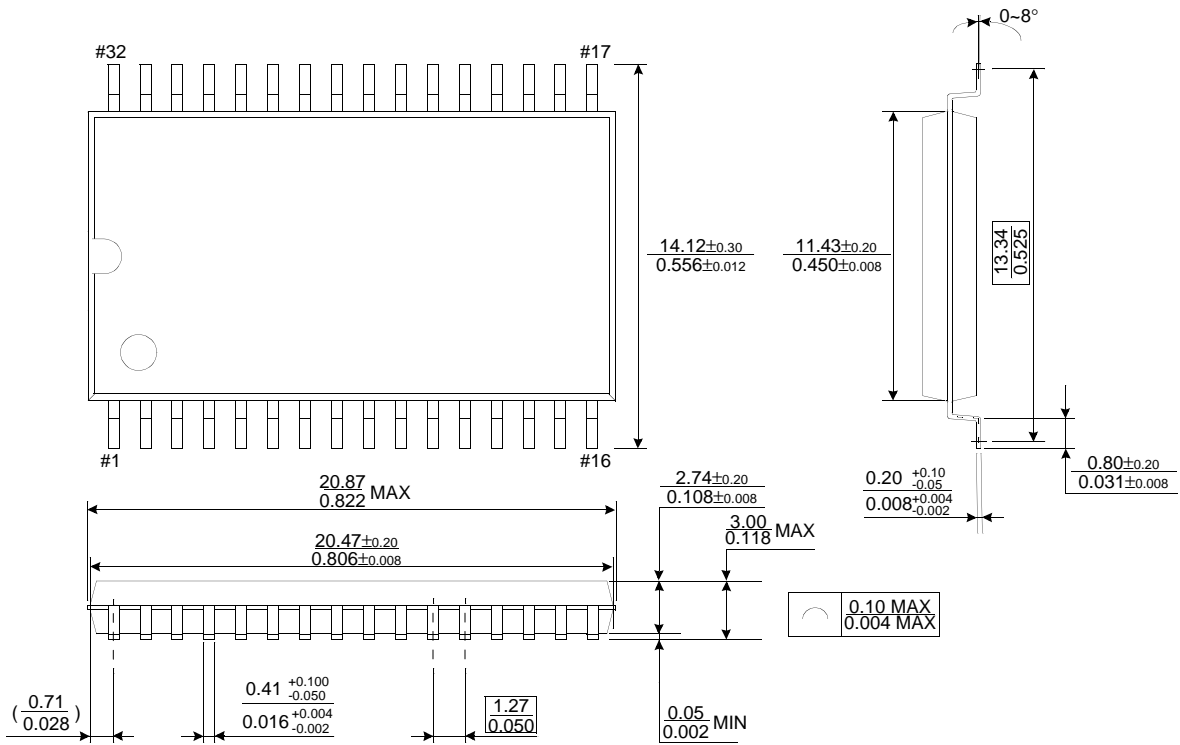


1. 3.0V for KM68V1000C Family, 2.7V for KM68U1000C Family

PACKAGE DIMENSIONS

Units: millimeter(inch)

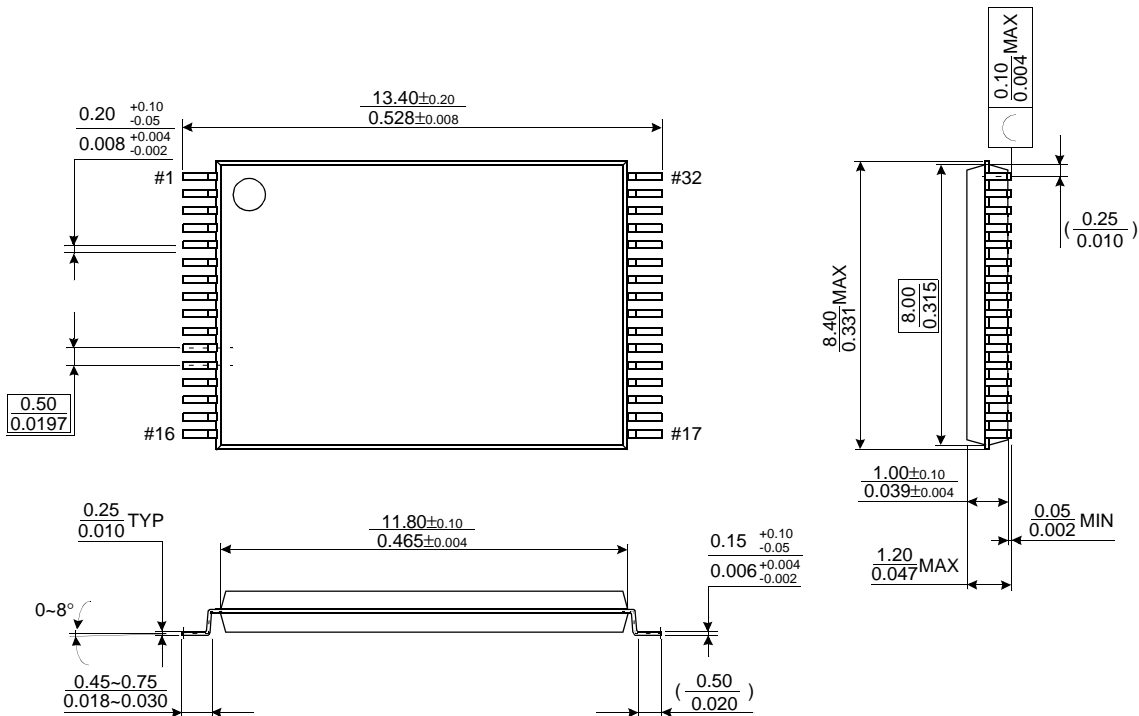
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



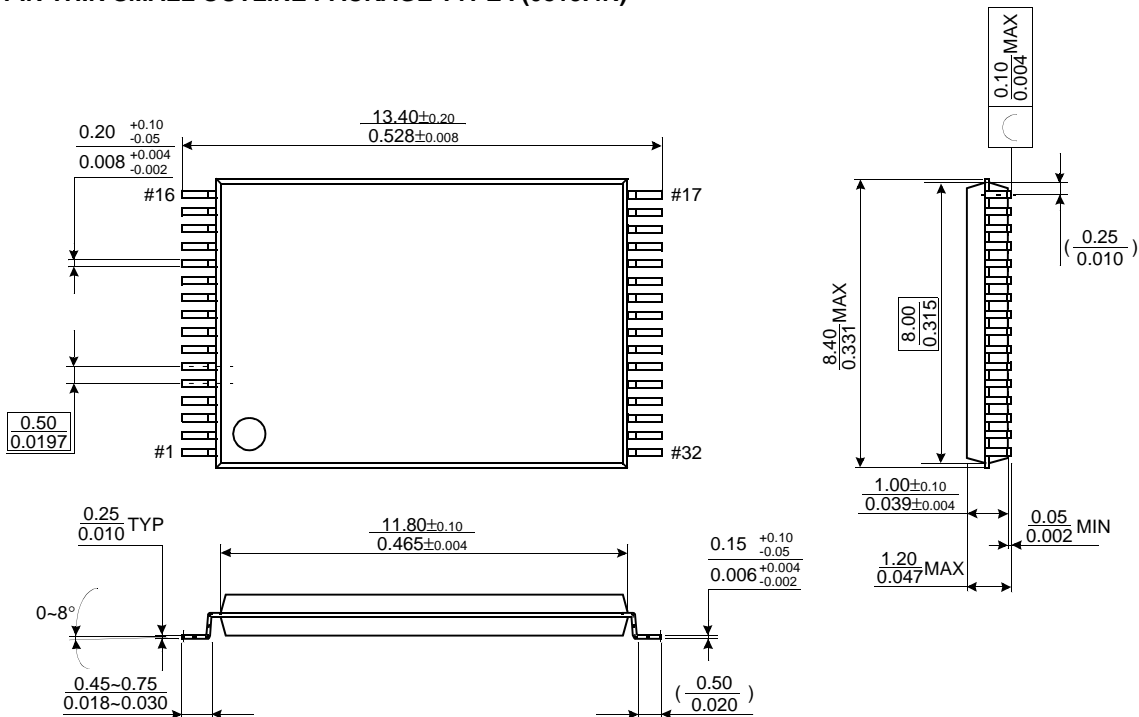
PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



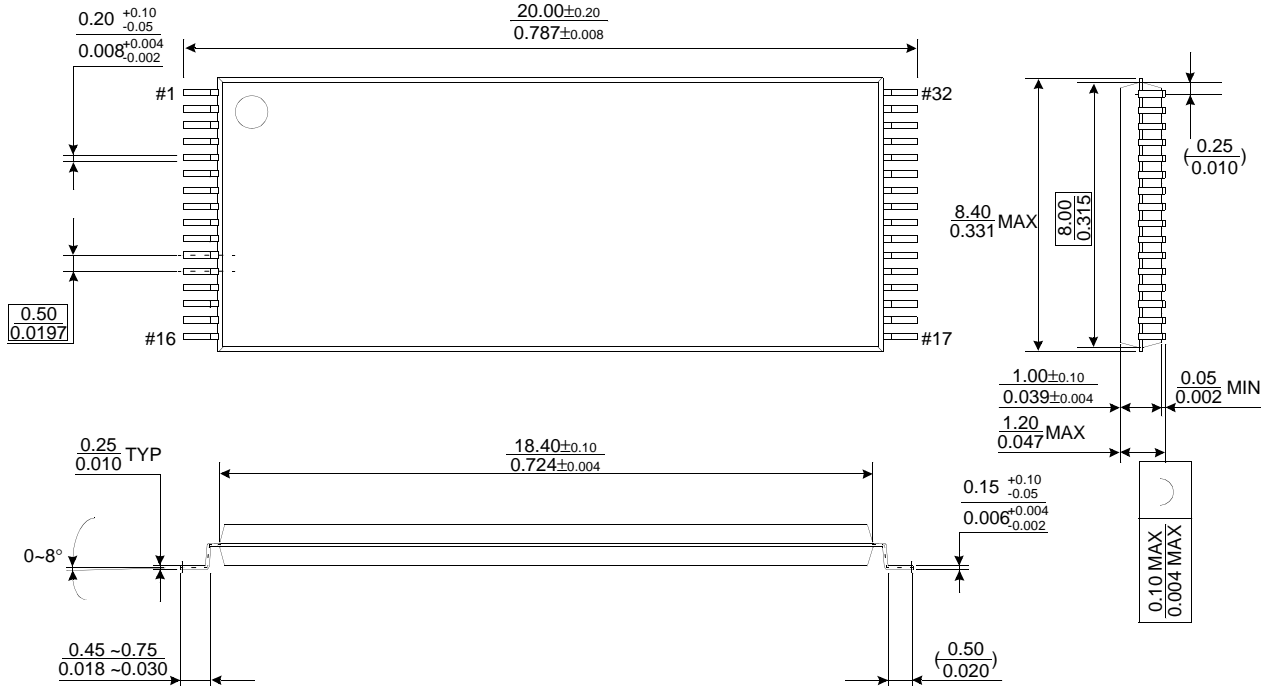
32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)



PACKAGE DIMENSIONS

Units: millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820R)

