

## Octal transceiver/register with dual enable (3-State)

74LVC652

**\*FEATURES**

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

**DESCRIPTION**

The 74LVC652 is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC652 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropriate clock inputs (CPAB or CPBA) regardless of the select inputs (SAB and SBA) or output enable (OEAB and OEBA) control inputs. Depending on the select inputs SAB and SBA data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OEn inputs this operating mode permits. The output enable inputs OEAB and OEBA determine the operation mode of the transceiver.

When OEAB is LOW, no data transmission from An to Bn is possible and when OEBA is HIGH, there is no data transmission from Bn to An possible. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each output reinforces its input.

**QUICK REFERENCE DATA**

GND = 0V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	C <sub>L</sub> = 50pF V <sub>CC</sub> = 3.3V	5.0	ns
f <sub>max</sub>	Maximum clock frequency		150	MHz
C <sub>I</sub>	Input capacitance		5.0	pF
C <sub>PD</sub>	Power dissipation capacitance per latch	Notes 1, 2	45	pF

**NOTES:**

- C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW)  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacitance in pF;  
 f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is V<sub>I</sub> = GND to V<sub>CC</sub>.

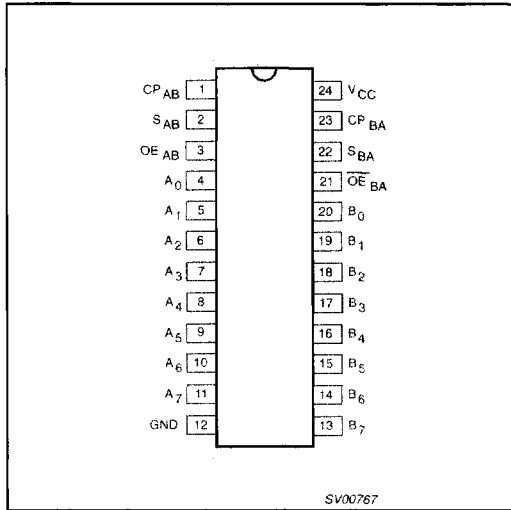
**ORDERING AND PACKAGE INFORMATION**

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to +85°C	74LVC652 D	74LVC652 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC652 DB	74LVC652 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC652 PW	4LVC652PW DH	SOT355-1

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## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP <sub>AB</sub>	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S <sub>AB</sub>	Select 'A' to 'B' source input
3	OE <sub>AB</sub>	Output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A <sub>0</sub> to A <sub>7</sub>	'A' data inputs/outputs
12	GND	Ground (0V)
13, 14, 15, 16, 17, 18, 19, 20	B <sub>0</sub> to B <sub>7</sub>	'B' data inputs/outputs
21	OE <sub>BA</sub>	Output enable A to B input
22	S <sub>BA</sub>	Select 'B' to 'A' source input
23	CP <sub>BA</sub>	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A <sub>0</sub> to A <sub>7</sub>	B <sub>0</sub> to B <sub>7</sub>	
L	H	H or L	H or L	X	X	input	input	isolation
L	H	↑	↑	X	X	input	input	store A and B data
X	H	↑	H or L	X	X	input	un *	store A, hold B,
H	H	↑	↑	L	X	input	output	store A in both registers
L	X	H or L	↑	X	X	un *	input	hold A, store B,
L	L	↑	↑	X	L	output	input	store B in both registers
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
H	H	X	X	L	X	input	output	real-time A data to B bus
H	H	H or L	X	H	X	input	output	stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

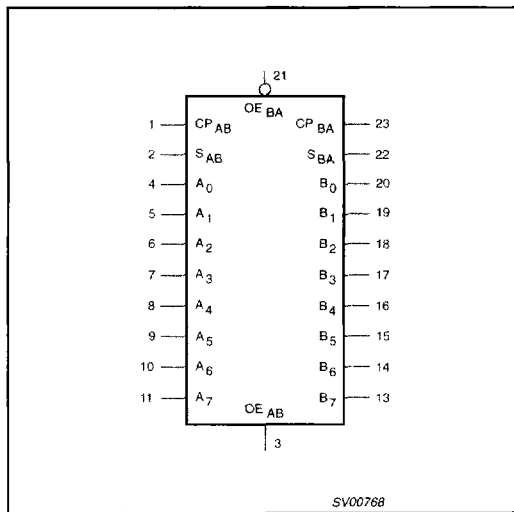
\* The data output functions may be enabled or disabled by various signals at the OE<sub>AB</sub> and OE<sub>BA</sub> inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

- un = unspecified
- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- ↑ = LOW-to-HIGH level transition

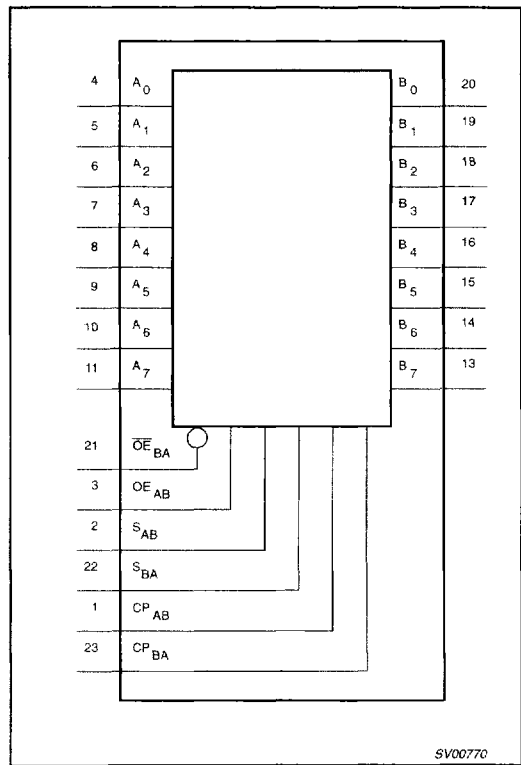
# Octal transceiver/register with dual enable (3-State)

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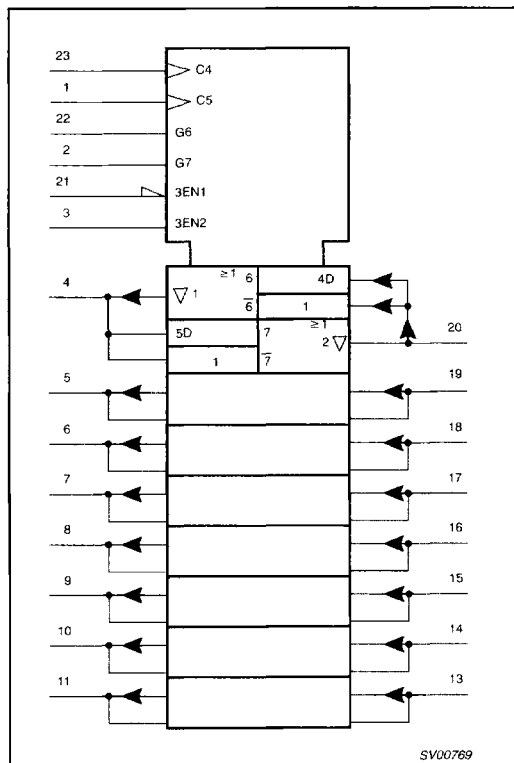
## LOGIC SYMBOL



## FUNCTIONAL DIAGRAM



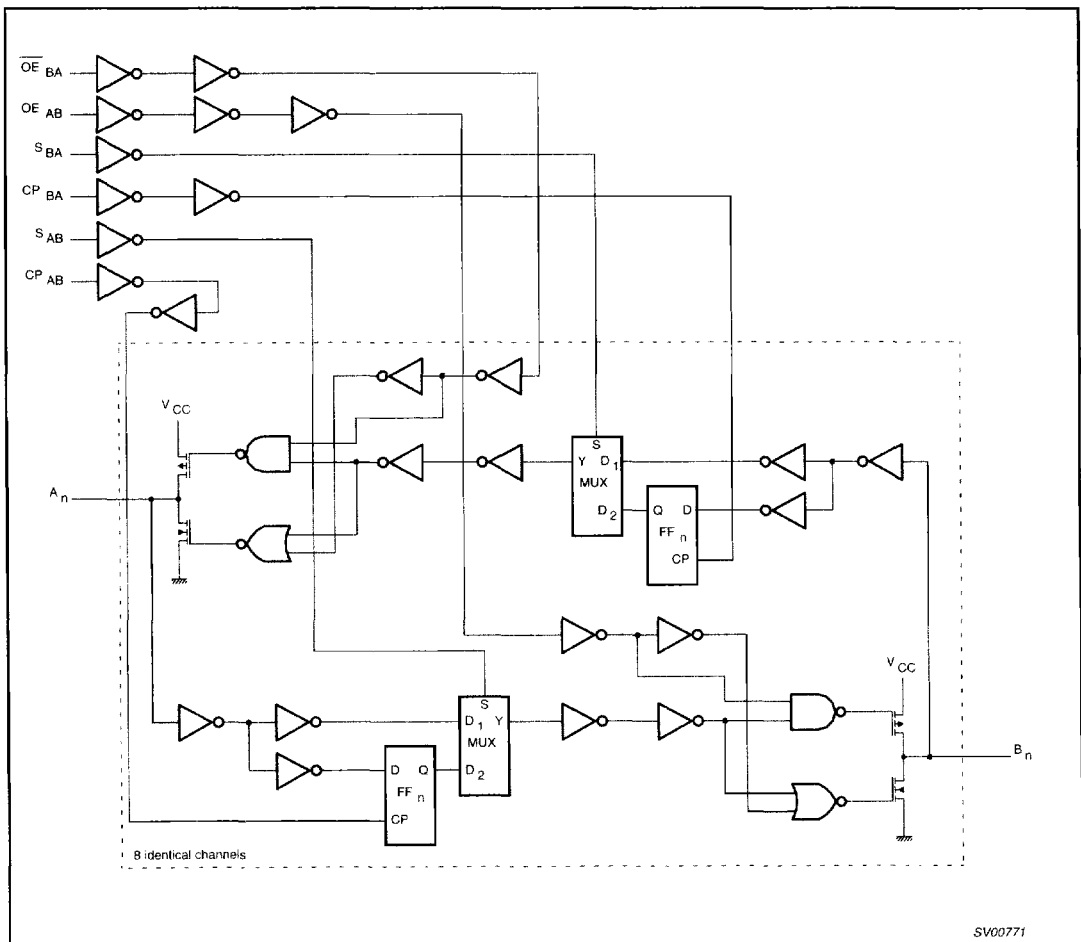
## LOGIC SYMBOL (IEEE/IEC)



# Octal transceiver/register with dual enable (3-State)

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## LOGIC DIAGRAM



## Octal transceiver/register with dual enable (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V <sub>I</sub>	DC input voltage range		0	5.5	V
V <sub>I/O</sub>	DC input voltage range for I/Os		0	V <sub>CC</sub>	V
V <sub>O</sub>	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7V V <sub>CC</sub> = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage	Note 2	-0.5 to +5.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	± 50	mA
V <sub>I/O</sub>	DC output voltage; output HIGH or LOW	Note 2	-0.5 to V <sub>CC</sub> + 0.5	V
	DC input voltage; output 3-State	Note 2	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	DC output diode current	V <sub>O</sub> = 0 to V <sub>CC</sub>	± 50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		± 100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Octal transceiver/register with dual enable (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = -40°C to +85°C				
			MIN	TYP <sup>1</sup>	MAX		
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V	
		V <sub>CC</sub> = 2.7 to 3.6V	2.0				
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V	
		V <sub>CC</sub> = 2.7 to 3.6V			0.8		
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6				
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8				
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55		
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND	Not for I/O pins		± 0.1	± 5	μA
I <sub>IHZ</sub> /I <sub>ILZ</sub>	Input current for common I/O pins	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND			± 0.1	± 15	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND			0.1	± 10	μA
I <sub>OFF</sub>	Power off leakage current	V <sub>CC</sub> = 0.0V; V <sub>I</sub> = 5.5V; V <sub>O</sub> = 5.5V			0.1	± 10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0			0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0			5	500	μA

**NOTES:**

- All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT	
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	MIN		TYP
$t_{PHL}/t_{PLH}$	Propagation delay An to Bn, Bn to An	Figures 1, 5	1.5	4.6	7.9	1.5	9.2	1.5	24	ns
$t_{PHL}/t_{PLH}$	Propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	Figures 2, 5	1.5	5.2	8.9	1.5	11	1.5	26	ns
$t_{PHL}/t_{PLH}$	Propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	Figures 3, 5	1.5	5.2	8.8	1.5	11	1.5	27	ns
$t_{PZH}/t_{PZL}$	3-State output enable time OE <sub>AB</sub> to B <sub>n</sub>	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time OE <sub>AB</sub> to B <sub>n</sub>	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
$t_{PZH}/t_{PZL}$	3-State output enable time OE <sub>BA</sub> to A <sub>n</sub>	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time OE <sub>BA</sub> to A <sub>n</sub>	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
$t_W$	Clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	Figures 4, 5	-	3.0	-	3.0	-	-	-	ns
$t_{su}$	Set-up time An, Bn to CP <sub>AB</sub> , CP <sub>BA</sub>	Figure 2	1.5	0.5	-	1.5	-	-	-	ns
$t_h$	Hold time An, Bn to CP <sub>AB</sub> , CP <sub>BA</sub>	Figure 2	1.0	0	-	1.0	-	-	-	ns
$f_{max}$	Maximum clock pulse frequency	Figure 2	7.5	150	-	-	-	-	-	MHz

**NOTE:**

1. These typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$

$V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$

$V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$

$V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

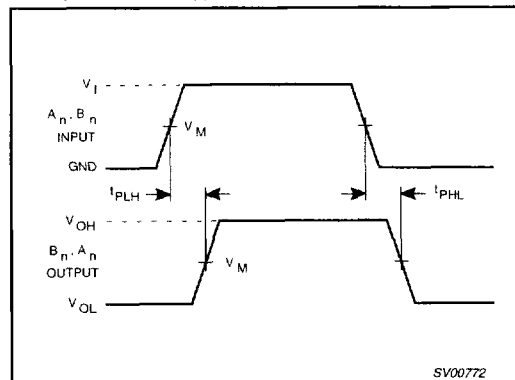


Figure 1. Input An, Bn to output Bn, An propagation delays.

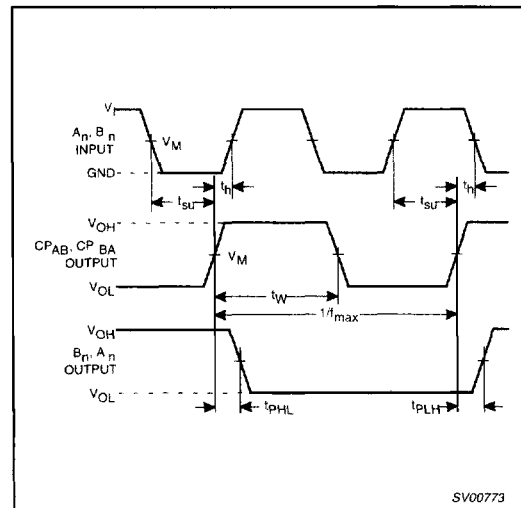


Figure 2. An, Bn to CP<sub>AB</sub>, CP<sub>BA</sub> set-up and hold times, clock CP<sub>AB</sub>, CP<sub>BA</sub> pulse width, maximum clock pulse frequency and the CP<sub>AB</sub>, CP<sub>BA</sub> to output B<sub>n</sub>, A<sub>n</sub> propagation delays.

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### AC WAVEFORMS (Continued)

- $V_M = 1.5V$  at  $V_{CC} \geq 2.7V$
- $V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$
- $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.
- $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$
- $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

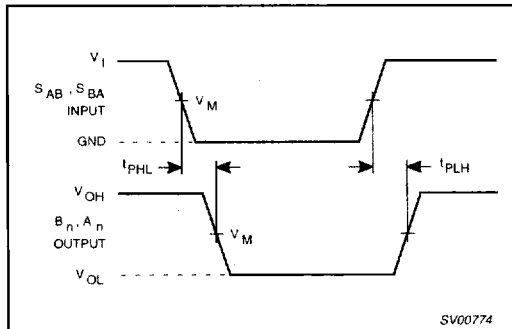


Figure 3. Input  $S_{AB}$ ,  $S_{BA}$  to output  $B_n$ ,  $A_n$  propagation delay times.

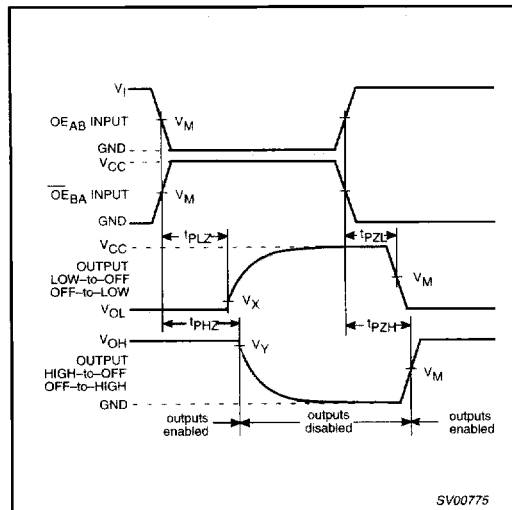


Figure 4. OE inputs ( $OE_{AB}$ ,  $OE_{BA}$ ) to outputs  $A_n$ ,  $B_n$  enable and disable times.

### TEST CIRCUIT

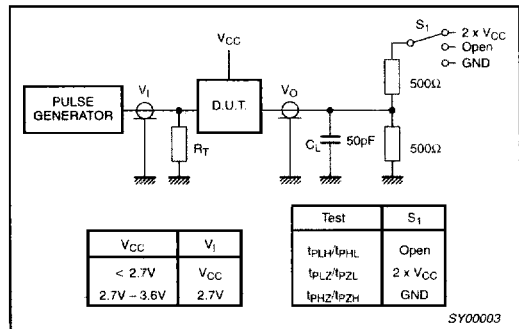


Figure 5. Load circuitry for switching times.

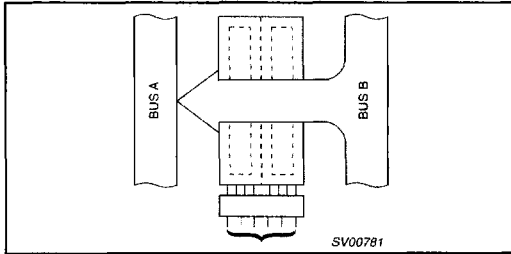


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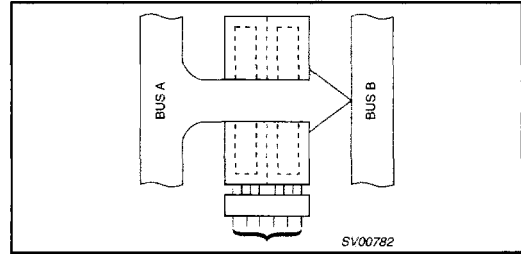
## APPLICATION INFORMATION

Real-time transfer; bus B to bus A



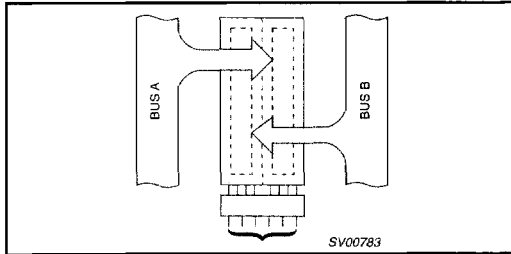
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	L	X	X	X	L

Real-time transfer; bus A to bus B



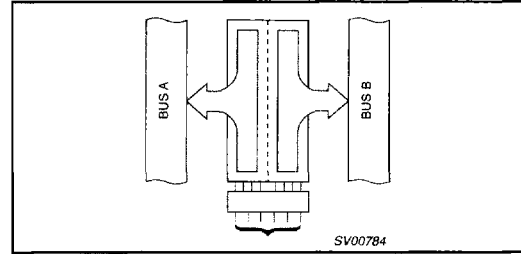
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
H	H	X	X	L	X

Store A, B or A and B in one register



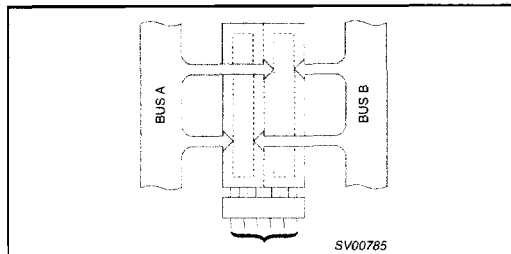
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
X	H	↑	↑	L	X
L	X	X	X	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



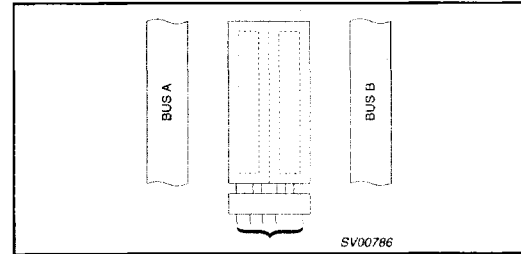
OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE <sub>AB</sub>	OE <sub>BA</sub>	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	H	H or L	H or L	X	X