54F/74F114

Dual JK Negative Edge-Triggered Flip-Flop With Common Clocks and Clears

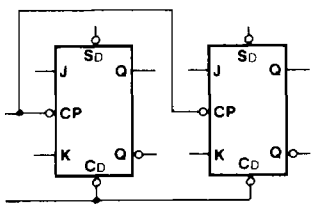
Description

The 'F114 contains two high-speed JK flip-flops with common Clock and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

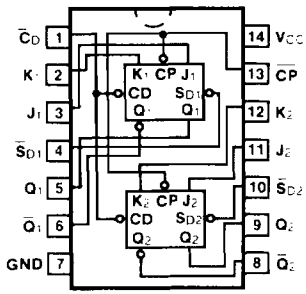
Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
- LOW input to $\overline{C}_D$ sets Q to LOW level
- Clear and Set are independent of Clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code: See Section 5

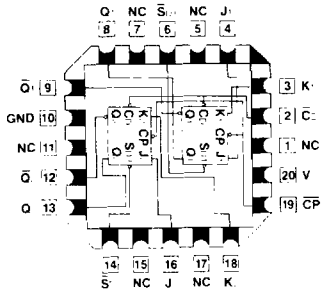
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

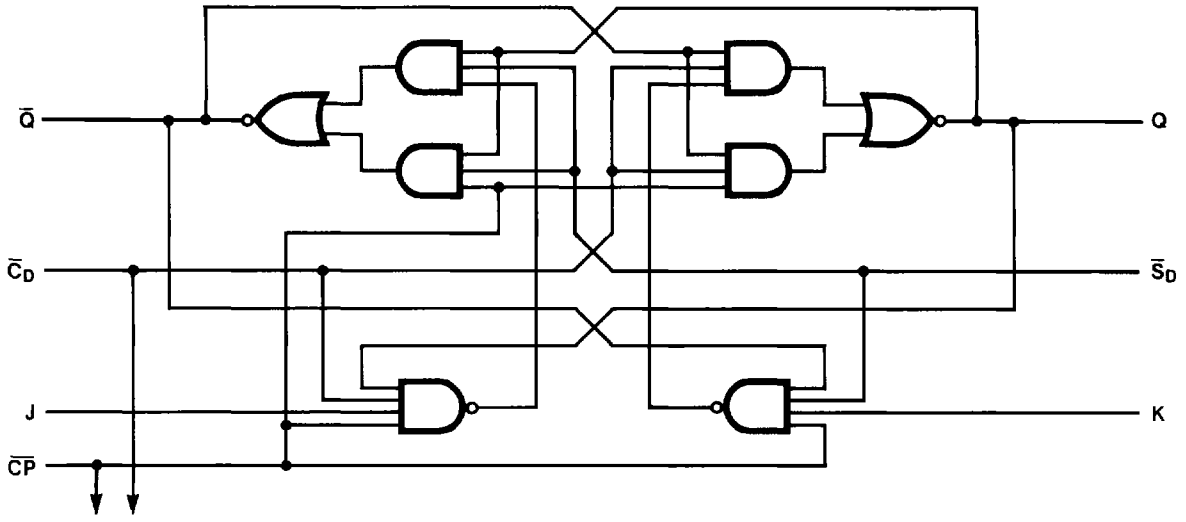
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	0.5/0.375
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/3.0
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/3.7
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.875
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

Truth Table

Inputs		Output
$@t_n$		$@t_n$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	19	mA	V_{CC} = Max, V_{CP} = 0

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125				90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	3.0 3.0	5.0 5.5	6.5 7.5			3.0 3.0	7.5 8.5	ns	3-1 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_D$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.0 3.0	4.5 4.5	6.5 6.5			3.0 3.0	7.5 7.5	ns	3-1 3-9

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}$	4.0 3.0					5.0 3.5		ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}$	0 0					0 0			
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse Width HIGH or LOW	4.5 4.5					5.0 5.0		ns	3-8
$t_w(L)$	$\overline{C}_D$ or $\overline{S}_{Dn}$ Pulse Width, LOW	4.5					5.0		ns	3-9
t_{rec}	$\overline{C}_D$ or $\overline{S}_{Dn}$ to $\overline{CP}$ Recovery Time	4.0					5.0		ns	3-11