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# HM624256A Series

262144-word × 4-bit High Speed CMOS Static RAM

# HITACHI

Rev. 0.0  
Dec. 1, 1995

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## Description

The Hitachi HM624256A is a high speed 1M Static RAM organized as 262,144-word × 4-bit. It realizes high speed access time (20/25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM624256A, packaged in a 400-mil plastic SOJ is available for high density mounting.

## Features

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed  
Access time: 20/25/35 ns (max)
- Low power dissipation  
Active mode: 350 mW (typ)  
Standby mode: 100 μW (typ)
- Completely static memory  
No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible  
All inputs and outputs

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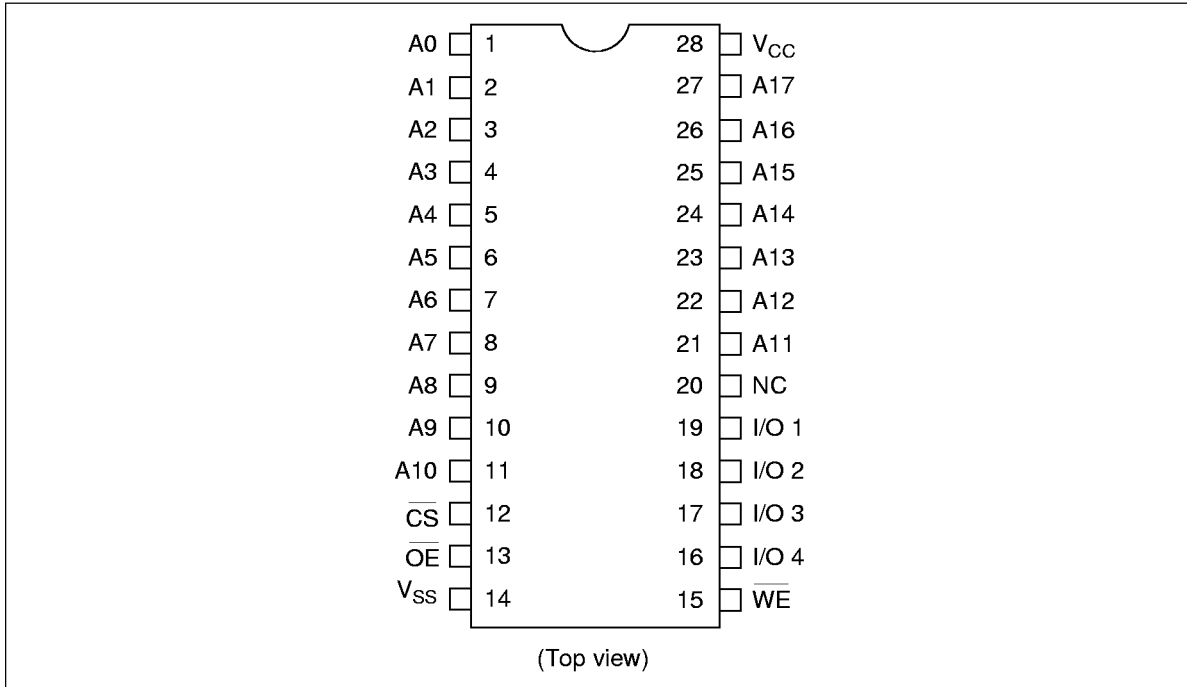
## HM624256A Series

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### Ordering Information

Type No.	Access Time	Package
HM624256AP-20	20 ns	400 mil 28-pin plastic DIP (DP-28C)
HM624256AP-25	25 ns	
HM624256AP-35	35 ns	
HM624256ALP-20	20 ns	400 mil 28-pin plastic SOJ (CP-28D)
HM624256ALP-25	25 ns	
HM624256ALP-35	35 ns	
HM624256AJP-20	20 ns	400 mil 28-pin plastic SOJ (CP-28D)
HM624256AJP-25	25 ns	
HM624256AJP-35	35 ns	
HM624256ALJP-20	20 ns	400 mil 28-pin plastic SOJ (CP-28D)
HM624256ALJP-25	25 ns	
HM624256ALJP-35	35 ns	

**Pin Arrangement**

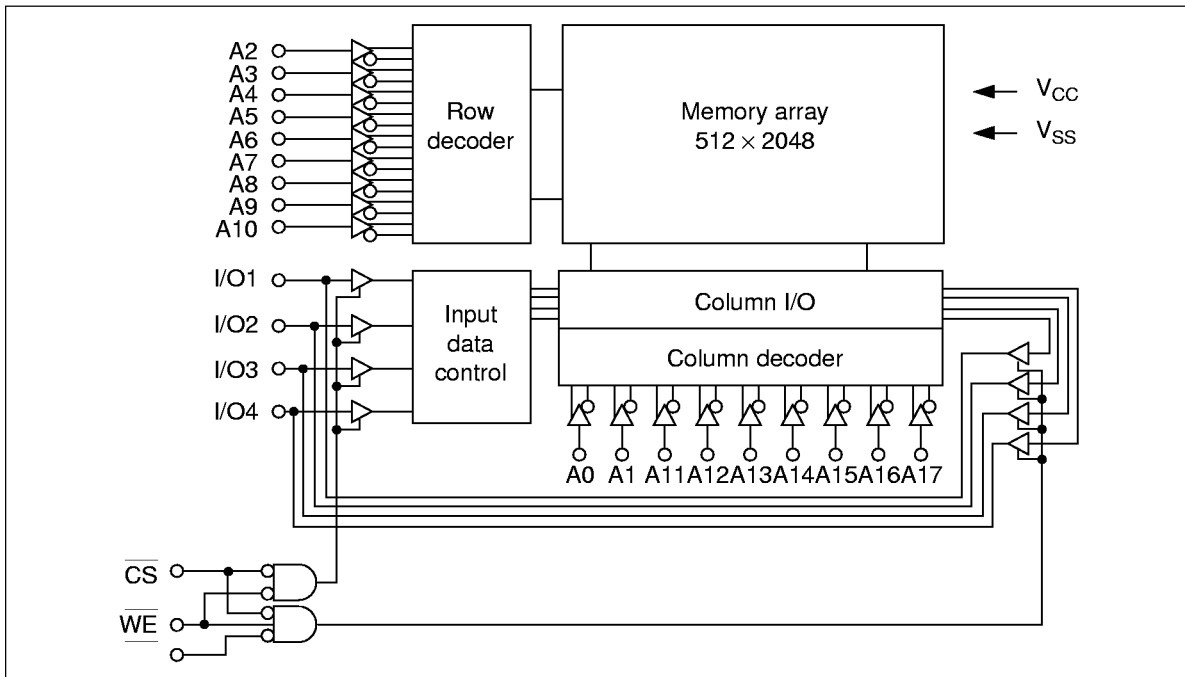


**Pin Description**

Pin Name	Function
A0 – A17	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$V_{cc}$	Power supply
$V_{ss}$	Ground

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## Block Diagram



## Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	$V_{CC}$ Current	I/O Pin	Ref. Cycle
H	X	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
L	L	H	Read	$I_{CC}$	Dout	Read cycle (1) – (3)
L	H	L	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: X: H or L

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{in}$	$-0.5^{*1}$ to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature range	$T_{opr}$	0 to +70	°C
Storage temperature range	$T_{stg}$	-55 to +125	°C
Storage temperature range under bias	$T_{bias}$	-10 to +85	°C

Note: 1.  $V_{in\ min} = -2.0\ V$  for pulse width  $\leq 10\ ns$

## HM624256A Series

### Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>IH</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>IL</sub>	-0.5 <sup>1</sup>	—	0.8	V

Note: 1. V<sub>IL</sub> min = -2.0 V for pulse width ≤ 10 ns

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	HM624256A-20			HM624256A-25/35			Unit	Test Conditions
		Min	Typ <sup>1</sup>	Max	Min	Typ <sup>1</sup>	Max		
Input leakage current	I <sub>LI</sub>	—	—	2.0	—	—	2.0	μA	V <sub>CC</sub> = max V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	2.0	—	—	2.0	μA	$\overline{CS} = V_{IH}$ V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current	I <sub>CC</sub>	—	—	150	—	—	120	mA	$\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA, min cycle
Standby power supply current	I <sub>SB</sub>	—	—	60	—	—	40	mA	$\overline{CS} = V_{IH}$ , min cycle
Standby power supply current (1)	I <sub>SB1</sub>	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2$ V 0 V ≤ V <sub>in</sub> ≤ 0.2 V or V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V
	I <sub>SB1</sub> <sup>2</sup>	—	—	100 <sup>2</sup>	—	—	100 <sup>2</sup>	μA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	—	—	0.4	V	I <sub>OL</sub> = 8 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	2.4	—	—	V	I <sub>OH</sub> = -4 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

2. L-version

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	5 <sup>2</sup>	pF	V <sub>in</sub> = 0 V
		—	6 <sup>3</sup>	pF	
Input/output capacitance	C <sub>I/O</sub>	—	8	pF	V <sub>I/O</sub> = 0 V

Notes: 1. This parameter is sampled and not 100% tested.

2. SOJ package

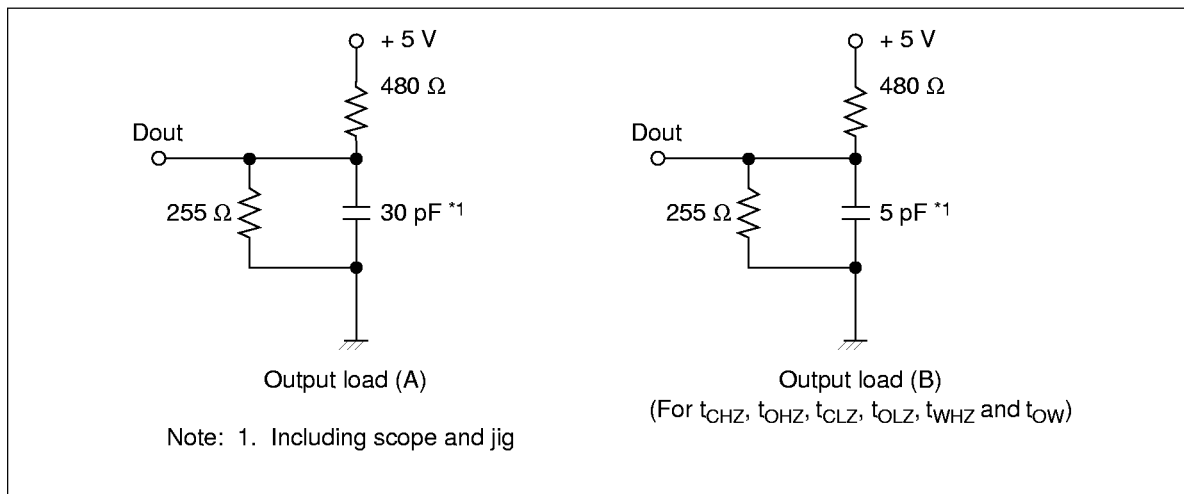
3. DIP package

## HM624256A Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels: 0V to 3.0 V
- Input rise and fall time: 4 ns
- Input timing reference levels: 1.5 V
- Output timing reference levels: 1.5 V
- Output load: See figures

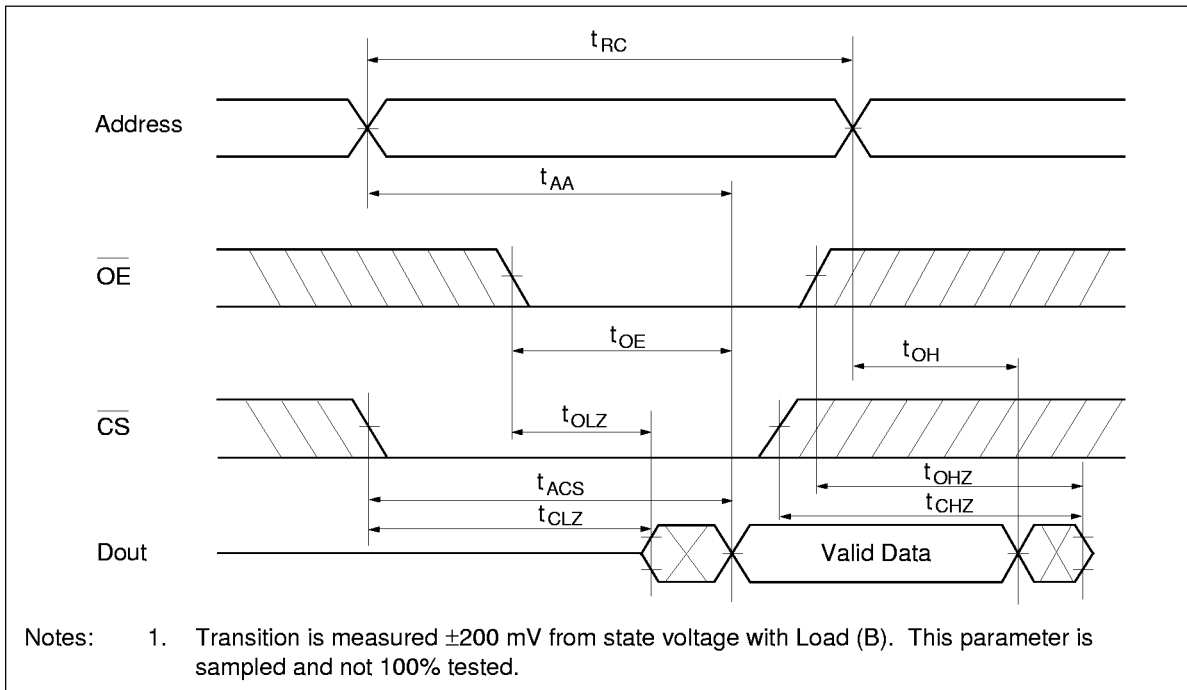


### Read Cycle

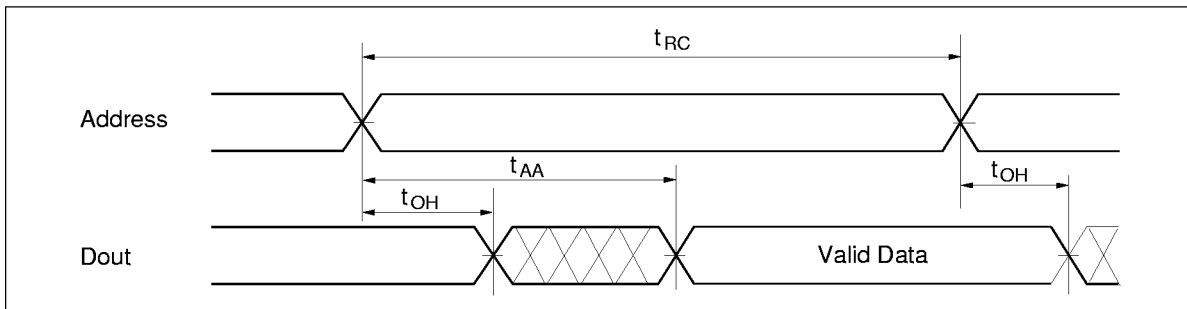
Parameter	Symbol	HM624256A-20		HM624256A-25		HM624256A-35		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	$t_{RC}$	20	—	25	—	35	—	ns
Address access time	$t_{AA}$	—	20	—	25	—	35	ns
Chip select access time	$t_{ACS}$	—	20	—	25	—	35	ns
Chip selection to output in low-Z	$t_{CLZ}^{*1}$	5	—	5	—	5	—	ns
Output enable to output valid	$t_{OE}$	—	10	—	12	—	15	ns
Output enable to output in low-Z	$t_{OLZ}^{*1}$	0	—	0	—	0	—	ns
Chip deselection to output in high-Z	$t_{CHZ}^{*1}$	0	10	0	12	0	15	ns
Chip disable to output in high-Z	$t_{OHZ}^{*1}$	0	10	0	10	0	10	ns
Output hold from address change	$t_{OH}$	5	—	5	—	5	—	ns
Chip selection to power up time	$t_{PU}$	0	—	0	—	0	—	ns
Chip deselection to power down time	$t_{PD}$	—	12	—	15	—	25	ns

Notes: 1. Transition is measured  $\pm 200$  mV from steady state voltage with Load (B). This parameter is sampled not 100% tested.

Read Timing Waveform (1)\*1 ( $\overline{WE} = V_{IH}$ )

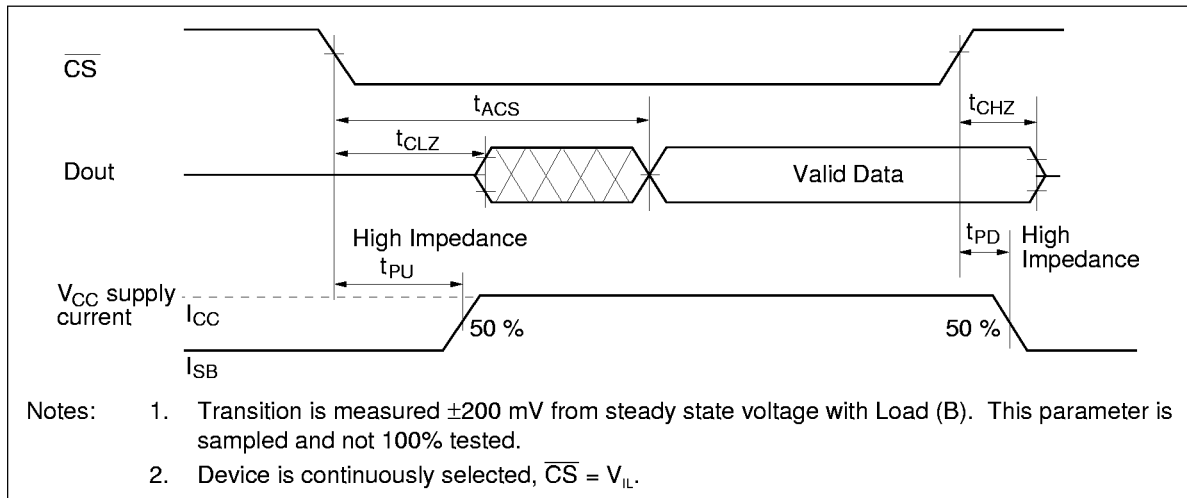


Read Timing Waveform (2) ( $\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$ )



## HM624256A Series

### Read Timing Waveform (3)<sup>\*1, \*2</sup> ( $\overline{WE} = V_{IH}$ , $\overline{OE} = V_{IL}$ )



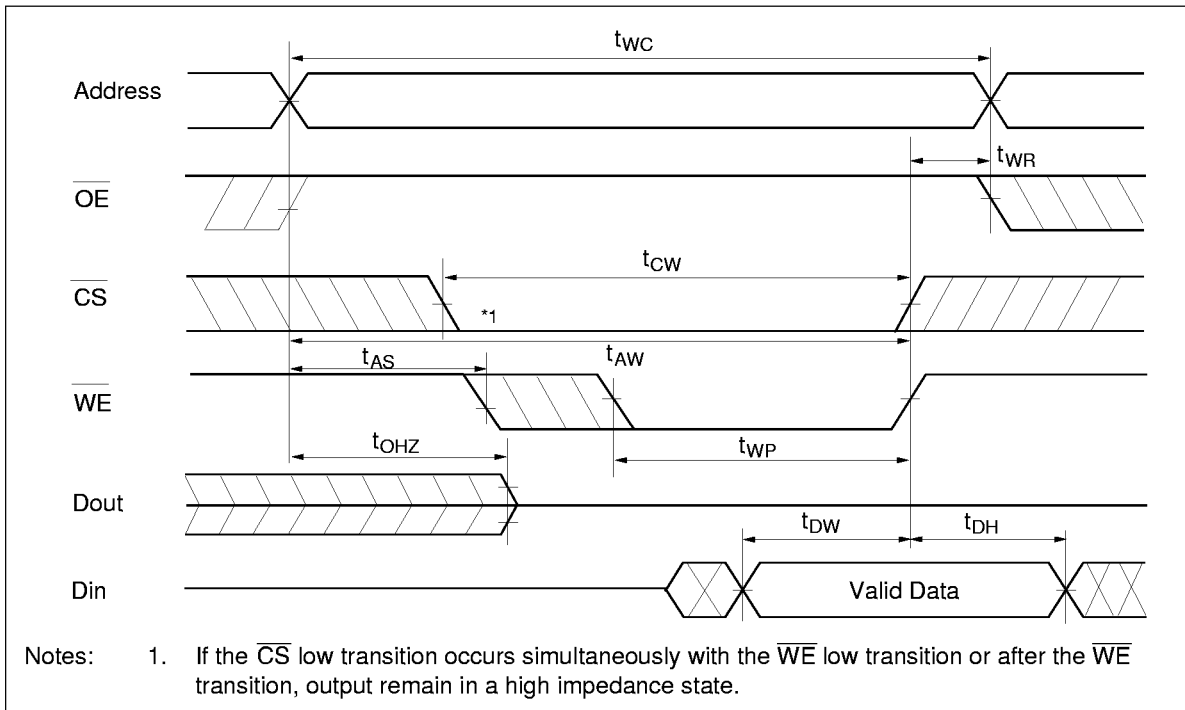
### Write Cycle

Parameter	Symbol	HM624256A-20		HM624256A-25		HM624256A-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	$t_{WC}$	20	—	25	—	35	—	ns
Chip selection to end of write	$t_{CW}$	15	—	17	—	25	—	ns
Address valid to end of write	$t_{AW}$	16	—	20	—	30	—	ns
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns
Write pulse width	$t_{WP}^{*2}$	15	—	17	—	25	—	ns
Write recovery time	$t_{WR}^{*3}$	0	—	0	—	0	—	ns
Output disable to output in high-Z	$t_{OHZ}^{*4}$	0	10	0	10	0	10	ns
Write to output in high-Z	$t_{WHZ}^{*4}$	0	12	0	15	0	15	ns
Data to write time overlap	$t_{DW}$	12	—	15	—	20	—	ns
Data hold from write time	$t_{DH}^{*5}$	0	—	0	—	0	—	ns
Output active from end of write	$t_{OW}^{*1}$	0	—	0	—	0	—	ns

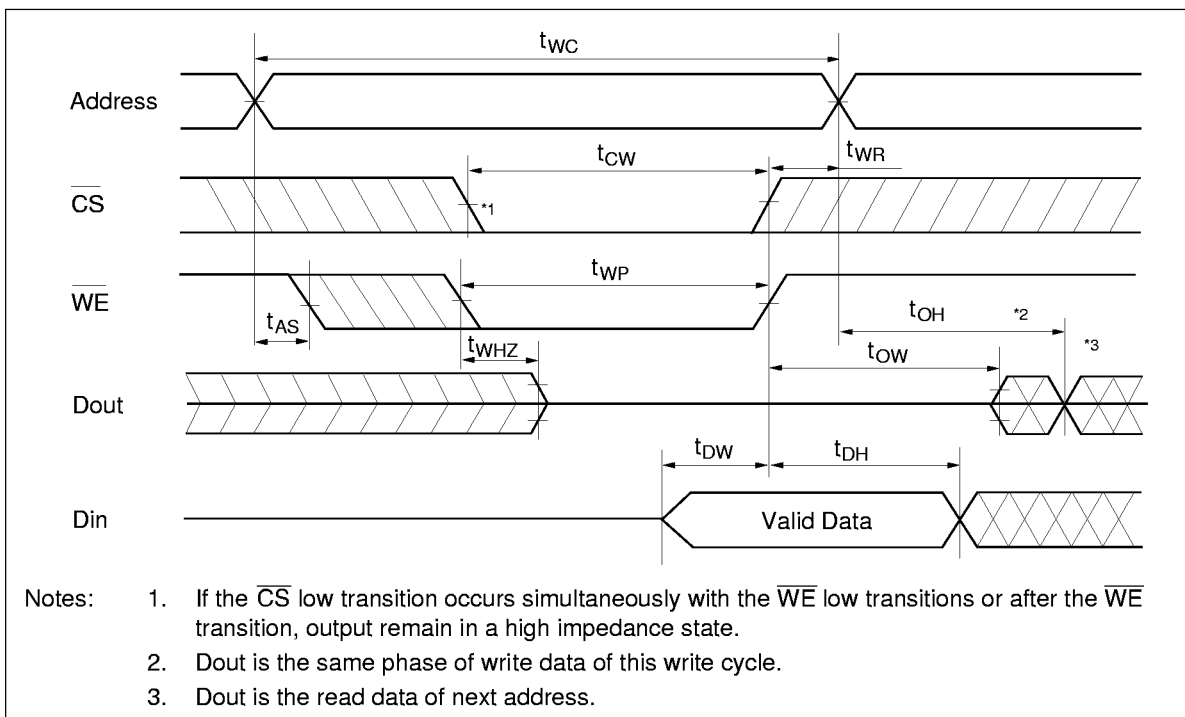
- Notes:
1. Transition is measured  $\pm 200$  mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
  2. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
  3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
  4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
  5. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.



Write Timing Waveform (1)



Write Timing Waveform (2) ( $\overline{OE}$  Low Fixed)



## HM624256A Series

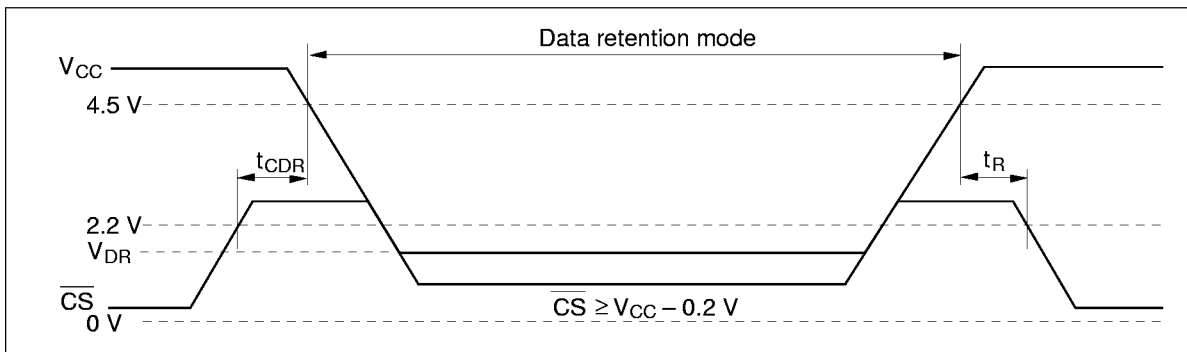
### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	2	$50^{*1}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1.  $V_{CC} = 3.0 \text{ V}$

### Low $V_{CC}$ Data Retention Timing Waveform

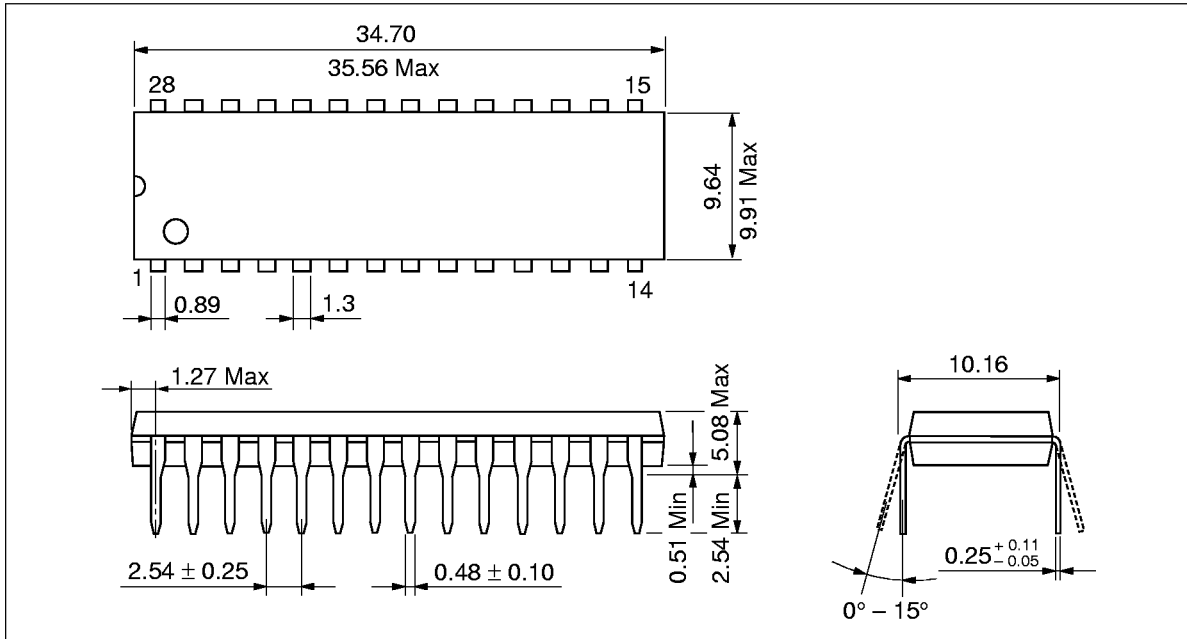


# HM624256A Series

## Package Dimensions

HM624256AP/ALP Series (DP-28C)

Unit: mm



# HM624256A Series

HM624256AJP/ALJP Series (CP-28D)

Unit: mm

