Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

IDT7134S
IDT7134L

FEATURES:

- High-speed access
  - — Military: 45/55/70ns (max.)
  - — Commercial: 35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

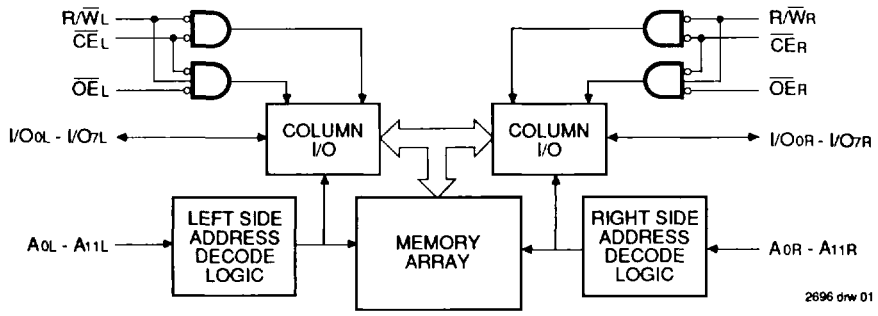
The IDT7134 is a high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port RAM location.

The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual-ports typically operate on only 500mW of power at maximum access times as fast as 35ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin or 52-pin LCC, and 52-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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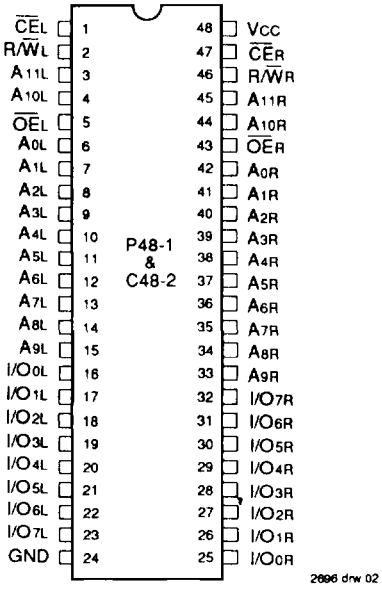
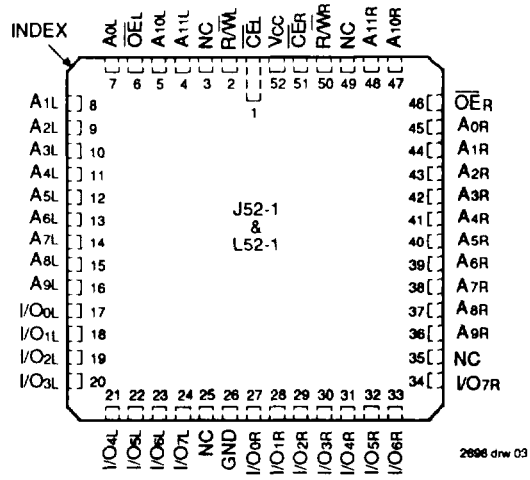
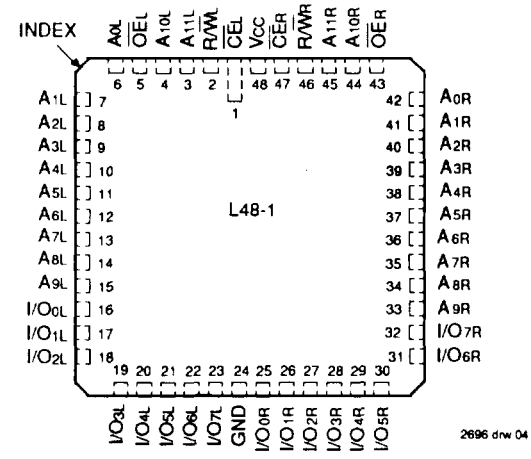
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

NOTE: 2696 tbl 01

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2696 tbl 02

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2696 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. VIL (min.) = -3.0V for pulse width less than 20ns.

2696 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134S		IDT7134L		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage	IOL = 6mA	—	0.4	—	0.4	V
		IOL = 8mA	—	0.5	—	0.5	
VOH	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

2696 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		IDT7134x35(4)		IDT7134x45		IDT7134x55		IDT7134x70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open, f = fMAX(3)	MIL.	S	—	—	100	240	100	230	100	230	mA
				L	—	—	100	200	100	180	100	180	
			COM'L.	S	100	220	100	200	100	200	100	200	
				L	100	180	100	160	100	160	100	160	
ISB1	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq$ VIH, f = fMAX(3)	MIL.	S	—	—	25	70	25	70	25	70	mA
				L	—	—	25	50	25	50	25	50	
			COM'L.	S	25	75	25	70	25	70	25	70	
				L	25	45	25	40	25	40	25	40	
ISB2	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq$ VIH, Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	50	160	50	150	50	150	mA
				L	—	—	50	130	50	120	50	120	
			COM'L.	S	50	140	50	130	50	130	50	130	
				L	50	110	50	100	50	100	50	100	
ISB3	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ & $\overline{CE}_R \geq$ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, f = 0(3)	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
ISB4	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq$ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	50	130	50	120	50	120	mA
				L	—	—	45	100	45	90	45	90	
			COM'L.	S	45	120	45	110	45	110	45	110	
				L	45	100	45	90	45	90	45	90	

NOTES:
1. "x" in part number indicates power rating (S or L).
2. Vcc = 5V, TA = +25°C.
3. fMAX = 1/tRC = All inputs cycling at f = 1/tRC (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby ISB3.
4. 0°C to +70°C temperature range.

2696 tbl 06

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES[1]

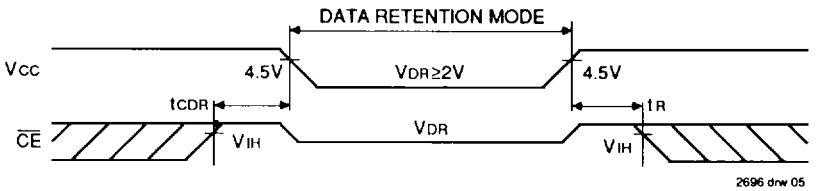
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2696 tbl 07

LOW Vcc DATA RETENTION WAVEFORM



2696 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2696 tbl 08

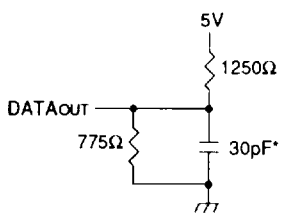
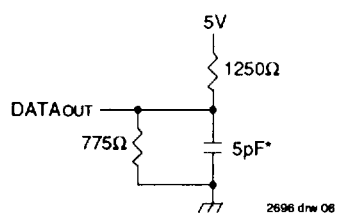


Figure 1. Output Load



2696 drw 06

Figure 2. Output Load (for tLZ, tHZ, tWZ, tOW)

*Including scope and jig

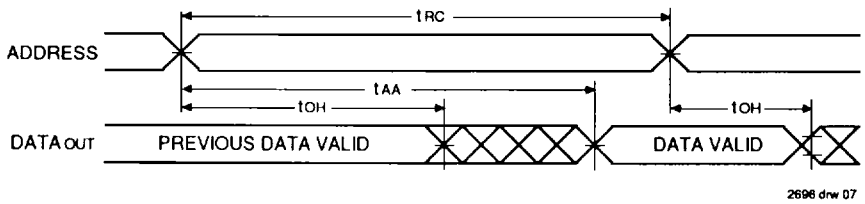
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7134S35[3] IDT7134L35[3]		IDT7134S45 IDT7134L45		IDT7134S55 IDT7134L55		IDT7134S70 IDT7134L70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	25	—	30	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tLZ	Output Low Z Time[1, 2]	5	—	5	—	5	—	5	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	20	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	—	50	ns

2698 tbl 10

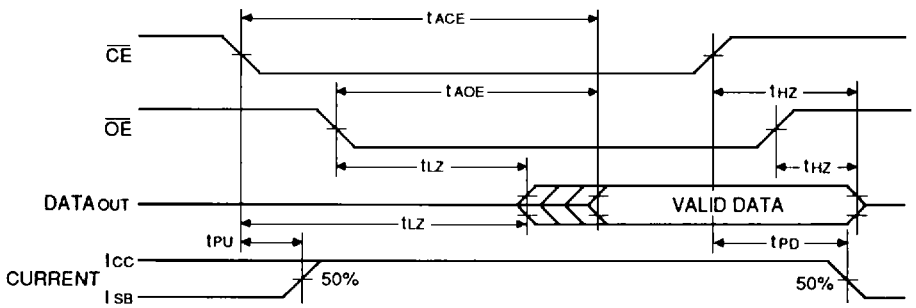
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2698 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2698 drw 08

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to or coincident with CE transition low.
4. OE = VIL.

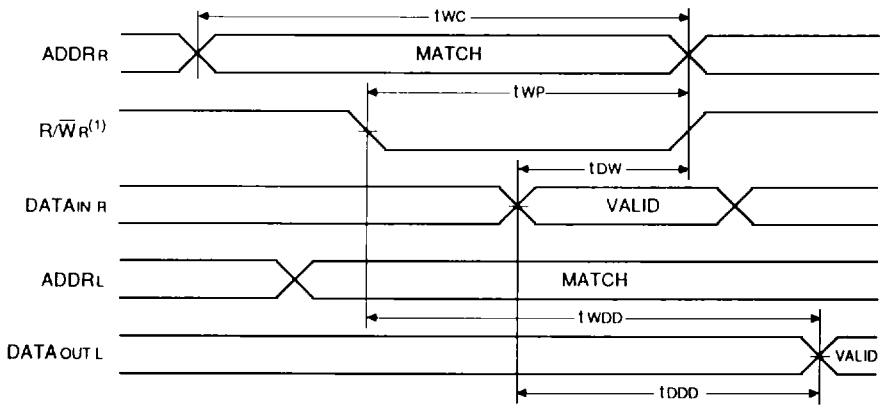
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7134S35[5] IDT7134L35[5]		IDT7134S45 IDT7134L45		IDT7134S55 IDT7134L55		IDT7134S70 IDT7134L70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End of Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	20	—	20	—	25	—	30	—	ns
tHZ	Output High Z Time[1, 2]	—	20	—	20	—	25	—	30	ns
tDH	Data Hold Time[3]	3	—	3	—	3	—	3	—	ns
tWZ	Write Enabled to Output in High Z[1, 2]	—	20	—	20	—	25	—	30	ns
tOW	Output Active from End of Write[1, 2, 3]	3	—	3	—	3	—	3	—	ns
tWDD	Write Pulse to Data Delay[4]	—	80	—	80	—	80	—	90	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	55	—	55	—	55	—	70	ns

NOTES:
2696 tbl 10

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2)
2. This parameter is guaranteed but not tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with Port-to-Port Delay".
5. 0°C to +70°C temperature range only.
6. Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).

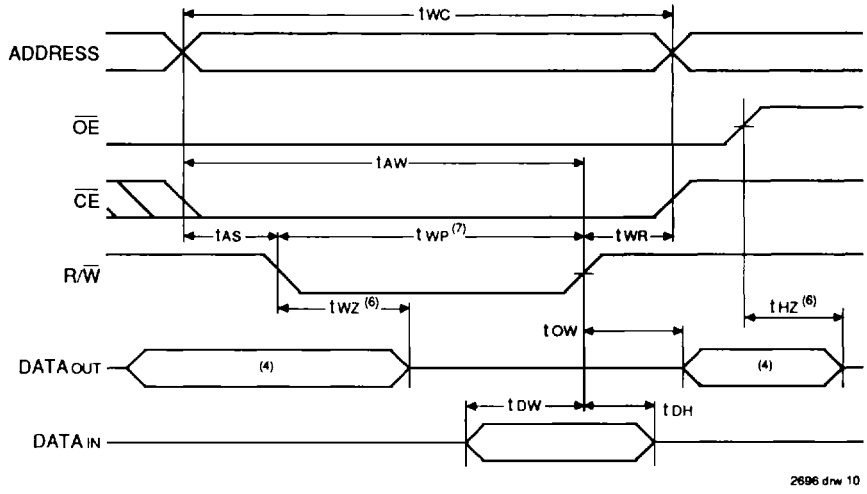
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY[1]



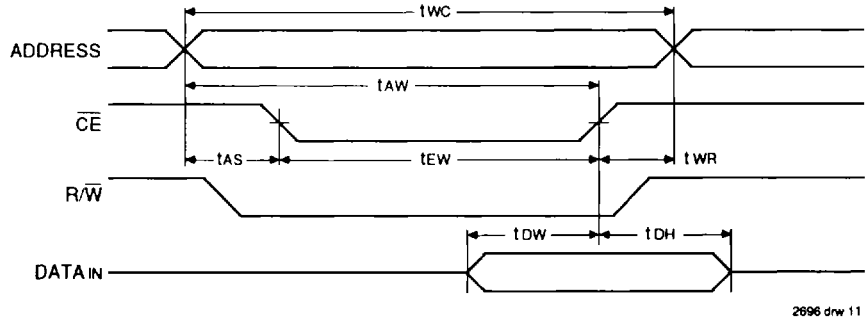
2696 drw 09

NOTES:
1. Write cycle parameters should be adhered to in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 2, 3, 4, 6, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 2, 3, 5)



NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .

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FUNCTIONAL DESCRIPTION:

The IDT7134 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

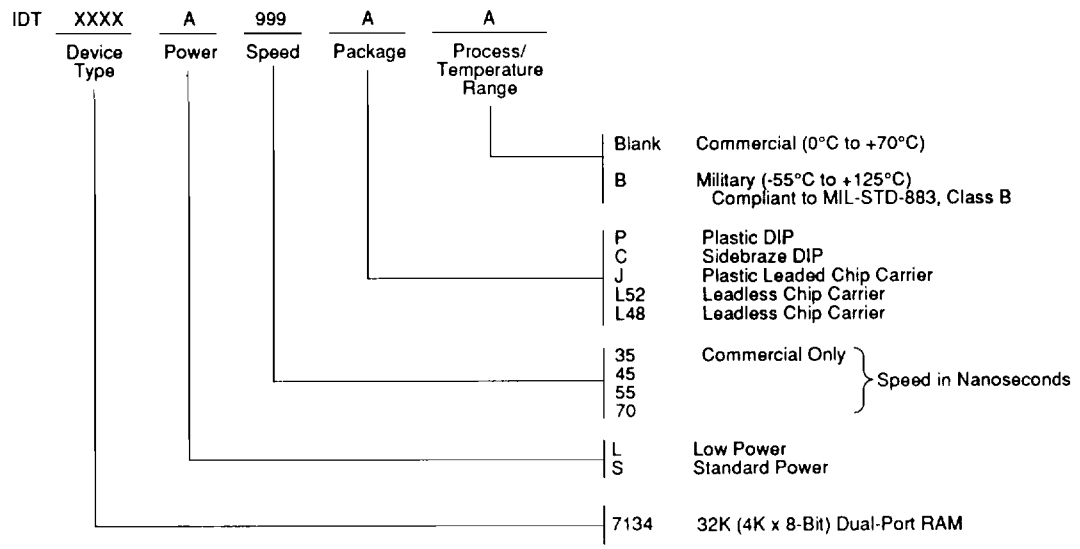
TABLE I – READ/WRITE CONTROL

Left or Right Port[1]				
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = H$, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

NOTES: 2696 tbl 11

1. $A_{0L} - A_{11L} \neq A_{0R} - A_{11R}$
   H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ORDERING INFORMATION



2696 drw 12